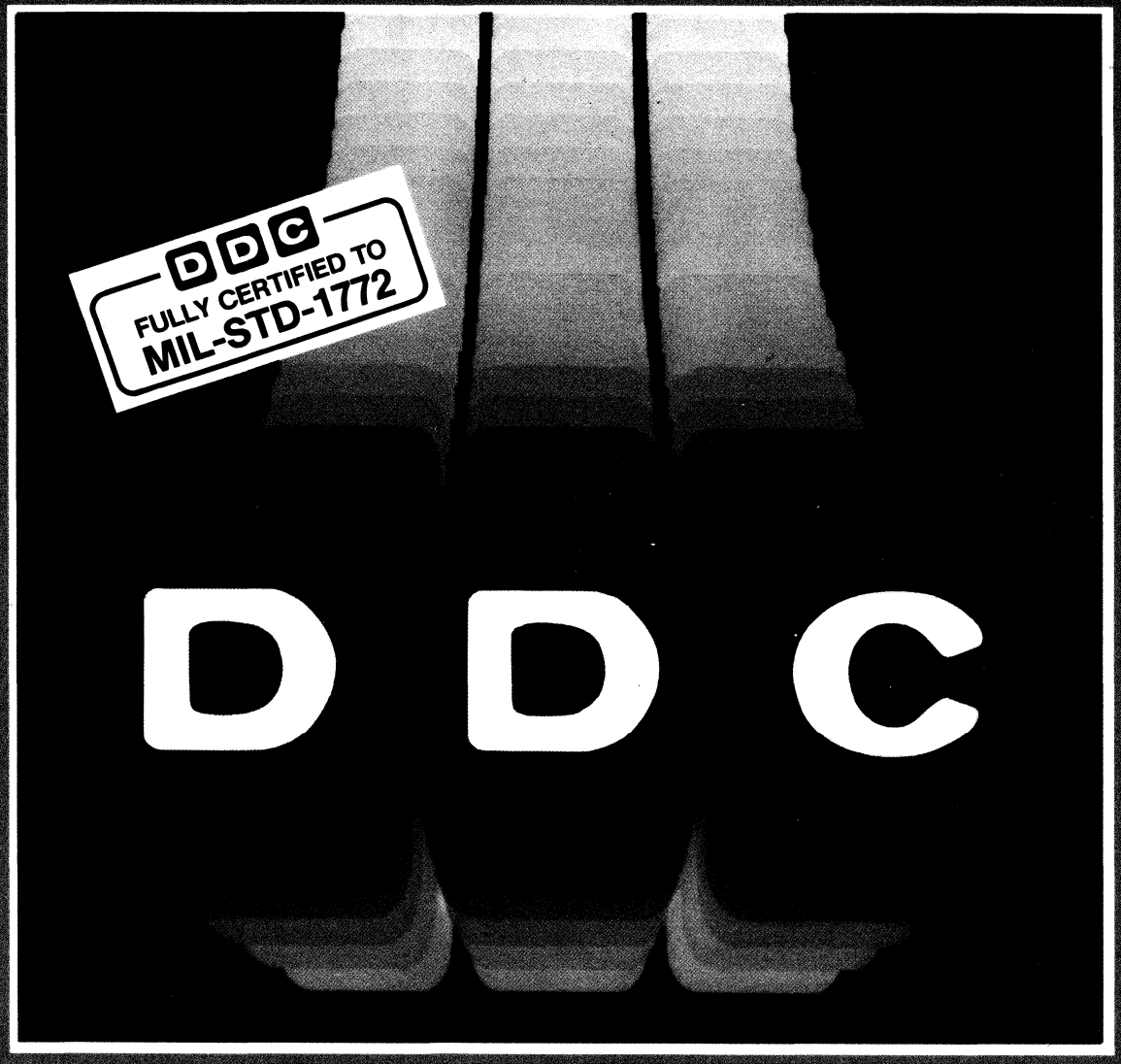
AUGUST 1984

DATA CONVERTERS



Product Catalog

ILC DATA DEVICE CORPORATION

INTRODUCTION

ILC Data Device Corporation was incorporated in 1964 as a supplier of high performance operational amplifiers. From its inception, emphasis has been placed on state of the art, high quality data and signal conversion components and systems. In 1971 DDC was acquired by ILC Industries, sole supplier of the Apollo, Skylab and Shuttle space suits. Since its acquisition by ILC Industries, DDC has accelerated its progress in the data conversion field and is today the leading supplier of synchro conversion equipment and a dominant supplier of high performance A/D and D/A conversion equipment. DDC's present capability encompasses diversity in the design and production of high quality discrete and hybrid data conversion components and systems. This diversification, combined with research proficiency, manufacturing expertise and strong customer support is responsible for the company's recognized reputation for excellence.

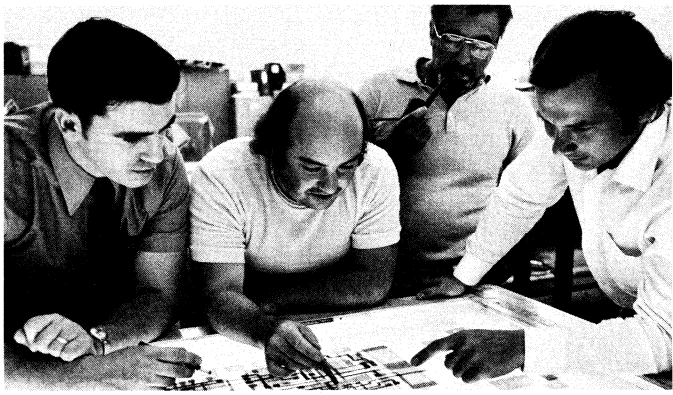
DDC boasts a complete design engineering function integrated with a sophisticated manufacturing operation whose capability ranges from production quantities of standard components to custom circuitry requiring comprehensive engineering, production and quality. A staff of highly trained application specialists provides the know-how and ability to work with customers in solving challenging design problems and insuring proper application and support of DDC furnished equipment.

FACILITIES

DDC is headquartered in Bohemia, Long Island, New York, where it occupies 130,000 square feet of space in two adjacent buildings in the Airport International Plaza. A 50,000 square foot addition to the main building houses one of the most modern thick and thin film hybrid manufacturing operations in the industry. An elaborate environmental control system enables the Company to qualify its products to high performance and reliability standards such as MIL-Q-9858A, MIL-STD-883C and MIL-STD-1772. DDC is certified as a QPL supplier of SEM modules to MIL-M-28787 and has provided equipment meeting the reliability levels required for manned space flight. The second building houses DDC's Engineering Division where a highly specialized staff engages in state-of-the-art analog and digital circuit design. Our capabilities include the design of monolithic components, computer interfaces, instrumentation and custom hybrid circuits. An extensive model shop for pilot production and experimental work completes this facility.

DDC is conveniently located next to Long Island MacArthur (formerly Islip) Airport which offers both non-stop service to Boston, Washington, Pittsburgh and several other major east coast cities and convenient transportation to and from the two New York City airports.

DDC maintains domestic regional sales offices in Woodland Hills, California, Santa Clara, California and Vienna, Virginia. Foreign offices are maintained in England, France, Germany and Japan. A sales representative force, covering



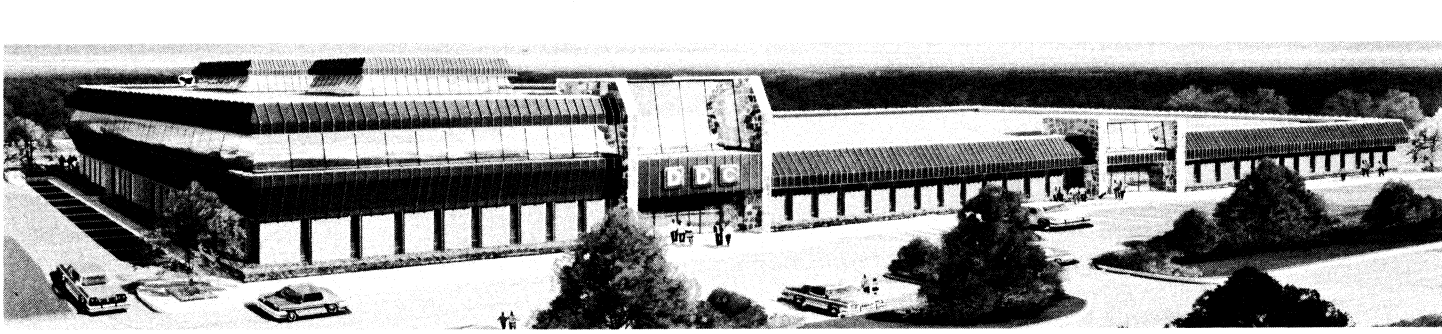
the United States, Canada, Western Europe, Far and Middl East Sections rounds out our sales organization.

ABOUT THIS CATALOG

While preparing this catalog, we have attempted to organize product and related information in such a manner as to minimize the amount of time it will take to locate the information required. DDC's Data Conversion Products have, therefore been organized into nine general categories presented in Sections A through I. The Table of Contents identifies each section and lists the page numbers where they can be located Several special features have been incorporated in this catalog. Each section is preceded by a discussion of the theory of operation and pertinent application notes. In addition to the Table of Contents, an alphanumeric product index listing all of DDC's Data Conversion products can be found on the last page. Each of the nine sections begins with a product selection guide to help you find the group of products you are interested in by summarizing some key features of each device. Other information in this catalog will acquaint you with our company by giving a brief history and description of DDC's facilities, capabilities, quality assurance system, and other operating groups.

To illustrate how to use this catalog efficiently, we will give a few examples. If you are looking for information on a specific product, such as an ADH-8516, use the product index guide on the last page to locate the appropriate page number for the ADH-8516. If you are looking for a particular type of converter, such as a 12 bit A/D converter, look up the product summary table page number in the Table of Contents under the Analog to Digital Section. Turn to that page and you will find A/D converters grouped together with key parameters. For additional information on products found there follow the procedure outlined in the first example.

The information on each product contained in the catalog is designed to give all of the information necessary to choose the precise product for your application. Each detail data sheet is self-contained; all electrical and mechanical information is neatly condensed. Military specifications, where applicable, are also listed. Finally, if you still have questions after reading this catalog, we invite you to contact our highly-trained factory applications engineering staff or our field sales representative.



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NOTE: New products are highlighted in grey.

CAPABILITIES

ENGINEERING

During the last several years, DDC has put together a staff of highly specialized engineers, whose capabilities include state-of-the-art analog and digital circuit design, computer interfaces, instrumentation, data conversion system design, and thick-film hybrid design and packaging. A fully-equipped engineering department for the design of proprietary products and custom electronics, as well as subsystems and systems is key to our leadership position in data conversion electronics. Development and fabrication capability in two model shops (Thick-Film Hybrid and Discrete) plus a fully-equipped laboratory complement a large and modern design and drafting department. Approximately 20 percent of the plant is dedicated to engineering, an exceptionally high percentage for a manufacturing company. In addition, the percentage of our employees involved in the engineering disciplines is exceptionally high for a manufacturing company and indicative of our dedication to stringent performance, high reliability programs requiring specialized engineering talents.

The Engineering Department is capable of initial design, breadboard fabrication and testing, prototype assembly and evaluation, and finally, system and subsystem design, fabrication and testing at a rate of several million dollars annually. Because DDC manufacturing uses two different electronic disciplines (discrete and thick-film hybrid), the Engineering Department maintains two model shops, one for each manufacturing discipline. This allows a quick reaction capability for deliverable product, as well as product evaluation and development with minimal impact upon our continuous production line. Through the utilization of these model shops, new designs and products can be thoroughly tested and evaluated before release to manufacturing.

Design and drafting facilities in a well lit, open area permit DDC to do its own original artwork for printed circuit boards, as well as rubyliths for thick and thin-film hybrids, in addition to the normal product engineering and drafting disciplines that the electronics business demands. A full documentation system is in place, as are reproduction facilities, utilizing both ozalid and xerography for print duplication and distribution. A microfilm specification retrieval system has been in operation for several years. Via this microfilm system, DDC has access to the complete range of military, industrial and commercial standards, specifications and handbooks at its fingertips.

PRODUCT ASSURANCE

At DDC, the Product Assurance function is headed by a Vice President. He has sole responsibility for Product Assurance and reports directly to the President. This ensures independent actions, thereby maintaining integrity of the Product Assurance (Quality, Reliability, and Maintainability) function.

The Quality Assurance program at DDC is fully compliant with MIL-Q-9858A and MIL-STD-45662. DDC's Workmanship Standards Manual complies with MIL-E-5400, MIL-E-16400, MIL-STD-883C, MIL-STD-454, MIL-STD-275 and MIL-STD-1772 as well as the particular requirements of current DDC customers.

The Reliability Programs employed by DDC are based on the requirements of MIL-STD-785, MIL-STD-781, and MIL-HDBK-217. DDC's complete standard product line — tried and proven components — can be presented in a Hi-Rel configuration and thus be integrated into a design for a Hi-Rel system. The Maintainability Programs employed by DDC are structured in accordance with the requirements of MIL-STD-470, MIL-STD-471, and MIL-HDBK-472. Both the maintainability and reliability functions are integrated with the design as well as manufacturing tasks to ensure a total system approach to product assurance.

MANUFACTURING

DDC's manufacturing capabilities are subdivided into the unique disciplines in which the company specializes. Approximately 20,000 square feet are dedicated to manufacture of discrete components, harnesses and assemblies, with an additional 25,000 square feet set aside in a clean, modern, environmentally-controlled, thick-film hybrid area. Each of these areas is managed by a different team of specialists, under the direction of a single Vice-President of Manufacturing. In addition, 4,000 square feet is dedicated to Material Control and Purchasing disciplines to assure an orderly flow of material into the production lines. The Material Control Department also services the engineering needs, but this is augmented by separate purchase and expediting functions resident within the Engineering Department to minimize the impact on an orderly and scheduled flow of standard and custom manufactured product.

Approximately 40 percent of DDC's employees are involved in discrete assembly, which has made DDC a leader in the field of military, high reliability data conversion modules, subsystems and systems. This well disciplined manufacturing arm avails itself of some of the most modern assembly techniques offered in the industry today. In addition to having been approved by most of America's leading aerospace companies as compliant to MIL-Q-9858A and their own stringent requirements, this facility is certified by the U.S. Navy as a SEM (Standard Electronic Module) facility. This U.S. Navy certification was granted in February of 1976 and has been maintained since.

DDC's modern, thick-film hybrid facility is among the most advanced existing anywhere today. It has been certified to high reliability standards by most aerospace and military customers in the U.S., as well as Europe, and is capable of manufacturing components for use in manned-space applications. It is a clean environment area, with carefully filtered air circulation system and limited access. All personnel working within or entering the thick-film area are required to wear protective covering to minimize contamination of the environment. The thick-film hybrid facility was certified by the U.S. Navy as a SEM facility at the same time as our discrete facility was SEM certified and similarly, retains its certification to this date. Approximately 20 percent of DDC's employees are involved in the thick-film operation which presently consumes approximately 20 percent of the available floor space. This is one of our most rapidly growing areas of involvement, and is presently in the process of being expanded. DDC is a leader in the design and manufacture of high quality complex hybrids.

In the area of hybrid assembly, DDC is one of the few companies that routinely designs and manufactures thick-film hybrids which contain both analog and digital circuitry within the same package. The complexities of the hybrids routinely manufactured by DDC is rarely, if ever, duplicated in production quantities anywhere in the U.S., and our equipment and machinery is of the highest caliber and quality and includes automatic laser trimming, wire bonding and testing.

SALES & MARKETING

DDC maintains a world-wide chain of representatives and direct sales staff to serve the needs of the data conversion community. Because of the advanced technological level of DDC products, most of this field organization consists of graduate engineers. The field staff has a full complement of literature and pricing for an extensive line of standard DDC products. The field organization is supported by an Applications Engineering Group at the Bohemia, NY factory which is capable of giving professional applications assistance and more detailed technical information.

DDC is frequently asked to modify its standard products to meet specific customer requirements for performance, quality and configuration control. Our factory Applications Engineering staff is prepared to take your individual requests and translate them into documentation for engineering design, product manufacturing, and quality assurance at DDC.

EQUIPMENT

Representative of some of the capital equipment possessed by DDC is a full hybrid production facility. This includes a multitude of both ultrasonic and thermocompression wire bonders, epoxy and eutectic die-attach equipment, and beam lead bonding capability. Machinery for these functions is of the most modern type available and is being upgraded and added to constantly.

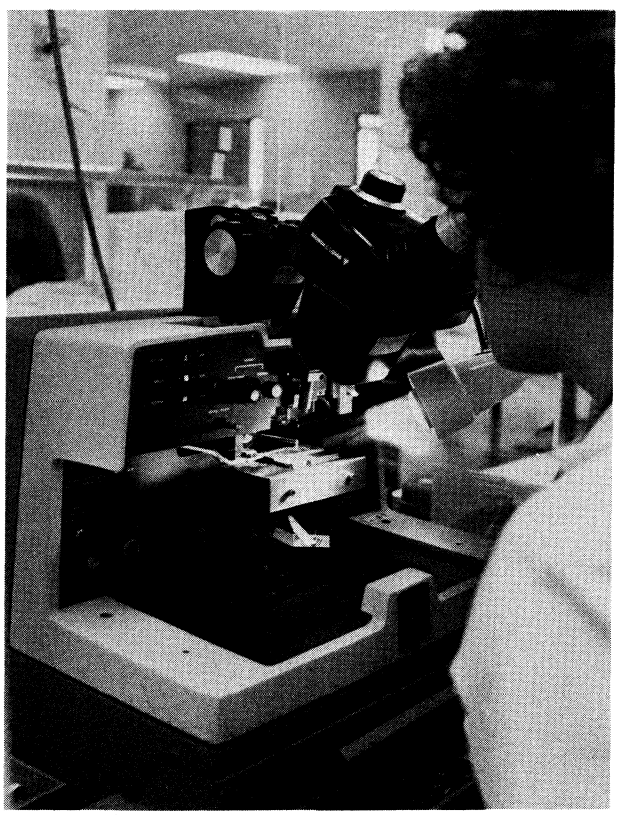
Multizone belt furnaces exist for the deposition and firing of conductive and resistive substrate materials, and we manufacture our own substrate screens. Each hybrid operator and hybrid inspector is provided with the latest type stereoscopic and/or zoom microscopes to assure the proper placement and performance of the hybrid component parts. In addition, our Quality Assurance Department possesses a unique lenseless microscope for inspection purposes, plus centrifuge, gross and fine leak testing, photographic examination, and PIND equipment.

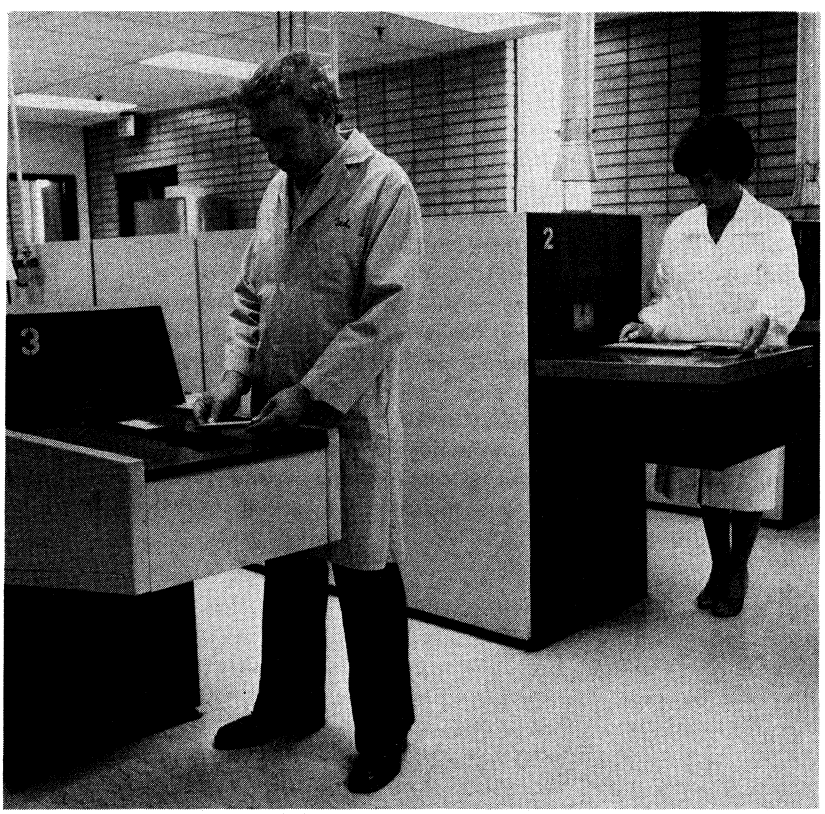
Our Engineering-Hybrid Model Shop contains a representative sampling of each of the above-mentioned pieces of equipment, so that prototype quantities are fabricated on equipment identical to that which is used in production. The only exception to this is in the area of the multizone belt furnaces. In this instance, the engineering substrates are produced on the actual manufacturing equipment.

Our testing facilities include the most modern digital voltmeters, oscilloscopes, signal generators, and other similar production and bench test equipment. Several automatic and semi-automatic computer test stations are in place and functional on a daily basis. These minicomputer controlled test consoles check individual components, subassemblies, and completely integrated systems. The Engineering Department has duplicates of manufacturing equipment, and all engineering evaluations and investigations are consistent with procedures used in actual manufacture.

Several temperature chambers are utilized for the burn in and temperature testing of finished product. A fully-equipped component test facility under the direction of our Quality Assurance Department exists for fully characterizing, testing and evaluating all incoming component parts prior to utilization in a DDC product. In addition to the most modern, semi-automatic, integrated circuit test equipment, a Lorlan computer-aided transistor and diode test machine is utilized for daily incoming inspection and grading purposes. Facilities to probe semiconductor chips exist in the Component Test area and all semiconductor chips are tested, either by probing or by mounting on test substrates and in test headers for full characterization testing and evaluation.

Although DDC has been in existence since 1963, a major portion of our machinery and equipment has been purchased since 1974 when the current building was occupied. The significance of this move on the Company caused us to relegate much of the equipment which existed prior to 1974 to back up or second tier status. New equipment was procured for prime utilization and additions have been made on a continuing basis to keep pace with our needs.





QUALITY EXCELLENCE

DDC was awarded, under the Contractor Assessment Program (CAP), the Department of Defense award for Quality Excellence. This award is based upon the DCASMA QAR evaluation of the DDC Quality System.

RIGID QUALITY STANDARDS

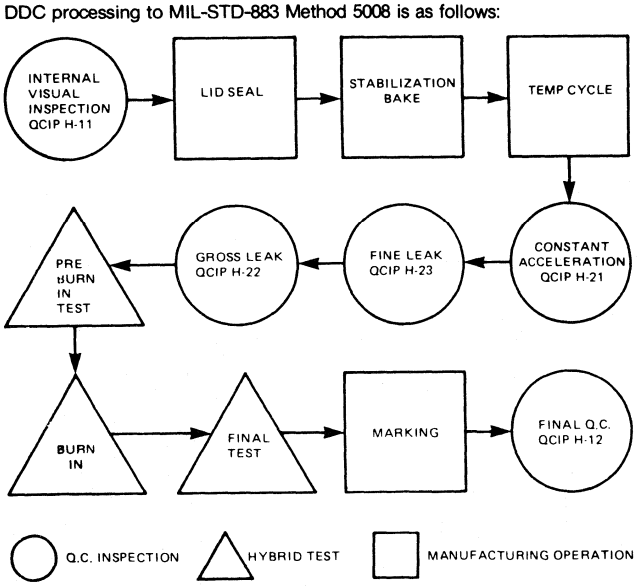
DDC designs and manufactures hybrid and discrete products for industrial, military, and space applications. To satisfy our customer's quality requirements, it takes more than engineering and manufacturing capability; it takes aggressive and skillful product assurance professionals offering advice and monitoring quality every step of the way. Our quality system complies with MIL-Q-9858A and the DDC Product Assurance Manual.

Our concern for quality starts at the proposal with a thorough review of specifications and drawings to establish detailed work instructions and Product Assurance Plans. These plans assure proper monitoring throughout all stages of design, fabrication and test.

In the hybrid manufacturing area, specifications MIL-M-38510 and MIL-STD-883 are used to establish workmanship standards. In the discrete manufacturing area, the standards are set in accordance with MIL-STD-454 and MIL-STD-275.

TYPICAL HYBRID PROCESSING

DDC processing to MIL-STD-883 Method 5008 is as follows:



MIL-STD-883 REQUIREMENT	DDC CONTROLLING PROCEDURES	TITLE	REMARKS
2017	QCIP H-11	Internal Visual	
None	Welded	Lid Seal	
1008		Stabilization Bake	DDC Procedure Condition C 24 hrs. @ +150° C.
1010	QCIP H-27	Temperature Cycling	Condition C 10 Cycles +25, —65, +25, +150° C.
2001	QCIP H-21	Constant Acceleration	5000g Condition A
1014	QCIP H-23	Fine Leak	883 Test Condition A
	QCIP H-22	Gross Leak	883 Test Condition C
1015		Burn In	DDC Procedure
2009	QCIP H-12	Final QC	External Visual

MIL-STD-883 PROCESSING FLOW CHART

The Product Assurance department evaluates incoming passive and active devices to verify their physical, electrical, and environmental characteristics. Equipment for these tests include the lastest in automatic test and inspection systems.

To enhance inspection of complex hybrids DDC has developed its own automatic inspection systems. Defects can be automatically recorded to greatly improve inspection reporting.

DDC maintains a product assurance evaluation laboratory to evaluate incoming materials, investigate manufacturing problems, support engineering studies and perform detailed failure analysis. The laboratory is staffed with Quality Assurance professionals and is equipped with the following state-of-the-art equipment:

Scanning Electron Microscope (SEM). With the SEM, DDC engineers can examine surface structures up to 200,000 times magnification.

Energy Dispersive X-Ray Spectrometer (EDAX). With an EDAX attached to the SEM, we can identify chemical elements, some of which may cause reliability problems within the hybrid. The EDAX is especially valuable for incoming inspection and failure analysis studies.

TEST METHODS FOR DISCRETE MODULES

Discrete modules will meet the specific test methods and conditions of MIL-STD-202 shown unless alternative methods are specified by the customer in his procurement documentation.

METHOD	CONDITION	COMMENT
204	C	10G, 2000 Hz vibration
213	A	50G, 11ms shock
106*	—	Moisture
107	A	Thermal shock
101	B	Salt spray
105	B	50,000 ft. altitude

*when conformally coated on P.C. board

MIL-STD-202 TEST METHODS

PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc.

It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a pin connection by ripping out the plated through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.

SECTION A

A/D CONVERTERS

SUMMARY TABLE

Name	Form Factor	Resolution	Linearity Error (Max)	Conversion Time	Features	Page
ADC-4450	2 x 2 x 0.4" Discrete module	12 bits	±0.012% F.S.R.	1.5 μs	Low cost, high speed, frequency domain A/D	13
ADC-00401	32 pin triple DIP hybrid	12 bits	±0.012% F.S.R.	2.0 μs	High speed pin for pin replacement for ADC85 units. Low cost.	17
ADC-00403 and ADC-00404	32 pin DDIP Hermetic hybrid	12 bits	+0.012% F.S.R.	2.0 μs	High speed pin for pin replacement for ADC85 units. Military applications	23
ADH-8516	36 pin DDIP hybrid	12 bits	±0.012% F.S.R. ±0.024% F.S.R.	2.0 μs	High speed 3-state outputs	29
DDC ADC87	32 pin triple DIP hybrid	12 bits	±0.0125% F.S.R.	10 μs	−55°C to +125°C operation. Pin for pin replaces ADC85	30
DDC 5101	24 pin DDIP hybrid	8 bits	±0.195% F.S.R.	900 ns	Form-fit-function replacement for MN 5101 A/D	36
DDC-5200 SERIES	24 pin DDIP Ceramic hybrid	12 bits	±0.012% F.S.R.	50 μs	Pin for pin replaces MN5200 Series	40
DDC 5210 SERIES	24 pin DDIP hybrid	12 bits	±0.012% F.S.R.	13 μs	Form-fit-function replacement for MN 5210 series A/D.	44
DDC-5240	32 pin triple DIP hybrid	12 bits	±0.0125% F.S.R.	5 μs	High speed pin for pin replacement for ADC85	48

BACKGROUND INFORMATION

INTRODUCTION

In A/D converters, DDC has focused on high performance products based on the most recent advances in component technology and circuit design. Most converters are self-contained with internal clocking and reference, and require no external components except for optional offset and gain trimming. Pin programmable features include different input voltage ranges, unipolar or bipolar coding, and 3-state outputs.

THE SUCCESSIVE APPROXIMATION METHOD

An A/D converter using the successive approximation method contains an internal D/A converter. The digital input bits in the D/A converter are tried in succession until the D/A output is equal to the external analog input signal. The D/A digital input will then represent the digitized external signal.

All successive approximation converters are based on the closed loop technique shown in Figure 1. An internal successive approximation register (SAR) produces a digital output which activates the bits in the internal D/A converter. A clock and control logic circuit operates the register according to a comparator signal which detects the difference between the analog input and the output of the internal D/A. A conversion is initiated by an externally supplied pulse which starts the sequence. All bits except the MSB are initially turned off. The control logic then sets one bit at a time in the register, setting each bit high or low according to the comparator output. The most significant bit (bit 1, the MSB) is first set to logic 1, and the precision D/A produces a current equal to 1/2 full scale. This current I_{OUT} is compared to the current I_{IN} created by the input voltage V_{IN} at the summing junction. If the I_{OUT} is less than I_{IN}, the comparator tells the SAR to leave the first bit at logic 1 and, as the clock continues, bit 2 is set at logic 1. If I_{OUT} is greater than I_{IN}, the first bit is reset to logic 0 before trying bit 2.

Any succeeding bit that does not cause the combined bit currents to exceed the input current remains set at a logic 1, and any bit that causes the combined bit currents to exceed the input current is reset to a logic 0. After the LSB has been tried, the SAR transmits a Conversion Complete (CC) signal. The output of the SAR at this time is a digital number representing the analog input as a fraction of the internal reference voltage. The accuracy of the digital output will be proportional to the accuracy of the reference and internal D/A, and the highest accuracy attainable will be ±1/2 LSB.

THE TWO STEP METHOD

The speed of a successive approximation converter is limited by the need to wait for each bit to settle for each trial. At the cost of increased complexity, it is possible to use a two step technique, which can achieve more than twice the speed. In a two-step process, the bits are tried in two groups, called the coarse bits and the fine bits. Each group of bits is tried with its own A/D converter, and each A/D requires less resolution (fewer bits). A two step conversion process is faster than single stage conversion not only because a new conversion can be initiated while the fine bits are being tried, but also because the settling times for each bit are reduced when a A/D requires less accuracy.

Figure 2 shows how the two step technique can be implemented. The analog input is sampled by the track/hold amplifier and held for the first part of the conversion cycle. The coarse bits A/D converter digitizes the most significant bits at a relatively fast rate and the coarse bits are stored in the digital combiner. The analog voltage corresponding to the coarse bits which is formed by the D/A converter is subtracted from the analog input signal being held by the input track/hold amplifier. Correction circuits are usually required at the differencing junction to compensate for non-linearities in the A/D and D/A, track/hold errors, and temperature drifts. With a PROM these errors, which are highly repeatable, can be uniquely corrected for each converter.

As soon as the summed voltage from the differencing junction has been acquired by the fine bits track/hold amplifier, the input track/hold can acquire a fresh analog input voltage to commence a new conversion cycle. Meanwhile, the fine bits A/D digitizes the fine bits and the digital combiner accepts them to complete the first conversion cycle. The entire two-step conversion cycle is regulated by a clock with control logic, and a Start Conversion pulse initiates each conversion. An important advantage of two step conversion is that the ultimate accuracy of conversion is determined by the accuracy of the subtraction process, which involves the D/A and track and hold amplifier. These circuits need to settle only once during each conversion cycle. The internal coarse and fine bit A/D's may be successive approximation or flash converters.

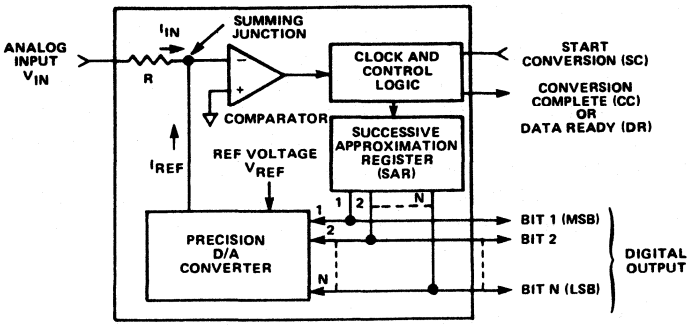


FIGURE 1. SUCCESSIVE APPROXIMATION A/D CONVERSION

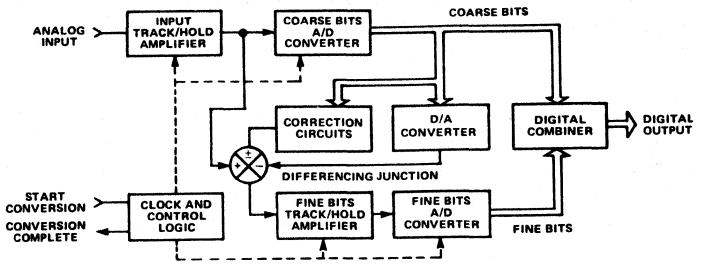


FIGURE 2. TWO-STEP A/D CONVERSION

THE FLASH QUANTIZATION METHOD

The flash quantization method which is illustrated in Figure 3 is the most rapid A/D conversion technique. A string of comparators is used to compare the analog input voltage directly with voltage steps on a resistance ladder. In Figure 3, for instance, if the analog input voltage lies between $3/8V_R$ and $4/8V_R$, the lower three comparators would respond and the upper four would not. The decoding logic translates the comparator responses into appropriately coded digital output.

Flash quantization is rapid because signals propagate very quickly through the parallel-connected comparators and the decoding logic. In constrast, the throughput delay in a successive approximation converter with n bits includes n D/A settling times and n comparator response times. On the other hand, the complexity of a flash quantization converter can be greater because the number of comparators required and the complexity of the decoding logic depends on the number of bits. A resolution of n bits will require 2^n resistors and 2^n-1 comparators. The three bit converter shown in Figure 3 requires $2^3=8$ resistors and $2^3-1=7$ comparators. A converter with 6 bit resolution requires $2^6 = 64$ resistors and $2^6 - 1 = 63$ comparators.

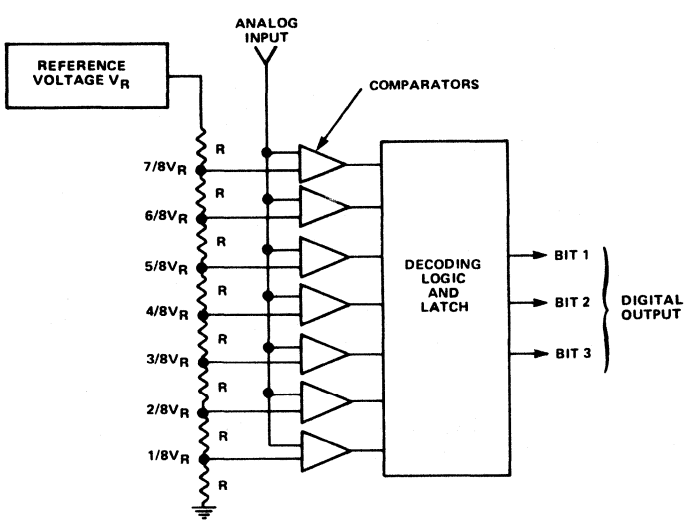


FIGURE 3. 3-BIT FLASH CONVERSION

A/D TRANSFER CHARACTERISTICS AND ACCURACY

The output of an A/D converter is inherently quantized and ideally any input analog value within ±1/2 LSB of the digital code to which it corresponds should give the same digital output. This results in the ideal transfer characteristic shown in Figure 4 for a 3 bit A/D converter with unipolar straight binary or bipolar offset binary coding. In Figure 4, for example, the 100 code output corresponds to all analog input values within ±1/2 LSB of the analog value in the center of the range.

It can be seen from Figure 4 that a transfer function described by transition values does not cover a full range of analog input values extending from 0 to F.S. or from −F.S. to +F.S. In Figure 4, for instance, the unipolar analog input extends from 0 to +F.S. − 1/2 LSB, and the code for +F.S. is not defined. For some converters, the analog scale is offset by 1 LSB in order to give +F.S. a code value. The code for the opposite end of the scale (0 to −F.S.) will then be undefined. This is most often done with complementary coding, in which logic 1 and logic 0 values are interchanged, so F.S. can correspond to a 000. . .code.

The accuracy of an A/D converter is measured by determining the analog input values corresponding to 50% dither between adjacent digital codes. Ideally, as shown in Figure 4, the transition points will occur midway between LSB values, at points such as 1/2 LSB, 3/2 LSB, 5/2 LSB, etc.. The transition table for a 3 bit converter in Figure 5 is equivalent to the transfer characteristic in Figure 4.

The total error in a converter is the sum of the offset error, the gain error and the linearity error. For a unipolar A/D, the offset error is usually specified for the transition corresponding to ±1/2 LSB, but can be assigned by the manufacturer to be at either end of the analog input range. For a bipolar A/D, the offset error could also be assigned to be at the transition close to the center of the range where the analog input is ±1/2 LSB. At whatever point offset is designated, the offset error will be the difference between the measured value for 50% dither and the theoretical analog value for that point.

The gain error is measured at the transition points at the opposite ends of the range. The gain is equal to the difference between the measured inputs at the two transition points (keeping negative signs for negative inputs), divided by the theoretical input

span between them. For the 3 bit converter described above, the input span is F.S. – 2 LSB for straight binary coding, and 2 F.S. – 2 LSB for offset binary coding.

Linearity measurements must be corrected for both offset and gain errors. The analog input is measured for 50% dither at each transition point. The linearity error at each point is the difference between the theoretical value and the measured value after the measured value has been corrected by first substracting the offset error and then multiplying by the gain correction. An alternative procedure, which simplifies calculations is to trim the offset error and then multiply by the gain correction.

Monotonicity is usually also an important requirement. If the converter is monotonic, the digital code will never decrease when the analog input is increased, and will never increase as the input is decreased. All DDC converters are monotonic.

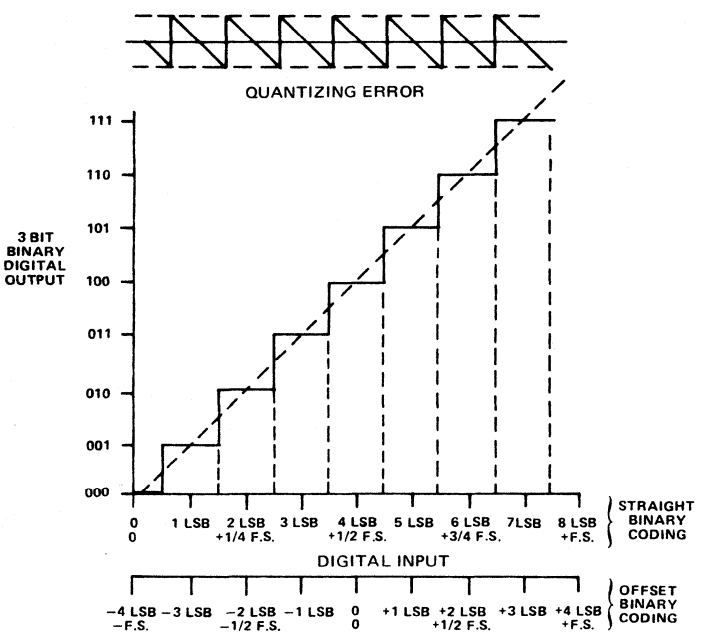


FIGURE 4. IDEAL TRANSFER CHARACTERISTIC FOR A 3-BIT A/D CONVERTER

ANALOG INPUT		BIT TRANSITION		
UNIPOLAR STRAIGHT BINARY	BIPOLAR OFFSET BINARY	(MSB) BIT 1	BIT 2	(LSB) BIT 3
+F.S. – 3/2 LSB	+F.S. – 3/2 LSB	1 1	1 1	0 1
+3/4 F.S. – 1/2 LSB	+1/2 F.S. – 1 LSB	1 1	0 1	1 0
+1/2 F.S. + 1/2 LSB	+1/2 LSB	1 1	0 0	0 1
+1/2 F.S. – 1/2 LSB	–1/2 LSB	0 1	1 0	1 0
+1/4 F.S. + 1/2 LSB	–1/2 F.S. + 1/2 LSB	0 0	1 1	0 1
+3/2 LSB	–F.S. + 3/2 LSB	0 0	0 1	1 0
+1/2 LSB	–F.S. + 1/2 LSB	0 0	0 0	0 1

FIGURE 5. THEORETICAL TRANSITION VALUES FOR 3 BIT A/D CONVERTER

PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc.

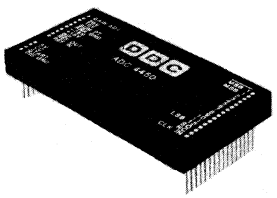
It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a pin connection by ripping out the plated through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.

APPLICATION NOTES

The following application notes are available upon request:

- o A DESIGNER'S GUIDE TO DEGLITCHING DACS
- o SIMPLIFY THE UP INTERFACE TO YOUR 12-BIT A/D CONVERTER
- o GETTING THE BEST FROM A/D CONVERTERS
- o MEND FLASH-CONVERTER FLAWS WITH A TRACK-HOLD CURE
- o MEET THE DEGLITCHER
- o D/A GLITCH CAUSES ABOUND BUT SOLUTIONS ARE RARE
- o OPTIMIZING D/A CONVERTER PERFORMANCE
- o ACHIEVE HIGH SPEED DATA ACQUISITION WITH A FAST ADC & DMA
- o CHANGE POLAR TO RECTANGULAR WITH MULTIPLYING D/A UNITS

ADC-4450 SERIES



LOW COST, HIGH SPEED FREQUENCY DOMAIN A/D CONVERTER

DESCRIPTION AND APPLICATIONS

The ADC-4450 Series is a high performance analog to digital converter, designed for spectrum analysis, fast fourier transform devices and other frequency domain applications. Its high speed and low price make it ideal for use in multiplexed data acquisition systems, vibration modal analysis, sonar or radar signal digitizing and nuclear instrumentation. Configured for an external clock input as the ADC-4450, an optional device, ADC-4452, is available with an internal clock and clock output.

FEATURES

- *12 BITS: 600 kHz (1.5 μs)*
- *–72 dB TOTAL HARMONIC DISTORTION*
- *–72 dB INTERMODULATION DISTORTION*
- *.0125% F.S.R. LINEARITY*
- *SERIAL AND PARALLEL OUTPUT*
- *SHORT CYCLING*

SPECIFICATIONS (at + 25°C unless otherwise noted)

PARAMETER	UNIT	VALUE
RESOLUTION	**bits**	**12**
ACCURACY AND DYNAMICS		
Total Harmonic Distortion* (2, 3)	dB	–72
Intermodulation Distortion* (2, 4)	dB	–72
Linearity	LSB	±1/2
Linearity and Differential Linearity Tempco	ppm FSR/°C	1
Differential Non-linearity*		
ADC-4450		
Less than 6 MHz clock freq	LSB	± 1/2 typ, ± 1 max (no missing codes)
6 to 6.7 MHz clock freq	LSB	± 1/2 typ, ± 1.5 max (6 missing codes)
6.7 to 8.0 MHz clock freq	LSB	± 1/2 typ, ± 2 max (12 missing codes)
ADC-4452	LSB	± 1/2 typ, ± 1.5 max (4 missing codes)
Gain Error	%	±2
Gain Tempco	ppm FSR/°C	25
Offset Error	mV	±100
Offset Tempco	ppm FSR/°C	10
Word Rate	kHz	600 max (1.5 μs conversion time)
ANALOG INPUT RANGES		
Voltages	V	±10, 0 to +20 ±5, 0 to +10 ±2.5, 0 to +5
Impedance	Ω	2500 1250 625
Gain Adjust Impedance	Ω	400 k
Reference		
Internal Reference Drive Capability	mA	±0.5 max (not buffered)
External Reference (User Supplied to REF IN)		
Input Range	V	+6.3, ±2%
Current	mA	4.5 typ
Input Impedance	KΩ	1.4 typ
DIGITAL INPUT/OUTPUT		
Logic		
Input	TTL	1 std load
Output	TTL	4 std load
Code		Complementary Binary, Complementary Offset Binary and Complementary Two's Complement (using MSB)
THERMAL CHARACTERISTICS		
Temperature Range		
Operating	°C	0 to +70
Storage	°C	–55 to +125
POWER SUPPLY CHARACTERISTICS (Worst Case)		ADC-4450 Series: +5 ±10% / +15 ±5% / –15 ±5%
Voltage/Regulation	V	
Current	mA	140 typ / 25 typ / 40 typ
	mA	190 max / 35 max / 60 max
PHYSICAL CHARACTERISTICS		
Size	in	2 x 4 x 0.40 (51 x 102 x 10.2 mm)
Weight	oz	5 (141.8 g)

*NOTES:
1. for +1/2 LSB linearity.
2. +1 LSB max at 6MHz; +1.5 LSB max at 6 to 6.7MHz; 2 LSB max at 6.7 to 8 MHz.
3. Total harmonic distortion measured with a one-tone test (100kHz) at a word rate of 256 kHz.
4. Intermodulation distortion measured with a two-tone test (100kHz) Hz and (105kHz) Hz at a word rate of 256 kHz.

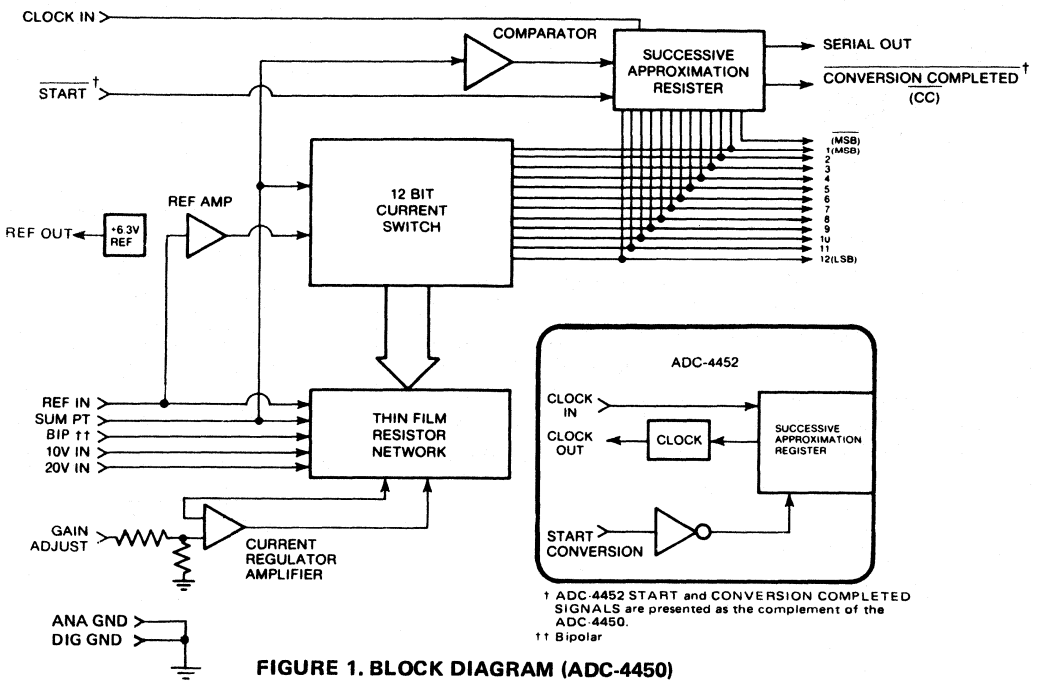


FIGURE 1. BLOCK DIAGRAM (ADC-4450)

TECHNICAL INFORMATION

The ADC-4450 Series Frequency Domain, Analog to Digital converters are successive approximation devices, capable of operating with six unipolar and bipolar input ranges (see specifications). Digital output codes include: Complementary Offset Binary; Complementary Binary and Complementary Two's Complement, when using $\overline{\text{MSB}}$ (see Figure 1.) Output data is available in 12 bit parallel and serial formats, and has drive capability of 5 TTL loads.

In certain applications the converters may require offset and gain adjustments. The procedure, set forth in Figure 2., is to be used to make the necessary adjustments for unipolar and bipolar input configurations (Complementary Offset Binary codes shown).

OFFSET AND GAIN ADJUSTMENTS

Offset Adjustment

(Unipolar Configurations)

1. Set the input level to zero.
2. Adjust the potentiometer of the offset circuit (Figure 2.) to achieve 50% dither between digital output code 111----10 and 111----11.

(Bipolar Configurations)

1. Set the input level to equivalent minus Full Scale plus 1 LSB.
2. Adjust the potentiometer to achieve 50% dither between digital output codes 111---10 and 111---11.

Gain Adjustment

Gain adjustments are made for both input configurations with input levels set to plus Full Scale minus 1 LSB. Adjustment of the potentiometer in the Gain circuit (Figure 2.) must achieve a 50% dither between digital output codes 000---00 and 000---01.

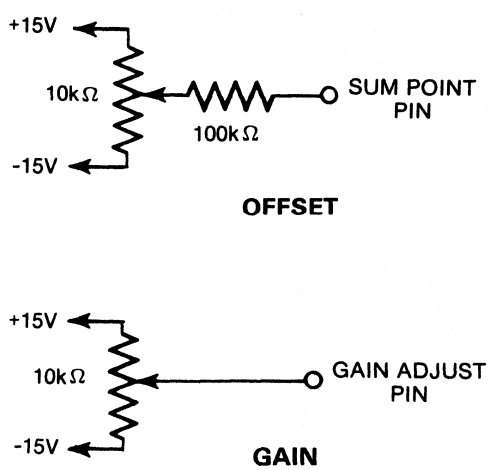
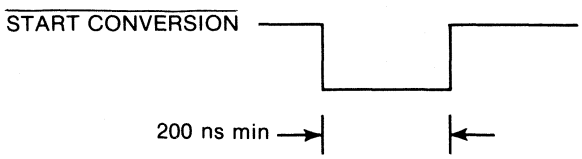


FIGURE 2. OFFSET AND GAIN CIRCUITS

The ADC-4450 Series converters may be operated synchronously or asynchronously, with respect to Start Conversion input signal timing.

The Start Conversion pulse must be 200 ns (1.5 Clock Pulses min), when operating in an asynchronous mode, at a 7.5 MHz clock rate (Figure 3). Synchronous conversions are started on the "0" level of a negative 50 ns (min) Start Conversion pulse, applied to the START pin (ADC-4452 requires a positive pulse). The Start Conversion pulse specifications supplied in Figure 3. are intended to insure sufficient time to reset internal logic, while the START line is low. Start must be low during at least one low to high clock transition. Allowing START to go high, after the reset period, will begin the conversion on the next low to high clock transition. A converter busy signal is provided on the CC pin. Logic "1" indicates that a conversion is in progress (Logic "0" indicates data available). The ADC-4452 Conversion Completed (CC) is presented as the complement of the ADC-4450 output signal (see Figure 1 †). Transfer of data may occur 20 ns (typ) after the trailing edge of the Converter Complete signal.

ASYNCHRONOUS OPERATION



SYNCHRONOUS OPERATION

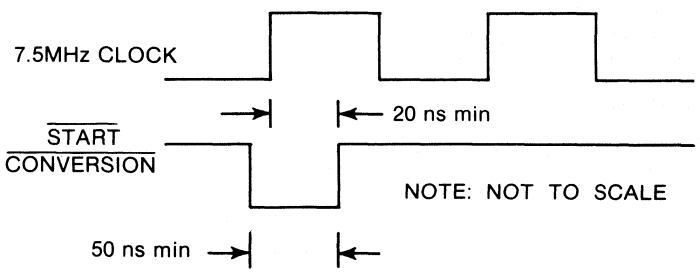
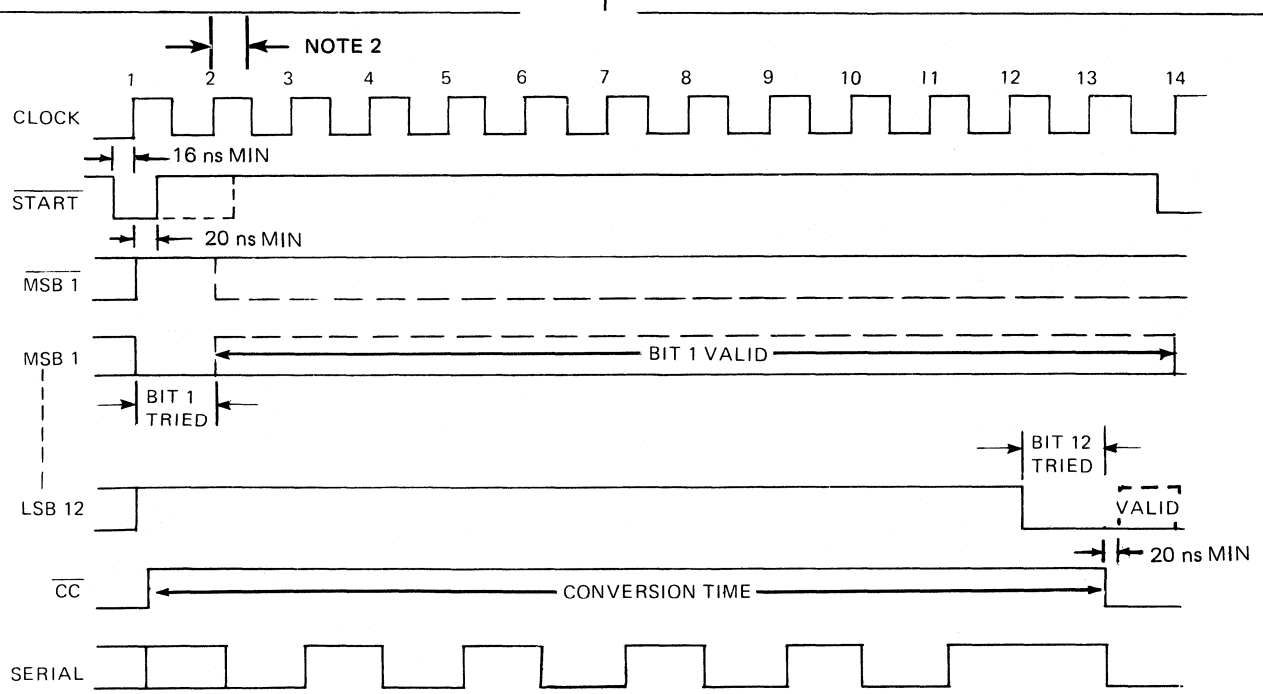


FIGURE 3. START PULSE TIMING

CONVERTER TIMING

All timing specifications are based on 7.5 MHz clock (guaranteed accuracy). Operation at 10 MHz clock will typically yield 10 bit linearity performance.

ADC-4450 series units reset internal logic on the first low to high clock transition after START CONVERSION goes low. Conversion begins on the first low to high transition after START CONVERSION is allowed to go high (see Figure 4). The converter will remain in a reset mode as long as START CONVERSION is held low.



NOTES: (1) ADC-4452 START and CONVERSION COMPLETED signals are complementary to the ADC-4450.
(2) 15% to 30% POSITIVE DUTY CYCLE yields OPTIMUM LINEARITY.

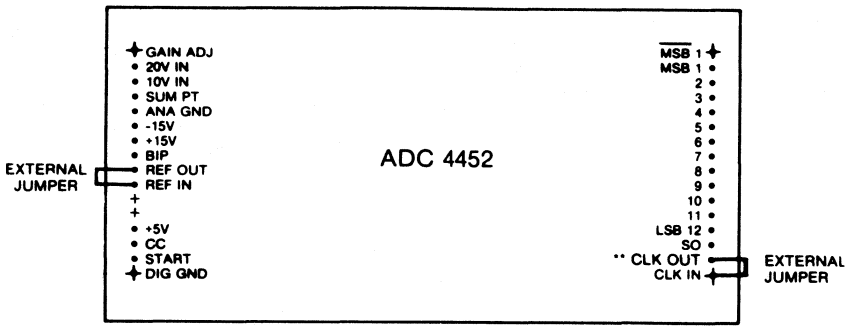
FIGURE 4. CONVERTER TIMING (ADC-4450)

INTERNAL REFERENCE CONNECTION

To operate the ADC-4450 Series converters with their internal reference, an external jumper must be connected between the REF IN and REF OUT pins (Figure 5). If an external reference is to be used it must be +6.3V ±2%, with output current of 4.5 mA.

INTERNAL CLOCK CONNECTION

To operate the internal clock designed into the ADC-4452, an external jumper must be connected between CLK IN and CLK OUT. This configuration provides clock output, with drive capability of 2 TTL loads.



**4452 ONLY.
†Analog and digital grounds are tied together internally.

FIGURE 5. INTERNAL CLOCK AND REFERENCE CONNECTIONS

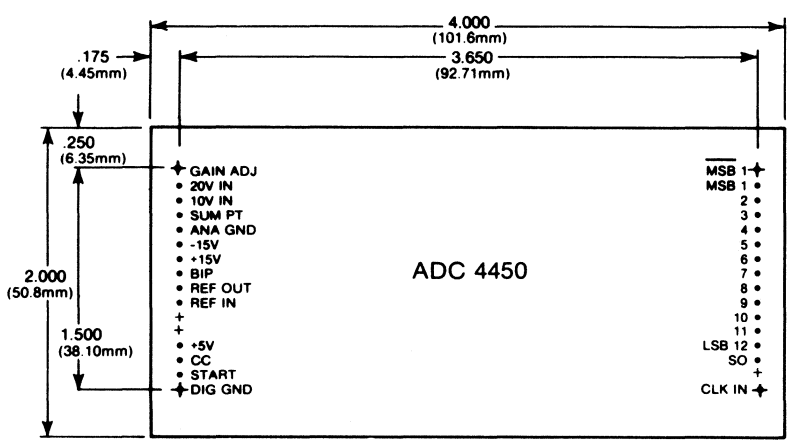
INPUT CONFIGURATION

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT IMPEDANCE (ohms)	INPUT TERMINAL	JUMPER CONNECTIONS
±2.5V	±3.75V	0.625k	10V IN	BIP—SUM PT. 20V IN—SUM PT.
0 to 5V	+7.5V	0.625k	10 V IN	BIP—ANALOG GND. 20V IN—SUM PT.
±5.0V	±7.5V	1.25k	20V IN	BIP—SUM PT.—10V IN.
0 to 10V	+15V	1.25k	20V IN	BIP—ANALOG GND. 10V IN—SUM PT.
±10.0V	±15V	2.5k	20V IN	BIP—SUM PT.
0 to 20V	+30V	2.5k	20V IN	BIP—ANALOG GND.

ORDERING INFORMATION

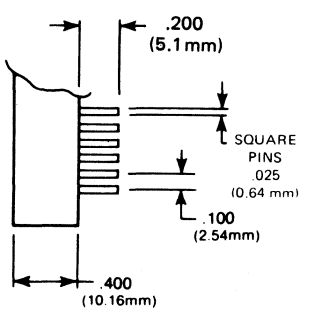
ADC - 4450 - 12

- 12 — Linearity Grade
  - —12=0.0125% FSR
  - —10=0.05% FSR
- 4450 — Model Family
  - 4450=Without Clock
  - 4452=With Internal Clock



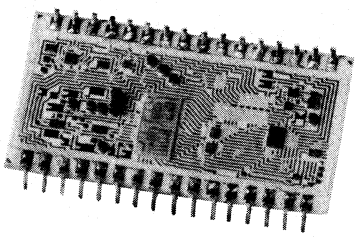
TOP VIEW

NOTE: Dimensions in inches and (milimeters)



If mating connector is required, user must supply: AMP P/N 87334-6 or suitable replacement.

12 BIT 2 μSEC HYBRID A/D CONVERTER
Low cost, high speed,standard pin out



FEATURES

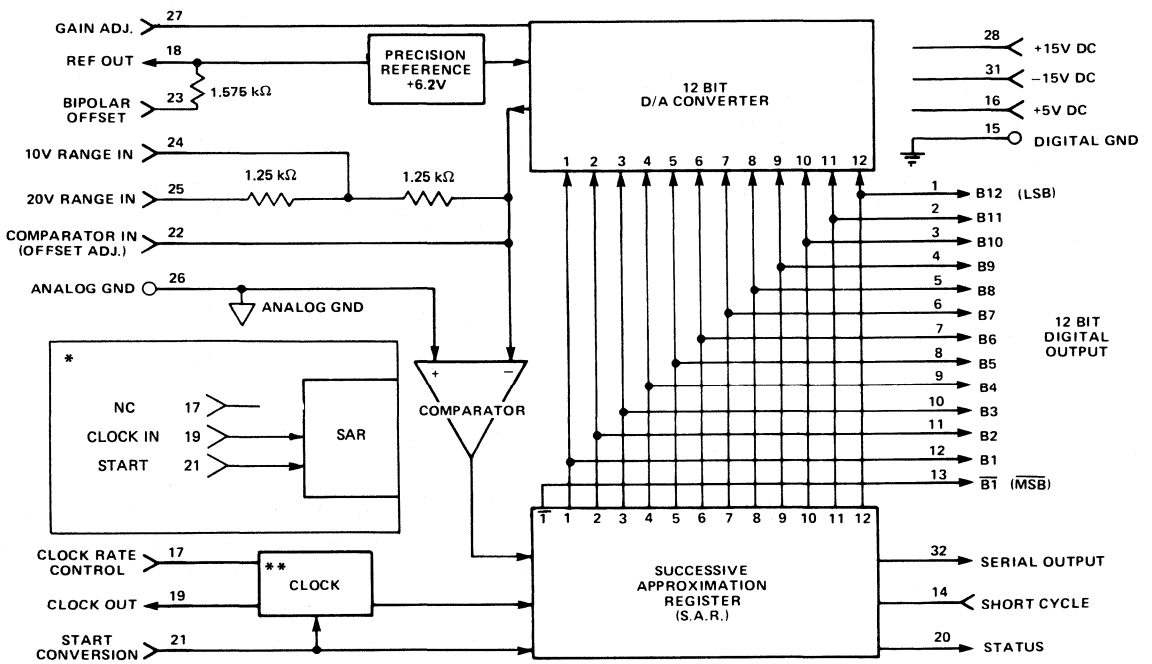
- *2 μSEC CONVERSION TIME*
- *12 BIT RESOLUTION AND LINEARITY*
- *LOW COST*
- *HIGHER SPEED PIN FOR PIN REPLACEMENT FOR ADC85 TYPES (NO BUFFER)*
- *32 PIN TDIP HYBRID PACKAGE*

DESCRIPTION

The ADC-00401 is a 12 bit 2 microsecond hybrid A/D converter packaged in a 32 pin TDIP. It offers a low cost higher speed pin for pin replacement for ADC87 and ADC85 types. Offered in models with internal or external clock, the ADC-00401 also features precision internal reference, 6 pin programmable input voltage ranges, and both serial and parallel data output.

APPLICATIONS

With its low cost, high speed and small package, the ADC-00401 is ideal for most commercial and industrial data conversion applications. Typical of these applications are vibration and FFT analysis, sonar and radar digitizing, medical and nuclear instrumentation, and multiplexed data acquisition systems.



*Function for external clock model only.
**Function for internal clock model only.

FIGURE 1. ADC-00401 BLOCK DIAGRAM

SPECIFICATIONS

Typical values at + 25°C case temperature and nominal power supply voltages

PARAMETER	UNITS	VALUES 10 BIT LIN	VALUES 12 BIT LIN
RESOLUTION	Bits	12	12
ACCURACY AND DYNAMICS			
Linearity Error	% of F.S.R.	±0.048 max	±0.012 max
Linearity Error Tempco	ppm/°C	±5 max	±2 max
Gain Error (Trimmable to zero)	% of F.S.R.	±0.1	±0.1
Gain Error Tempco	ppm/°C	±25	±15
Offset (Trimmable to zero)			
Unipolar	% of F.S.R.	±0.05 typ	±0.05 typ
Bipolar	% of F.S.R.	±0.1 typ	±0.1 typ
Offset Tempco			
Unipolar	ppm/°C	±3 max	±3 max
Bipolar	ppm/°C	±10 max	±7 max
Diff. Linearity Error	LSB	±1	±1
Conversion Time*	μs	1.5 max	2.0 max
Cycle Time*	μs	1.7 max	2.2 max
* The internal clock frequency is controlled by the applied Clock Rate Control voltage. See figure 4.			
ANALOG INPUTS			
Input Ranges			
Unipolar	V	0 to +5; 0 to +10; 0 to +20	
Bipolar	V	±2.5; ±5; ±10	
Max Voltage Without Damage	V	See figure 6.	
Impedance			
0 to +5V and ±2.5V	KΩ	0.625	
0 to 10V and ±5V	KΩ	1.25	
±10V	KΩ	2.50	
DIGITAL INPUTS			
Start Convert	nsec	50 min positive pulse. Trailing edge initiates conversion	
Loading	TTL loads	1	
DIGITAL OUTPUTS			
Parallel Data		Bit 1 through Bit 12 plus $\overline{\text{MSB}}$	
Drive	TTL loads	5	
Unipolar Coding		Complementary binary	
Bipolar Coding		Complementary offset binary or Complementary two's complement	
Serial Data		Non return to zero (NRZ)	
Drive	TTL loads	5	
Coding		Same as parallel data	
Status		Logic "1" during conversion. Logic "0" indicates valid parallel data.	
Drive	TTL loads	2	
Clock		13 positive pulses	
Period*	nsec	166 min	
Drive	TTL loads	2	
INTERNAL REFERENCE			
Voltage Output	V	+6.2 ±5%	
Current Output	mA	5 max for no degradation of specifications	
Voltage Tempco	ppm/°C	±20 max	
POWER SUPPLIES			
Voltages	V	+15 ±5% / −15 ±5% / +5 ±5%	
Max Voltage Without Damage	V	+18 / −18 / +7	
Current (Including Internal Clock)	mA	40 typ, 50 max / 65 typ, 80 max / 165 typ, 220 max	
Sensitivity	%FSR/%PS	±0.002 / ±0.002 / ±0.002	
TEMPERATURE RANGE			
Operating			
−3 Option	°C	0 to +70	
Storage	°C	−65 to +135	
PACKAGE			
Type		Ceramic case 32 pin TDIP	
Size	Inch (mm)	1.75 x 1.06 x 0.2 (44.5 x 27.0 x 5.1)	
Weight	Oz. (g)	0.67 (19)	

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a block diagram of the ADC-00401. Since the ADC-00401 is a successive approximation A/D converter, its main elements are a D/A Converter, a Comparator and a Successive Approximation Register. An internal Precision Reference and internal or external Clock, depending on model selected, complete the functional elements of the ADC-00401.

The successive approximation algorithm is initiated by a Start Conversion pulse input. This results in a change of the Status output signal, indicating that a conversion is in progress and output data is invalid. In a sequence starting with Bit 1, the D/A input is set to a "1" and the comparator detects whether the resulting D/A output is larger or smaller than the analog input signal. If the D/A output is larger than the analog input signal, Bit 1 is reset to "0". If not, then Bit 1 remains a "1". In succession, Bit 2 through Bit 12 are individually tested by the comparator. After 12 trials, and 13 clock pulse edges have occurred, the Successive Approximation Register (SAR) output is a digital representation of the analog input. At this time the Status output signal changes to indicate that conversion has been completed and output data is valid.

The ADC-00401 is available in both internal clock or external clock models. The internal clock model makes the clock signal available to the user on the Clock Output pin. In addition, the Clock Rate Control input pin may be used to make fine adjustments of the internal clock frequency. The ADC-00401 may be short cycled for less than 12 bit resolution with a resulting decrease in its conversion time.

Both parallel data and serial data are provided as digital outputs from the converter. For bipolar analog input signals the digital output data is coded in Complementary Two's Complement or Complementary Offset Binary. Both Bit 1 and Bit 1 complement ($\overline{\text{B1}}$) are provided as outputs, so either of these codes may be selected. For unipolar analog input signals, the digital output data is coded in Complementary Binary.

The ADC-00401 may be configured for any of six different input signal ranges by means of jumper wires between pins. Three bipolar and three unipolar ranges are implemented with combination of the two precision scaling resistors and the precision bipolar offset resistor. Inherent offset and gain errors of the A/D converter may be trimmed to zero with the addition of potentiometers.

The ADC-00401 contains an internal precision +6.2 volt reference. This reference voltage is provided for the user at an output pin. In order to avoid affecting converter performance, care must be taken not to load the reference beyond its output current capability.

To achieve the optimum performance available from the ADC-00401, it is recommended that decoupling capacitors be used on the supply lines. In addition, high frequency layout considerations should be kept in mind when designing a printed circuit board to accommodate the A/D converter. This includes minimum conductor lengths on signals, and a low impedance ground plane where possible.

TIMING DIAGRAM

A diagram of ADC-00401 typical timing is shown in Figure 2. A conversion is initiated by the application of a positive (50 nsec min) pulse to the Start Convert pin and a delayed (25 nsec min) clock to the Clock In pin. The rising edge of the clock causes the status signal to change to a "1", indicating that a conversion is in progress and parallel output data is not valid. Also in response to the clock rising edge, the MSB of the Successive Approximation Register (SAR) is reset to "0" and all other bits are set to "1". During clock period 1, the MSB trial takes place, and the MSB bit weight is compared to the analog input. The rising edge of clock pulse 2 causes the decision of the MSB trial to be stored, and simultaneously initiates the Bit 2 trial. In a successive manner, the rising edge of clock pulses 3 through 13 cause the storage of decisions on Bit 2 through Bit 12. The rising edge of clock pulse 13 causes the status signal to change to a "0", since the SAR now contains the valid 12 bit representation of the analog input. Parallel output data is valid during the interval that status signal is a "0".

Serial Data is available as an output in non return to zero (NRZ) format. Data for each bit becomes valid on the rising edge of the clock pulse one number higher than the bit number, and remains valid for one clock period. Typically, Serial Data is shifted into an external 12 bit shift register, using the falling edges of the clock signal. The falling edge of clock pulse 13 would therefore shift Bit 12 into the register.

The mimimum clock period allowed for rated performance of the ADC-00401 is 166 nanoseconds. This applies to both internal clock and external clock models. For internal clock models, the conversion will be initiated by the first rising edge of the clock that follows the falling edge of the Start Convert signal. Conversion time is defined as the time during which the Status signal is a "1" and parallel output data is not valid. Cycle time, which is slightly longer than conversion time, is defined as the minimum time which must elapse between successive Start Convert pulses.

EXTERNAL CLOCK

The ADC-00401 is available in internal clock and external clock models. For external clock models the user must provide a clock signal to Clock Input (pin 19). Thirteen positive clock pulses are required to complete the conversion process. For rated A/D performance, the applied clock period must be 166 nanoseconds minimum. Figure 2 shows Clock In timing relationships. Best performance is achieved with a clock "high" duty cycle of between 12% and 33%. This sequence initiates conversions for both gated clock and continuous clock inputs. Care must be taken to comply with the minimum cycle time requirement between successive Start Convert pulses.

SHORT CYCLING AND CONTINUOUS CONVERSION

The ADC-00401 may be short cycled to fewer than 12 bits resolution, with a resulting decrease in conversion time. Figure 3 shows the required jumper connections and the resulting conversion times, with a 6 MHz clock, for 8 bit through 12 bit resolutions. For resolutions of less than 12 bits, it is possible to increase the clock frequency somewhat, since internal settling times are shorter. This may be accomplished by adjusting the Clock Rate Control voltage.

The ADC-00401 can be simply configured for continuous conversion operation when it is required. The falling edge of the Status (pin 20) signal is used to trigger a one shot. The one shot output, a 50 nsec minimum positive pulse, is connected to the Start Convert (pin 21) input to yield continuous conversion operation.

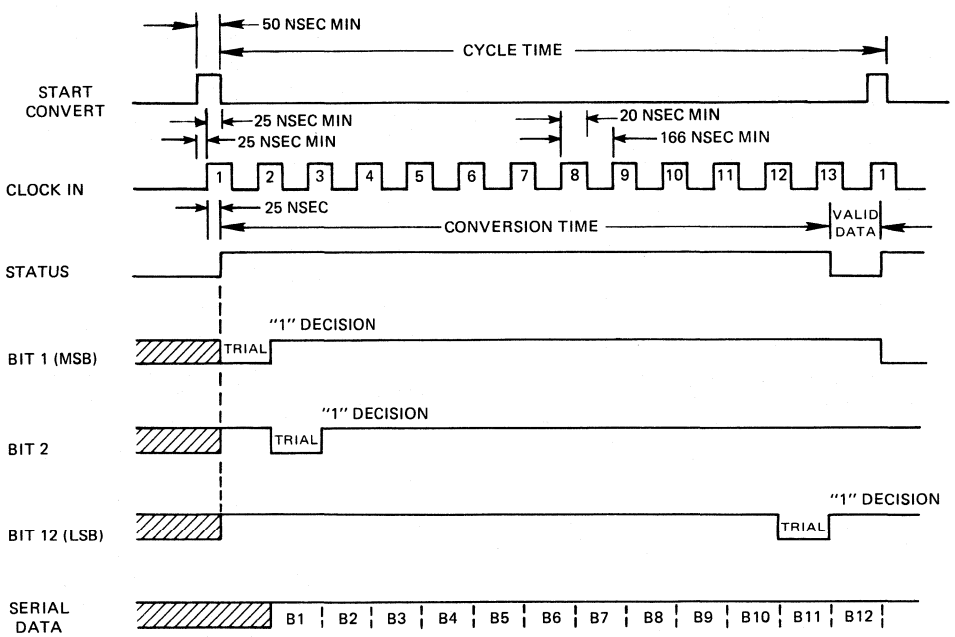


FIGURE 2. ADC-00401 TIMING DIAGRAM

CLOCK RATE CONTROL

The Clock Rate Control line is made available in the internal clock model of the ADC-00401 to make small adjustments of the internal clock frequency. Figure 4 shows a typical circuit using a potentiometer to generate the Clock Rate Control voltage, and the resulting clock frequencies. For 12 bit operation, care must be taken to comply with the 166 nanosecond minimum clock period requirement. For short cycled operation, the Clock Rate Control voltage may be set greater than 5 volts, resulting in a clock frequency greater than 8 MHz.

PARALLEL DATA

Bit 1 through Bit 12 plus $\overline{MSB}$ are the parallel output data lines provided by the ADC-00401. Each signal can drive a minimum of 5 standard TTL loads. Parallel output data is valid during the time that the Status signal is a "0". If a strobe signal is required to read the parallel data into a register a "one-shot" can be triggered by the falling edge of the Status signal, or the falling edge of clock pulse 13 can be isolated by gating the Clock and Status signals together.

SERIAL DATA

Serial Data is provided by the ADC-00401 in non return to zero (NRZ) format with the MSB first. The Serial Data output line can drive a minimum of 2 standard TTL loads.

Each bit becomes valid on the rising edge of the clock pulse one number higher than the bit number, and remains valid for one clock period. Typically an external 12 bit shift register is used to store the serial data, after it has been shifted into the register using the falling edges of the clock signal. The LSB would be shifted into the register by the falling edge of clock pulse 13.

OUTPUT CODING

The ADC-00401 provides Complementary Binary coded output data for unipolar analog inputs, and either Complementary Offset Binary or Complementary Two's Complement coded output data for bipolar analog inputs. Figure 5 illustrates the output data for various analog inputs for each of the three code figurations. For bipolar analog inputs, the 2 choices of output code are available since both MSB and $\overline{MSB}$ signals are provided as outputs.

ANALOG INPUT RANGES

The ADC-00401 may be configured for any of six different input signal ranges by means of jumper wires between pins. Three bipolar and three unipolar ranges are possible. Figure 6 shows these six choices of analog input range, along with the jumper connections required to implement each range. The chart also shows, for each input range, which pin is to be used for the input signal, and what impedance will be presented at that pin. Absolute maximum input voltage is also shown for each configuration.

OFFSET AND GAIN TRIMS

Gain and offset errors of the ADC-00401 are factory trimmed to be less than the values listed in the specification table. The converter is externally trimmable to zero gain and zero offset error, providing the user with flexibility for applications requiring maximum performance.

Figure 7 illustrates the external trim potentiometer circuit connections required to adjust the gain and offset errors of the ADC-00401 to zero. Multi-turn trimpots, with temperature coefficient of less than 100 ppm/°C, are recommended for best performance.

If gain adjust pot is not used, connect Gain Adjust (pin 27) to Analog Gnd (pin 26) to minimize noise.

RESOLUTION	CONNECT PIN 14 TO	CONVERSION TIME
8 BIT	PIN 4	1.3 μsec
9 BIT	PIN 3	1.5 μsec
10 BIT	PIN 2	1.6 μsec
11 BIT	PIN 1	1.8 μsec
12 BIT	NC	2.0 μsec

FIGURE 3. SHORT CYCLE OPERATION

PIN 17 VOLTAGE	APPROXIMATE CLOCK RATE
+5V	8 MHz
0V	6 MHz

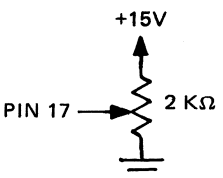


FIGURE 4. CLOCK RATE CONTROL

SCALE	BIPOLAR		UNIPOLAR
	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO'S COMPLEMENT	COMPLEMENTARY BINARY
+FS-1 LSB	0000 0000 0000	1000 0000 0000	0000 0000 0000
+3/4 FS	0001 1111 1111	1001 1111 1111	0011 1111 1111
+1/2 FS	0011 1111 1111	1011 1111 1111	0111 1111 1111
+1 LSB	0111 1111 1110	1111 1111 1110	1111 1111 1110
0	0111 1111 1111	1111 1111 1111	1111 1111 1111
− 1 LSB	1000 0000 0000	0000 0000 0000	
−1/2 FS	1100 0000 0000	0011 1111 1111	
−3/4 FS	1110 0000 0000	0001 1111 1111	
−FS	1111 1111 1111	0111 1111 1111	

FIGURE 5. OUTPUT CODING

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT IMPEDANCE (OHMS)	INPUT TERMINAL	JUMPER CONNECTION
±2.5V	±3.75V	0.625 K	PIN 24	PIN 23 TO PIN 22 PIN 25 TO PIN 22
0 to +5V	+7.5V	0.625 K	PIN 24	PIN 23 TO PIN 26 PIN 25 TO PIN 22
±5V	±7.5V	1.25K	PIN 24	PIN 23 TO PIN 22
0 to +10V	+15V	1.25 K	PIN 24	PIN 23 TO PIN 26
±10V	±15V	2.5K	PIN 25	PIN 23 TO PIN 22
0 to +20V	30V	2.5 K	PIN 25	PIN 23 TO PIN 26

FIGURE 6. ANALOG INPUT RANGE

INTERNAL REFERENCE

The ADC-00401 contains a +6.3 volt precision internal reference, which is made available for external use. A maximum output current of 5 mA will be provided by the internal reference, while maintaining rated performance. If this load is exceeded, gain and linearity error will increase. Damage will result from excessive loading.

LAYOUT PRECAUTIONS

To achieve the optimum performance of the ADC-00401, care must be taken in the printed circuit layout. Analog input lines and digital output lines should be separated from each other, and made as short as possible. To minimize ground noise, analog and digital grounds should be connected together in close proximity to the unit. A low impedance ground plane under the converter will yield the best results.

POWER SUPPLY DECOUPLING

Capacitive decoupling of all power supplies is required to minimize noise. Figure 8 shows the recommended power supply decoupling configuration. Tantalum or electrolytic capacitors of 1 μF or greater are used for low frequency decoupling. Ceramic capacitors of 0.01 μF or greater are used for high frequency decoupling. For best results, all capacitors should be placed as close to the unit as possible.

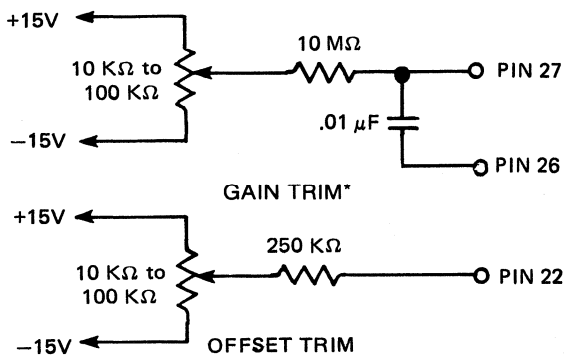
ACCURACY TESTING

Testing of the accuracy of the ADC-00401 consists of measurement of its gain, offset and linearity errors. Figure 9 shows a simple test circuit for making these measurements. A precision DC voltage source is used to provide the analog input signal, and the digital outputs are monitored by a string of light emitting diodes (LED).

The offset error can be measured by adjusting the DC voltage source until the LEDs indicate the zero code transition. The difference between the voltage input and zero volts is the offset error. After the offset error has been measured, the circuit shown in Figure 7 should be used to trim the offset error to zero.

With the offset error trimmed to zero, the gain error can be measured by adjusting the DC voltage source until the LEDs indicate the full scale code transition. The difference between the input voltage and the theoretical full scale input is the gain error. After the gain error has been measured, the circuit shown in Figure 7 should be used to trim the gain error to zero.

With the offset and gain errors trimmed to zero, any remaining error is a linearity error. Linearity error should be measured at the code transitions corresponding to each individual bit weight, and also at each of the major carry code transitions which occur at one count less than the individual bit weights.



*If gain trim is not used, connect pin 27 to pin 26.

FIGURE 7. OFFSET AND GAIN TRIM

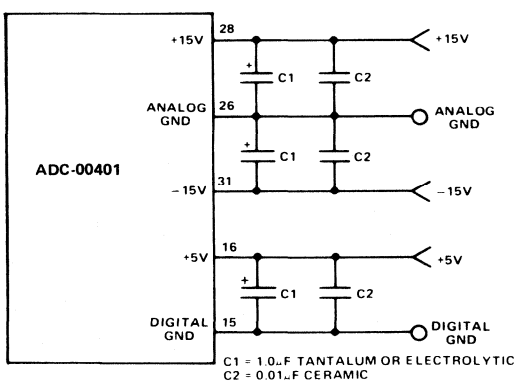


FIGURE 8. POWER SUPPLY DECOUPLING

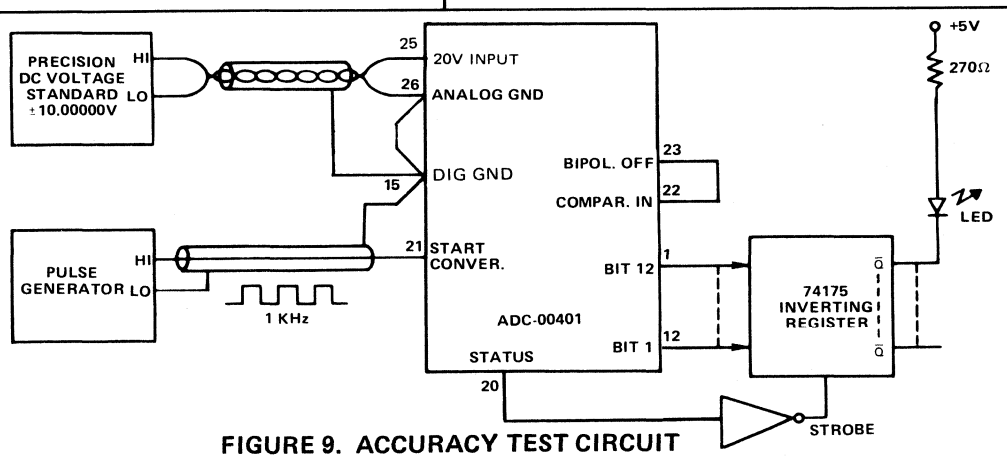


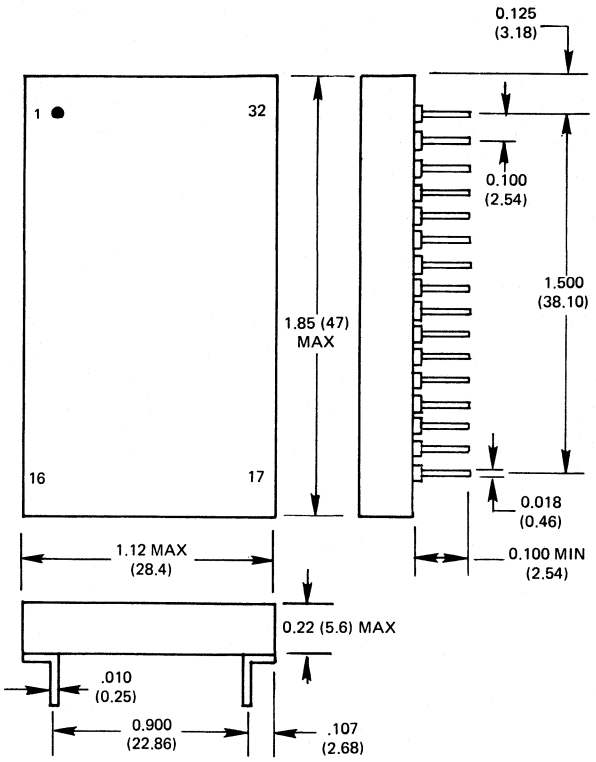
FIGURE 9. ACCURACY TEST CIRCUIT

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 12 (LSB)	17	NC*/Clk Rate Control**
2	Bit 11	18	Ref. Out (+6.2V)
3	Bit 10	19	Clock In*/Clock Out**
4	Bit 9	20	Status
5	Bit 8	21	Start Convert
6	Bit 7	22	Comparator In
7	Bit 6	23	Bipolar Offset
8	Bit 5	24	10V Range In
9	Bit 4	25	20V Range In
10	Bit 3	26	Analog Gnd
11	Bit 2	27	Gain Adjust
12	Bit 1 (MSB)	28	+15V Supply
13	$\overline{\text{Bit 1 (MSB)}}$	29	NC
14	Short Cycle	30	NC
15	Dig. Gnd	31	−15V Supply
16	+5 V Supply	32	Serial Out

*Function for external clock model only
**Function for internal Clock model only

MECHANICAL OUTLINE
32 PIN TRIPLE DIP



NOTES:
1. Dimensions shown are in inches, (millimeters)
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

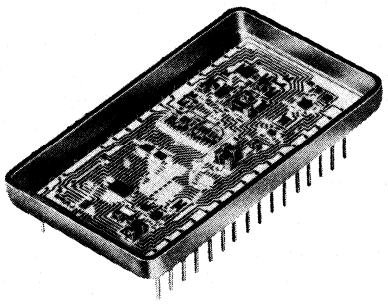
ORDERING INFORMATION

ADC - 00401 - 303

- Linearity Grade:
  - 3 = 12 bit (0.012% FSR)
  - 2 = 10 bit (0.048% FSR)
- Operating Temperature Range:
  - 3 = 0°C to +70°C
- Clock Option:
  - 1 = External Clock
  - 2 = Internal Clock

ADC-00403 AND ADC-00404

12 BIT 2μSEC HYBRID A/D CONVERTERS
Low cost, military, standard pin out



DESCRIPTION

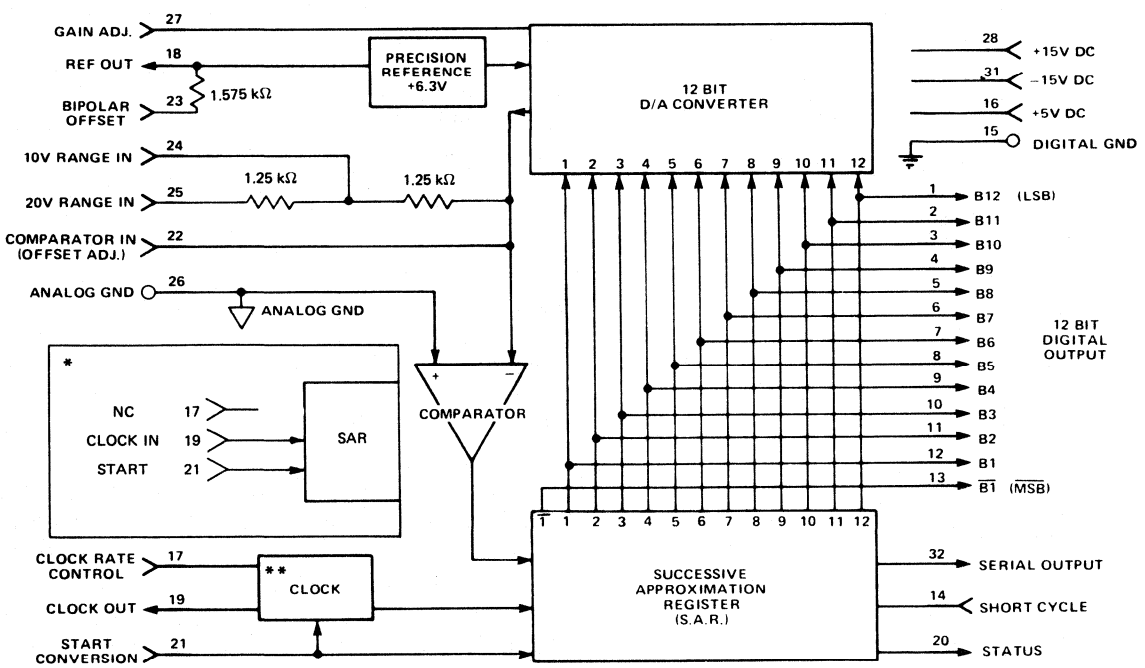
The ADC-00403 is a 12 bit 2 microsecond hybrid A/D converter packaged in a hermetic 32 pin TDIP. It offers a low cost higher speed pin for pin replacement for ADC87 and ADC85 types. Offered in models with internal (ADC-00404) or external (ADC-00403) clock, it also features precision internal reference, 6 pin programmable input voltage ranges, and both serial and parallel data output.

APPLICATIONS

With its low cost, high speed and small hermetic package, the ADC-00403 is ideal for most military and industrial data conversion applications. Typical of these applications are vibration and FFT analysis, sonar and radar digitizing, medical and nuclear instrumentation, and multiplexed data acquisition systems.

FEATURES

- *2 μSEC CONVERSION TIME*
- *12 BIT RESOLUTION AND LINEARITY*
- *LOW COST*
- *HIGHER SPEED PIN FOR PIN REPLACEMENT FOR ADC87 TYPES (NO BUFFER)*
- *32 PIN TDIP HERMETIC HYBRID*



*Function for ADC-00403 model only.
**Function for ADC-00404 model only.

FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Typical values at + 25°C case temperature and nominal power supply voltages

PARAMETER	UNITS	VALUES 10 BIT LIN	VALUES 12 BIT LIN
RESOLUTION	**Bits**	**12**	**12**
ACCURACY AND DYNAMICS			
Linearity Error	% of F.S.R.	±0.048 max	±0.012 max
Linearity Error Tempco	ppm/°C	±5 max	±2 max
Gain Error (Trimmable to zero)	% of F.S.R.	±0.1	±0.1
Gain Error Tempco	ppm/°C	±25	±15
Offset (Trimmable to zero)			
Unipolar	% of F.S.R.	±0.05 typ	±0.05 typ
Bipolar	% of F.S.R.	±0.1 typ	±0.1 typ
Offset Tempco			
Unipolar	ppm/°C	±3 max	±3 max
Bipolar	ppm/°C	±10 max	±7 max
Diff. Linearity Error	LSB	±1	±1
Conversion Time*	μs	1.5 max	2.0 max
Cycle Time*	μs	1.7 max	2.2 max
* The internal clock frequency is controlled by the applied Clock Rate Control voltage. See figure 4.			
ANALOG INPUTS			
Input Ranges			
Unipolar	V	0 to +5; 0 to +10; 0 to +20	
Bipolar	V	±2.5; ±5; ±10	
Max Voltage Without Damage	V	See figure 6.	
Impedance			
0 to +5V and ±2.5V	KΩ	0.625	
0 to 10V and ±5V	KΩ	1.25	
±10V	KΩ	2.50	
DIGITAL INPUTS			
Start Convert	nsec	50 min positive pulse. Trailing edge initiates conversion	
Loading	TTL loads	1	
DIGITAL OUTPUTS			
Parallel Data		Bit 1 through Bit 12 plus $\overline{MSB}$	
Drive	TTL loads	5	
Unipolar Coding		Complementary binary	
Bipolar Coding		Complementary offset binary or Complementary two's complement	
Serial Data		Non return to zero (NRZ)	
Drive	TTL loads	5	
Coding		Same as parallel data	
Status		Logic "1" during conversion. Logic "0" indicates valid parallel data.	
Drive	TTL loads	2	
Clock		13 positive pulses	
Period*	nsec	166 min	
Drive	TTL loads	2	
INTERNAL REFERENCE			
Voltage Output	V	+6.2 ±5%	
Current Output	mA	5 max for no degradation of specifications	
Voltage Tempco	ppm/°C	±20 max	
POWER SUPPLIES			
Voltages	V	+15 ±5%	−15 ±5% / +5 ±5%
Max Voltage Without Damage	V	+18	−18 / +7
Current (Including Internal Clock)	mA	40 typ / 50 max	65 typ / 80 max / 165 typ / 220 max
Sensitivity	%FSR/%PS	±0.002	±0.002 / ±0.002
TEMPERATURE RANGE			
Operating			
-1 Option	°C	−55 to +125	
-2 Option	°C	−25 to +85	
Storage	°C	−65 to +135	
PACKAGE			
Type		32 pin TDIP	
Size	Inch (mm)	1.14 x 1.93 x 0.2 (28.95 x 49.0 x 5.1	
Weight	Oz. (g)	0.67 (19)	

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a block diagram of the ADC-00403. Since the ADC-00403 is a successive approximation A/D converter, its main elements are a D/A Converter, a Comparator and a Successive Approximation Register. An Internal Precision Reference and internal or external Clock, depending on model selected, complete the functional elements of the ADC-00403.

The successive approximation algorithm is initiated by a Start Conversion pulse input. This results in a change of the Status output signal, indicating that a conversion is in progress and output data is invalid. In a sequence starting with Bit 1, the D/A input is set to "1" and the comparator detects whether the resulting D/A output is larger or smaller than the analog input signal. If the D/A output is larger than the analog input signal, Bit 1 is reset to "0". If not, then Bit 1 remains a "1". In succession, Bit 2 through Bit 12 are individually tested by the comparator. After 12 trials, and 13 clock pulse edges have occurred, the Successive Approximation Register (SAR) output is a digital representation of the analog input. At this time, the Status output signal changes to indicate that conversion has been completed and output data is valid.

The ADC-00403 is available in both internal clock or external clock models. The internal clock model makes the clock signal available to the user on the Clock Output pin. In addition, the Clock Rate Control input pin may be used to make fine adjustments of the internal clock frequency. The ADC-00403 may be short cycled for less than 12 bit resolution with a resulting decrease in its conversion time.

Both parallel data and serial data are provided as digital outputs from the converter. For bipolar analog input signals the digital output data is coded in Complementary Two's Complement or Complementary Offset Binary. Both Bit 1 and Bit 1 complement ($\overline{B1}$) are provided as outputs, so either of these codes may be selected. For unipolar analog input signals, the digital output data is coded in Complementary Binary.

The ADC-00403 may be configured for any of six different input signal ranges by means of jumper wires between pins. Three bipolar and three unipolar ranges are implemented with combination of the two precision scaling resistors and the precision bipolar offset resistor. Inherent offset and gain errors of the A/D converter may be trimmed to zero with the addition of potentiometers.

The ADC-00403 contains an internal precision +6.2 volt reference. This reference voltage is provided for the user at an output pin. In order to avoid affecting converter performance, care must be taken not to load the reference beyond its output capability.

To achieve the optimum performance available from the ADC-00403, it is recommended that decoupling capacitors be used on the supply lines. In addition, high frequency layout considerations should be kept in mind when designing a printed circuit board to accomodate the A/D converter. This includes minimum conductor lengths on signals, and a low impedance ground plane where possible.

TIMING DIAGRAM

A diagram of typical A/D converter timing is shown in Figure 2. A conversion is initiated by the application of a positive (50 nsec min) pulse to the Start Convert pin. A delayed (25 nsec min) clock must be applied to the Clock In pin for model ADC-00403. For model ADC-00404 the Clock Output appears after the falling edge of the Start Convert pulse. The rising edge of the clock causes the status signal to change to a "1", indicating that a conversion is in progress and parallel output data is not valid. Also in response to the clock rising edge, the MSB of the Successive Approximation Register (SAR) is reset to "0" and all other bits are set to "1". During clock period 1, the MSB trial takes place, and the MSB bit weight is compared to the analog input. The rising edge of clock pulse 2 causes the decision of the MSB trial to be stored, and simultaneously initiates the Bit 2 trial. In a successive manner, the rising edge of clock pulses 3 through 13 cause the storage of decisions on Bit 2 through Bit 12. The rising edge of clock pulse 13 causes the status signal to change to a "0", since the SAR now contains the valid 12 bit representation of the analog input. Parallel output data is valid during the interval that status signal is "0".

Serial Data is available as an output in non return to zero (NRZ) format. Data for each bit becomes valid on the rising edge of the clock pulse one number higher than the bit number, and remains valid for one clock period. Typically, Serial Data is shifted into an external 12 bit shift register, using the falling edges of the clock signal. The falling edge of clock pulse 13 would therefore shift Bit 12 into the register.

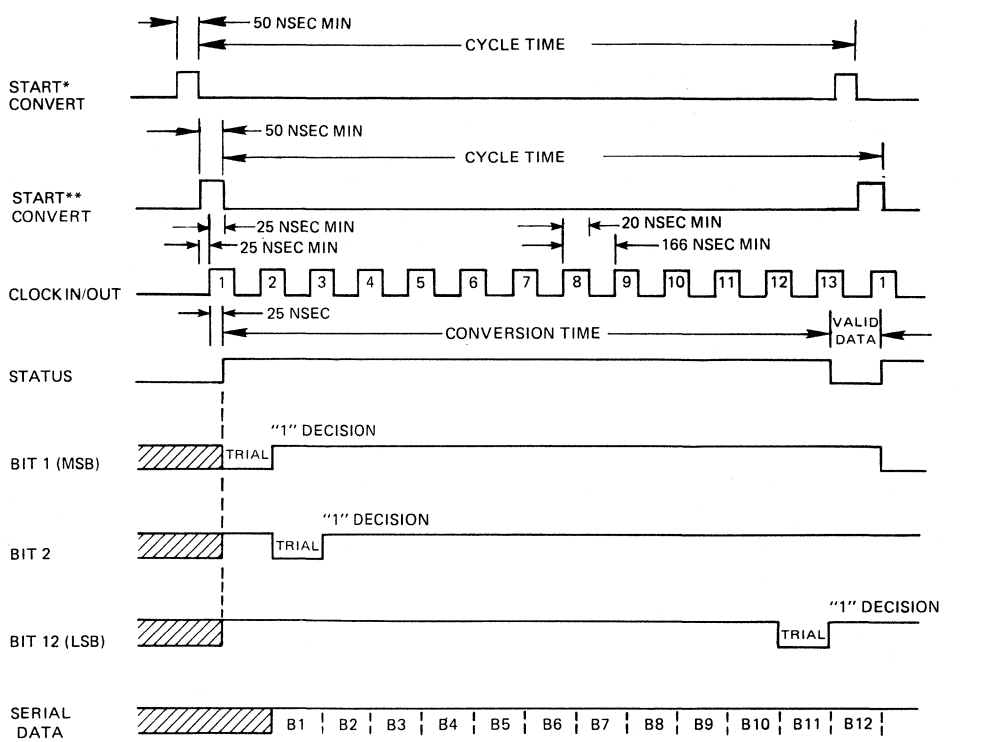
The minimum clock period allowed for rated performance of the ADC-00403 is 166 nanoseconds. This applies to both internal clock and external clock models. Conversion time is defined as the time during which the Status signal is a "1" and parallel output data is not valid. Cycle time, which is slightly longer than conversion time, is defined as the minimum time which must elapse between successive Start Convert pulses.

EXTERNAL CLOCK

The ADC-00403 is available in internal and external clock models. For external clock models the user must provide a clock signal to Clock Input (pin 19). Thirteen positive clock pulses are required to complete the conversion process. For rated A/D performance, the applied clock period must be 166 nanoseconds minimum. Figure 2 shows Clock In timing relationships. Best performance is achieved with a clock "high" duty cycle of between 12% and 33%. This sequence initiates conversions for both gated clock and continuous clock inputs. Care must be taken to comply with the minimum cycle time requirement between successive Start Convert pulses.

SHORT CYCLING AND CONTINUOUS CONVERSION

The ADC-00403 may be short cycled to fewer than 12 bits resolution, with a resulting decrease in conversion time. Figure 3 shows the required jumper connections and the resulting conversion times, with a 6 MHz clock, for 8 bit through 12 bit resolutions. For resolutions of less than 12 bits, it is possible to increase the clock frequency somewhat, since internal settling times are shorter. This may be accomplished by adjusting the Clock Rate Control voltage.



*For model ADC-00404 only.
**For model ADC-00403 only.

FIGURE 2. TIMING DIAGRAM

The ADC-00403 can be simply configured for continuous conversion operation when it is required. The falling edge of the Status (pin 20) signal is used to trigger a one shot. The one shot output, a 50 nsec minimum positive pulse, is connected to the Start Convert (pin 21) input to yield continuous conversion operation.

CLOCK RATE CONTROL

The Clock Rate Control line is made available in the internal clock model of the ADC-00403 to make small adjustments of the internal clock frequency. Figure 4 shows a typical circuit using a potentiometer to generate the Clock Rate Control voltage, and the resulting clock frequencies. For 12 bit operation, care must be taken to comply with the 166 nanosecond minimum clock period requirement. For short cycled operation, the Clock Rate Control voltage may be set greater than 5 volts, resulting in a clock frequency greater than 8 MHz.

PARALLEL DATA

Bit 1 through Bit 12 plus $\overline{\text{MSB}}$ are the parallel output data lines provided by the ADC-00403. Each signal can drive a minimum of 5 standard TTL loads. Parallel output data is valid during the time that the Status signal is a "0". If a strobe signal is required to read the parallel data into a register a "one-shot" can be triggered by the falling edge of the Status signal, or the falling edge of clock pulse 13 can be isolated by gating the Clock and Status signals together.

SERIAL DATA

Serial Data is provided by the ADC-00403 in non return to zero (NRZ) format with the MSB first. The Serial Data output line can drive a minimum of 2 standard TTL loads.

Each bit becomes valid on the rising edge of the clock pulse one number higher than the bit number, and remains valid for one clock period. Typically an external 12 bit shift register is used to store the serial data, after it has been shifted into the register using the falling edges of the clock signal. The LSB would be shifted into the register by the falling edge of clock pulse 13.

OUTPUT CODING

The ADC-00403 provides Complementary Binary coded output data for unipolar analog inputs, and either Complementary Offset Binary or Complementary Two's Complement coded output data for bipolar analog inputs. Figure 5 illustrates the output data for various analog inputs for each of the three code configurations. For bipolar analog inputs, the 2 choices of output code are available since both MSB and $\overline{\text{MSB}}$ signals are provided as outputs.

ANALOG INPUT RANGES

The ADC-00403 may be configured for any of six different input signal ranges by means of jumper wires between pins. Three bipolar and three unipolar ranges are possible. Figure 6 shows these six choices of analog input range, along with the jumper connections required to implement each range. The chart also shows, for each input range, which pin is to be used for the input signal, and what impedance will be presented at that pin. Absolute maximum input voltage is also shown for each configuration.

RESOLUTION	CONNECT PIN 14 TO	CONVERSION TIME
8 BIT	PIN 4	1.3 μsec
9 BIT	PIN 3	1.5 μsec
10 BIT	PIN 2	1.6 μsec
11 BIT	PIN 1	1.8 μsec
12 BIT	NC	2.0 μsec

FIGURE 3. SHORT CYCLE OPERATION

PIN 17 VOLTAGE	APPROXIMATE CLOCK RATE
+5V	8 MHz
0V	6 MHz

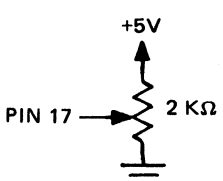


FIGURE 4. CLOCK RATE CONTROL

SCALE	BIPOLAR		UNIPOLAR
	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO'S COMPLEMENT	COMPLEMENTARY BINARY
+FS-1 LSB	0000 0000 0000	1000 0000 0000	0000 0000 0000
+3/4 FS	0001 1111 1111	1001 1111 1111	0011 1111 1111
+1/2 FS	0011 1111 1111	1011 1111 1111	0111 1111 1111
+1 LSB	0111 1111 1110	1111 1111 1110	1111 1111 1110
0	0111 1111 1111	1111 1111 1111	1111 1111 1111
− 1 LSB	1000 0000 0000	0000 0000 0000	
−1/2 FS	1100 0000 0000	0011 1111 1111	
−3/4 FS	1110 0000 0000	0001 1111 1111	
−FS	1111 1111 1111	0111 1111 1111	

FIGURE 5. OUTPUT CODING

INPUT RANGE	ABSOLUTE MAX INPUT	INPUT IMPEDANCE (OHMS)	INPUT TERMINAL	JUMPER CONNECTION
±2.5V	±3.75V	0.625 K	PIN 24	PIN 23 TO PIN 22 PIN 25 TO PIN 22
0 to +5V	+7.5V	0.625 K	PIN 24	PIN 23 TO PIN 26 PIN 25 TO PIN 22
±5V	±7.5V	1.25K	PIN 24	PIN 23 TO PIN 22
0 to +10V	+15V	1.25 K	PIN 24	PIN 23 TO PIN 26
±10V	±15V	2.5K	PIN 25	PIN 23 TO PIN 22
0 to +20V	30V	2.5 K	PIN 25	PIN 23 TO PIN 26

FIGURE 6. ANALOG INPUT RANGE

OFFSET AND GAIN TRIMS

Gain and offset errors of the ADC-00403 are factory trimmed to be less than the values listed in the specification table. The converter is externally trimmable to zero gain and zero offset error, providing the user with flexibility for applications requiring maximum performance.

Figure 7 illustrates the external trim potentiometer circuit connections required to adjust the gain and offset errors of the ADC-00403 to zero. Multi-turn trimpots, with temperature coefficient of less than 100 ppm/°C, are recommended for best performance.

If gain adjust pot is not used, connect Gain Adjust pin 27 to Analog Gnd pin 26 to minimize noise.

INTERNAL REFERENCE

The ADC-00403 contains a +6.3 volt precision internal reference, which is made available for external use. A maximum output current of 5 mA will be provided by the internal reference, while maintaining rated performance. If this load is exceeded, gain and linearity error will increase. Damage will result from excessive loading.

LAYOUT PRECAUTIONS

To achieve the optimum performance of the ADC-00403, care must be taken in the printed circuit layout. Analog input lines and digital output lines should be separated from each other, and made as short as possible. To minimize ground noise, analog and digital grounds should be connected together in close proximity to the unit. A low impedance ground plane under the converter will yield the best results.

POWER SUPPLY DECOUPLING

Capacitive decoupling of all power supplies is required to minimize noise. Figure 8 shows the recommended power supply decoupling configuration. Tantalum or electrolytic capacitors of 1 μF or greater are used for low frequency decoupling. Ceramic capacitors of 0.01 μF or greater are used for high frequency decoupling. For best results, all capacitors should be placed as close to the unit as possible.

ACCURACY TESTING

Testing of the accuracy of the ADC-00403 consists of measurement of its gain, offset and linearity errors. Figure 9 shows a simple test circuit for making these measurements. A precision DC voltage source is used to provide the analog input signal, and the digital outputs are monitored by a string of light emitting diodes (LED).

The offset error can be measured by adjusting the DC voltage source until the LEDs indicate the zero code transition. The difference between the voltage input and zero volts is the offset error. After the offset error has been measured, the circuit shown in Figure 7 should be used to trim the offset error to zero.

With the offset error trimmed to zero, the gain error can be measured by adjusting the DC voltage source until the LEDs indicate the full scale code transition. The difference between the input voltage and the theoretical full scale input is the gain error. After the gain error has been measured, the circuit shown in Figure 7 should be used to trim the gain error to zero.

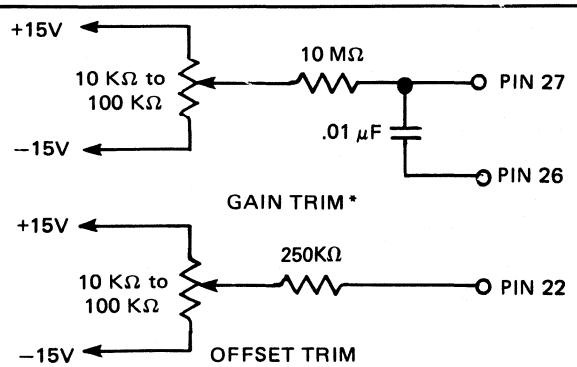


FIGURE 7. OFFSET AND GAIN TRIM

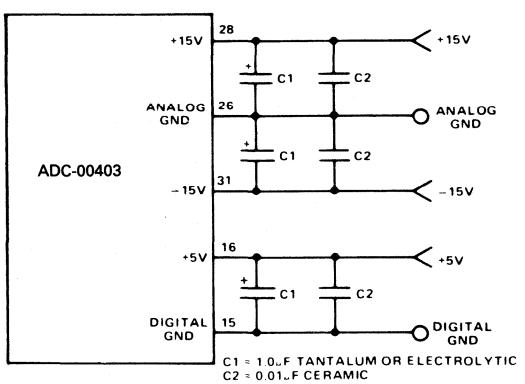


FIGURE 8. POWER SUPPLY DECOUPLING

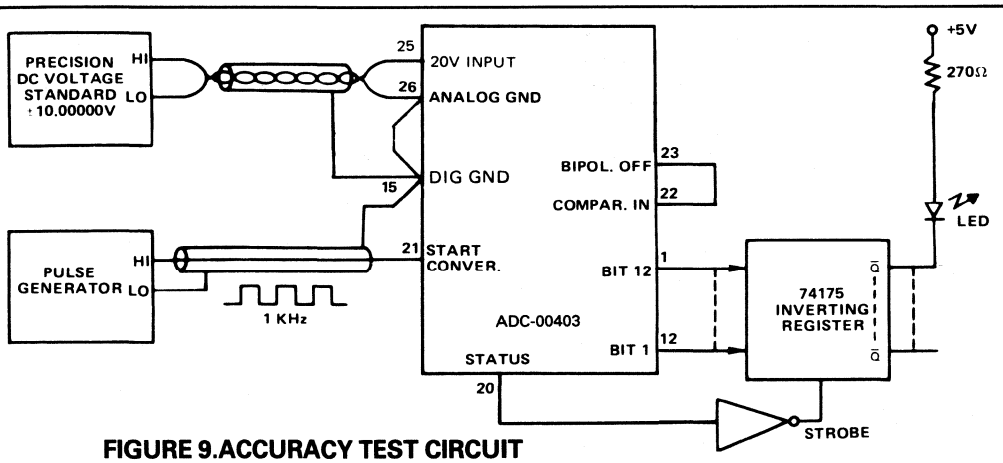


FIGURE 9.ACCURACY TEST CIRCUIT

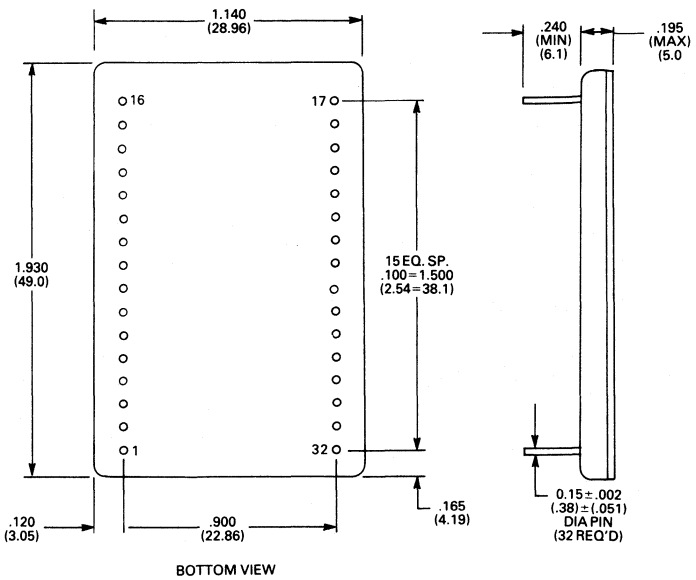
With the offset and gain errors trimmed to zero, any remaining error is a linearity error. Linearity error should be measured at the code transitions corresponding to each individual bit weight, and also at each of the major carry code transitions which occur at one count less than the individual bit weights.

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 12 (LSB)	17	NC*/Clk Rate Control**
2	Bit 11	18	Ref. Out (+6.2V)
3	Bit 10	19	Clock In*/Clock Out**
4	Bit 9	20	Status
5	Bit 8	21	Start Convert
6	Bit 7	22	Comparator In
7	Bit 6	23	Bipolar Offset
8	Bit 5	24	10V Range In
9	Bit 4	25	20V Range In
10	Bit 3	26	Analog Gnd
11	Bit 2	27	Gain Adjust
12	$\overline{\text{Bit 1 (MSB)}}$	28	+15V Supply
13	Bit 1 (MSB)	29	NC
14	Short Cycle	30	NC
15	Dig. Gnd	31	−15V Supply
16	+5 V Supply	32	Serial Out

*Function for ADC-00403 model only.
**Function for ADC-00404 model only.

MECHANICAL OUTLINE
32 PIN TRIPLE DIP



BOTTOM VIEW

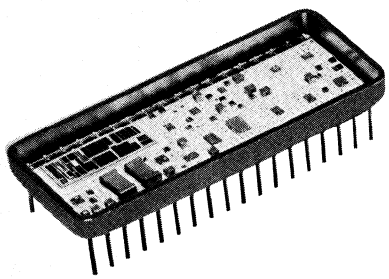
NOTES:
1. Dimensions shown are in inches, (millimeters)
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

ORDERING INFORMATION

ADC-00403-103

- Linearity Grade:
  - 3= 12 bit (0.012% FSR)
  - 2= 10 bit (0.048% FSR)
- Reliability Grade:
  - 1= Conforms to MIL-STD-883
  - 0= Same except preburn in test and burn in are omitted
- Operating Temperature Range
  - 1= −55°C to +125°C
  - 2= −25°C to +85°C
- Clock Option
  - 3= External Clock
  - 4= Internal Clock

12 BIT HYBRID A/D CONVERTER
2.0 μs Conversion Time; ±0.012% F.S. Range Linearity Error



FOR NEW DESIGNS
ORDER
ADC-00403

DESCRIPTION

Complete in a 36 pin DIP package, the ADH-8516 is the smallest 12 bit 2.0μsec analog to digital converter available. With a suitable track and hold amplifier such as Data Device Corporation's ADH-050, it can achieve word rates of 450 kHz. Conversion time may be reduced below 2.0μsec by pin programmable short cycling if less resolution is acceptable. Gain and offset can be trimmed to zero, making the accuracy equal to the ±1/2 LSB linearity. The ADH-8516 can be pin programmed to automatically ignore a new start command until internal conversion is completed, or to start a new cycle at once and abort any conversion in process, or to cycle continuously. The internal reference voltage is externally accessible.

APPLICATIONS

Because of its high speed and 3-state outputs, the ADH-8516 is especially suited for multiplexing and for interfacing with microprocessors. Applications include high-speed data acquisition systems, autocorrelation computers, PCM communications systems, radar signal processors, moving target indicators, and electronic countermeasures systems. Utilizing the advantages of thin film and MSI technologies, the ADH-8516 has very high reliability and is ideal for remotely located and hard to access equipment where small size and high MTBF are critical. Standard processing at no added cost is based on MIL-STD-883, except for burn-in which is an option.

FEATURES

- *VERY FAST HYBRID A/D WITH 3-STATE OUTPUTS*
- *CODING: Binary, Offset Binary, and Two's Complement*
- *VOLTAGE RANGES: ±2.5V, ±5V, ±10V, 0-5V, 0-10V, 0-20V*
- *BOTH SERIAL AND PARALLEL OUTPUT*
- *INTERNAL OR EXTERNAL CLOCK*
- *POWER CONSUMPTION 1.8W TYP*

SPECIFICATIONS

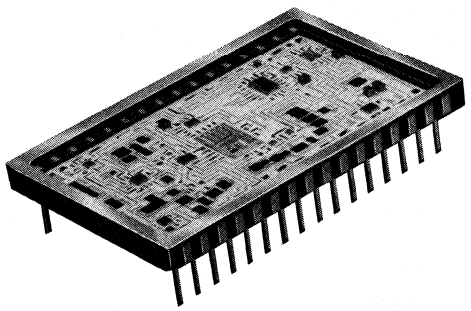
Typical values at 25°C case temperature and nominal power supply voltages

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	12	
ACCURACY AND DYNAMICS		ADH-8516-11	ADH-8516-12
Linearity Error	% F.S. Range	±0.024 Max.	±0.012 Max.
Linearity Error Tempco	ppm/°C	4 Max.	2 Max.
Gain Error (Trimmable to zero)	% F.S. Range	0.2 Typ.	0.2 Typ.
Gain Error Tempco	ppm/°C	30 Max.	20 Max.
Offset (Trimmable to zero)			
Unipolar	mV	10 Typ.	5 Typ.
Bipolar	mV	30 Typ.	10 Typ.
Offset Tempco			
Unipolar	ppm/°C	10 Typ.	5 Typ.
Bipolar	ppm/°C	25 Typ.	10 Typ.
Conversion Time	μsec	2.0 Max. for 12 bits Programmable to 1.2 Typ. for 8 bits	
Cycle Time	μsec	2.0 Typ.; 2.2 Max.	
ANALOG INPUT			
Input Ranges		Pin-Programmable	
Unipolar	V	0 to +5; 0 to +10; 0 to +20	
Bipolar	V	±2.5; ±5.0; ±10.0	
Max Voltage Without Damage	V	1.5 times F.S. input range	
Input Impedance			
0 to +5V and +2.5V Ranges	kΩ	0.625	
0 to +10V and ±5.0V Ranges	kΩ	1.25	
0 to +20V and ±10.0V Ranges	kΩ	2.5	
DIGITAL INPUT/OUTPUT (DTL/TTL COMPATIBLE)			
Digital Inputs			
Loading		1 Std. TTL load	
Start Conversion (SC)		Positive pulse; 20 nsec min., 1.5 μsec max.; Triggers on leading edge	
Clock Input (CI)		Min. period = 150 nsec; 40 – 60% duty cycle	
3-State Enable Lines		Two enable lines; MS Byte and LS Byte. Logic "0" enables output data bits	

PARAMETER	UNIT	VALUE		
DIGITAL INPUT/OUTPUT (DTL/TTL COMPATIBLE) (Cont'd)				
Short Cycle		Programs reduction in bits to obtain faster conversion		
Retrigger Input ($\overline{S}$)		Determines whether conversion can be initiated before end of cycle		
GI		Programs MSB inversion		
Digital Outputs (Buffered)				
Loading		5 Std. TTL loads, except CO = 2 Std. TTL loads		
12 Parallel Output Lines		GO, and B2 through B12; three-state		
Serial Output (SO)		Non-return to zero (NRZ)		
Clock Out (CO)		13 negative 50 nsec. typ. pulses; period = 150 nsec typ.		
Conversion Complete (CC)		Logic "0" during conversion		
B1 (MSB) and $\overline{B1}$		For pin-programmable MSB inversion		
INTERNAL REF. OUTPUT				
+ Ref Out Voltage	V	10.0 ±0.2		
+ Ref External Current Load	mA	±2 Max.		
– Ref Out Voltage (–Ref for Trimming Only)	V	–4.3 Nominal		
POWER REQUIREMENTS				
Supply Voltages	V	+15±3%	–15±3%	+5±5%
Max. Voltage Without Damage	V	+18	–18	+7
Current Typ.	mA	50	35	135
Max.	mA	65	65	250
TEMPERATURE RANGE (CASE)				
Operating				
–1 Option	°C	–55 to +125		
–3 Option	°C	0 to +70		
Storage	°C	–55 to +125		
PHYSICAL DATA				
Type of Package		36-Pin Double DIP		
Size	Inch	0.78 x 1.9 x .21 (1.98 x 4.83 x 0.53 cm)		
Weight	Oz.	0.64 Typ. (18g)		

ILC DATA DEVICE CORPORATION

12 BIT 10 μSEC HYBRID A/D CONVERTER
−55° C to +125° C Operation



FEATURES

- *PIN FOR PIN REPLACEMENT FOR INDUSTRY STANDARD ADC85/ADC87 MODELS*
- *−55° C TO +125° C OPERATION*
- *LOW POWER DISSIPATION −1.2W*
- *MIL-STD-883B SCREENING AVAILABLE (1,600,000 HOUR MTBF)*
- *OPERATION WITH ±15V OR ±12V SUPPLIES*

DESCRIPTION

The DDC ADC87 is a 12 bit 10μsec A/D converter packaged in a hermetically sealed ceramic 32 TDIP. It is a pin for pin replacement for industry standard ADC85 and ADC87 types. Offering wide operating temperature (−55° C to +125° C) and low power dissipation (1.2 Watts), the DDC ADC 87 is available screened to MIL-STD-883B. It also features internal clock and both serial and parallel data outputs.

APPLICATIONS

With its high reliability (MTBF of 1,600,000 hours), wide operating temperature, low power and small hermetic package, the DDC ADC87 meets the most demanding military and industrial requirements. Typical applications include data acquisition systems, automatic test equipment and electronic countermeasures systems.

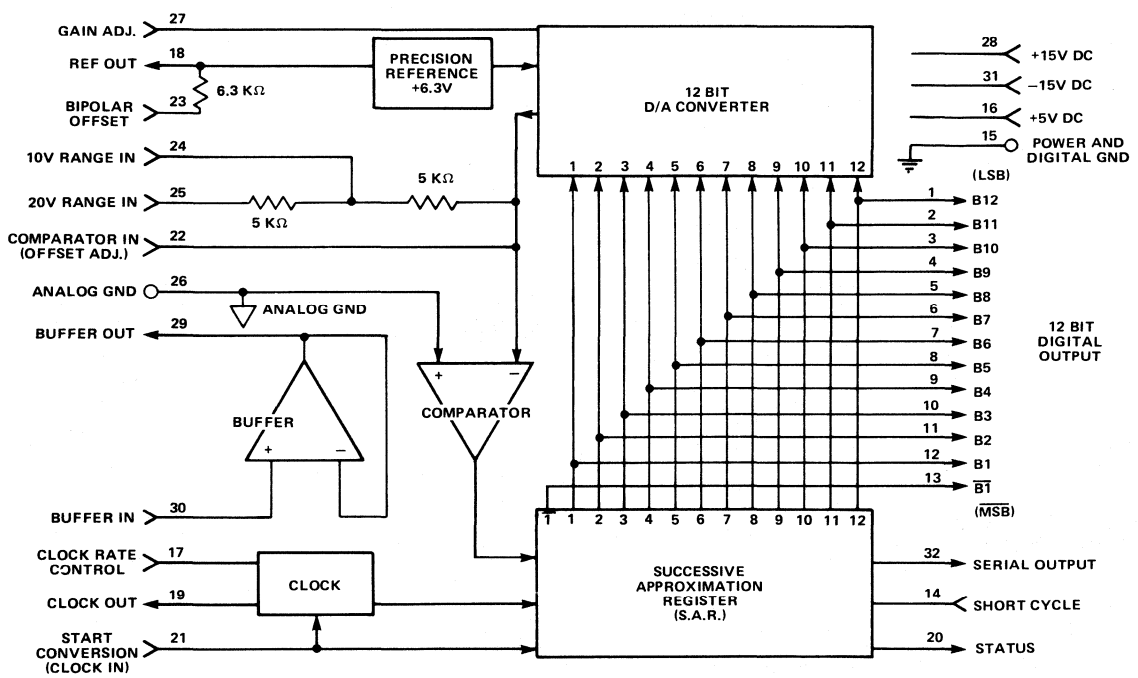


FIGURE 1. DDC ADC87 BLOCK DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION AND BLOCK DIAGRAM

The main elements of the DDC ADC87 as shown in the block diagram, Figure 1, are a voltage comparator, a 12 bit successive approximation register (S.A.R.), and a 12 bit digital to analog converter connected in a closed loop. The analog input and the D/A converter output are superimposed at the sum point of the comparator. Successive approximation is used to make the D/A output equal to the analog input. Conversions are initiated by an external START CONVERSION pulse, and a STATUS logic output indicates when a conversion has been completed and output data is available.

The 10V RANGE INPUT or 20V RANGE INPUT is connected to the analog input (depending on scaling) and the BIPOLAR OFFSET is used to select unipolar or bipolar operation. An input buffer amplifier is provided for higher input impedance, but its use has been made optional. The buffer amplifier must be allowed to settle before a conversion can be initiated.

The rate of the internal clock is determined by the voltage provided at the CLOCK RATE CONTROL input. When this input is connected to power ground, the internal clock rate is appropriate for the full accuracy 12 bit converter. However, it may be necessary to adjust the voltage to obtain the optimum clock rate.

The conversion rate can be increased by truncating the conversion at 10 or 8 bits using the SHORT CYCLE pin. Short cycling allows the clock to be speeded up. The internal clock rate can be increased by applying a more positive voltage to the CLOCK RATE CONTROL, thereby increasing the conversion rate still further. It is also possible to use an external clock.

There are two grounds in the system. The analog ground for the analog input signal is designated by ⏚. The power supply ground, designated by ⏚, is also used as a ground for all logic signals. To minimize crosstalk, the analog and power grounds are not connected internally. They should be connected as directly as possible externally, preferably with a ground plane beneath the module.

INPUT SCALING AND OUTPUT CODING

There are five input voltage ranges, with pin connections as shown in Figure 2, Connections for Normal Operation. For unipolar input (ranges 0 to +5V or 0 to +10V) the output coding using bits 1 through 12 is complementary offset binary. For bipolar input (ranges ±2.5V, ±5V, or ±10V) the output coding is either complementary straight binary using bits 1 through 12, or complementary two's complement if bits 2 through 12 and bit 1 (the MSB complement) is used. The coding is described by the transition table in Figure 3. The analog input voltage levels shown in the left hand column should correspond to the transition points between the digital codes shown at the right.

SPECIFICATIONS
Typical values at +25°C case temperature and nominal power supply voltages

PARAMETER	UNITS	VALUE 10 BIT LIN	VALUE 12 BIT LIN
RESOLUTION	Bits	12	12
ACCURACY AND DYNAMICS			
Linearity Error	% of F.S.R.	±0.048 max	±0.012 max
Linearity Error Tempco	ppm/°C	±5 max	±2 max**
Gain Error (Trimmable to zero)	%of F.S.R.	±0.1 typ	±0.1 typ
Gain Error Tempco	ppm/°C	±25 max	±15 max
Offset (Trimmable to zero)			
Unipolar	% of F.S.R.	±0.05 typ	±0.05 typ
Bipolar	% of F.S.R.	±0.1 typ	±0.1 typ
Offset Tempco			
Unipolar	ppm/°C	±3 max	±3 max
Bipolar	ppm/°C	±10 max	±7 max
Diff. Linearity Error	LSB	±1	±1
Conversion Time*	μs	10 max	10 max
Cycle Time*	μs	10.5 max	10.5 max

*The internal clock frequency is controlled by an externally applied voltage. The Conversion Time and Cycle Time values listed can be obtained by adjusting the clock voltage.
**±1 LSB max error over operating temperature range.

ANALOG INPUTS		
Input Ranges		
Unipolar	V	0 to +5; 0 to +10
Bipolar	V	±2.5; ±5; ±10
Max Voltage Without Damage	V	Two times full scale range
Impedance (Direct Input)		
0 to +5V and ±2.5V	KΩ	2.5 typ
0 to 10V and ±5V	KΩ	5 typ
±10V	KΩ	10 typ
Buffer Amplifier		
Impedance	MΩ	100 min
Bias Current	nA	100 typ; 250 max
Settling Time (to .01% for 20V step)	μs	2 typ
DIGITAL INPUT/OUTPUT (TTL COMPATIBLE)		
12 Bit Parallel Output		Positive logic, bits 1 through 12 plus MSB complement Drive capability: 2 std TTL loads Unipolar coding: Complementary Binary Bipolar coding: Complementary Offset Binary or Complementary Two's Complement
Serial Data Output		Non return to zero (NRZ); drive capability and coding same as for parallel output
Start Conversion Input		Positive pulse, 50 ns min, trailing edge initiates conversion Loading is 1 std TTL load
Status		Logic "1" during conversion; drops to "0" to indicate parallel data is available Drive capability is 2 std TTL loads
Internal Clock Output		Train of 13 positive pulses initiated by the Start Conversion trailing edge Drive capability is 2 std TTL loads Clock Frequency can be changed by pin programming or by external potentiometer adjustment
INTERNAL REFERENCE OUTPUT		
Voltage Level	V	+6.3 ±5%
Current	mA	0.2 max for no degradation in specifications
Voltage Tempco	ppm/°C	±10 max

PARAMETER	UNITS	VALUE		
POWER SUPPLIES				
Supply Voltages	V	+11.75 to +15.75	−11.75 to −15.75	+5 ±5%
Max Voltage Without Damage	V	+18	−18	+7
Current	mA	13 typ 20 max	18 typ 25 max	50 typ 75 max
Power Supply Sensitivity	%FSR/%PS	±0.002	±0.002	±0.001
THERMAL CHARACTERISTICS				
Temperature Ranges (Case)				
Operating	°C	−55 to +125		
Storage	°C	−55 to +135		
Thermal Impedances				
Case to Air	°C/Watt	θ_{CA} = 15		
Junction to Case	°C/Watt	θ_{JC} = 2		
PHYSICAL CHARACTERISTICS				
Type of Package		Ceramic case, hermetically sealed, 32 pin triple DIP		
Size	inches	1.75 x 1.15 x 0.22 (4.45 x 2.92 x 0.56 cm)		
Weight	oz	0.67 typ (19g)		

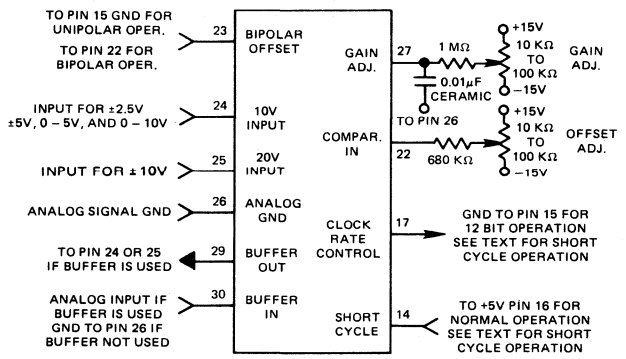


FIGURE 2. CONNECTIONS FOR NORMAL OPERATION

TIMING DIAGRAM AND EXTERNAL CLOCK

The timing for normal 12 bit operation of the DDC ADC87 is shown in Figure 4. The trailing edge of the START CONVERSION pulse starts the conversion by initiating the first of the 13 equal positive pulses of the internal clock. The leading edge of the first clock pulse then causes the STATUS to go to logic "1" and also causes the first bit to be tried. The leading edge of the second clock pulse causes Bit 2 to be tried, and Bit 1 then becomes valid. The twelfth clock pulse causes Bit 12 to be tried. Bit 12 becomes valid after the leading edge of the clock pulse 13, and the STATUS then drops to logic "0" to indicate that the conversion has been completed.

The SERIAL DATA OUTPUT is a non return to zero type (NRZ). Data for each bit becomes valid at the same time as the corresponding parallel data for the same bit, and remains valid for one clock cycle. A recommended way to clock data from the SERIAL OUTPUT is to use the trailing edge of each clock pulse to shift the data into a twelve bit shift register.

An EXTERNAL CLOCK can also be used as indicated in Figure 4. If the START CONVERSION input is at logic "1" at a time when any internal clock would normally be initiated, the clock is turned off and neither that pulse nor subsequent pulses will exist. Because of this feature an external clock with negative pulses can be applied to the Start Conversion input, pin 21. The leading edge of the first negative external clock pulse turns on the internal clock and Bit 1 is tried. If the external clock pulse is shorter than 200 ns, the Start Conversion input will be at logic "1" at the time when the second internal clock would normally be initiated, so the internal clock will turn off. The external clock is then free to initiate the trial of Bit 2 at any time. The only limitation on the rate of the external clock is that it must be no faster than twice the rate of the internal clock. The clock rate control could be used to adjust the internal clock rate to meet this criterion.

SHORT CYCLING AND CLOCK RATE CONTROL

The minimum conversion time and minimum cycle time depend on the number of bits tried and on the clock period. The clock period must be long enough to allow the comparator to settle out.

The number of bits tried can be reduced for both units by changing the SHORT CYCLE pin connection. Pin 14 is connected to the next higher bit than the number of bits to be tried. For instance, for 10 bits, connect pin 14 to pin 2 (bit 11). For 8 bits, connect pin 14 to pin 4 (bit 9).

When fewer bits are tried, it is possible to increase the clock rate because less accuracy is required. For full 12 bit operation when no particular or optimum conversion time is required, the Clock Rate Control, pin 17, is usually grounded as shown in Figure 2. In the same way, when rates are not critical, pin 17 can be connected to +5V for 10 bit operation and +15V for 8 bit operation. Optimum clock rates will generally require fine adjustment of the clock voltage. The approximate clock rates with the three standard voltage levels are:

PIN 17 Voltage	Approximate Clock Rate
0V	1.3 MHz
+5V	2 MHz
+15V	2.5 MHz

If both short cycling and pin-programmed clock rate control are used to increase the conversion rate, the following nominal conversion times are obtained for 10 and 8 bits:

Resolution	Pin 17 Voltage	Conversion Time
12 Bits	0V	10μs
10 Bits	+5V	6μs
8 Bits	+15V	4μs

TRANSITION VALUE		DIGITAL BIT OUTPUTS											
UNIPOLAR	BIPOLAR	MSB											LSB
COMPLEMENTARY BINARY	COMPLEMENTARY OFFSET BINARY	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12
+F.S. – 3/2 LSB	+F.S. – 3/2 LSB	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 1
+3/4 F.S. – 1/2 LSB	+1/2 F.S. – 1/2 LSB	0 0	0 1	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
+1/2 F.S. + 1/2 LSB	+ 1/2 LSB	0 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	0 1
+1/2 F.S. – 1/2 LSB	–1/2 LSB	0 1	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
+1/4 F.S. + 1/2 LSB	–1/2 F.S. + 1/2 LSB	1 1	0 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	0 1
+3/2 LSB	–F.S. + 3/2 LSB	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	0 1	1 0
+1/2 LSB	–F.S. + 1/2 LSB	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	0 1

3A. Theoretical transition values for Complementary Binary and Complementary Offset Binary coding. For Complementary Two's Complement coding, all values are the same as for Complementary Offset Binary, except that the MSB is reversed (MSB bits "0" become "1" and "1" become "0").

VOLTAGE RANGE	FULL SCALE (VOLTS)	1/2 LSB (VOLTS)
±2.5V	2.50000	0.00061
±5V	5.00000	0.00122
±10V	10.00000	0.00244
0 – 5V	5.00000	0.00061
0 – 10V	10.00000	0.00122

3B. Full Scale (F.S.) and 1/2 LSB for 12 bit accuracy.

FIGURE 3. THEORETICAL TRANSITION VALUES

Resolution	+V	R	Conversion Time
12 Bits	+5V	2 KΩ	6.8 – 10μs
10 Bits	+15V	5 KΩ	4.0 – 6μs
8 Bits	+15V	5 KΩ	3.5 – 6μs

Note that if the clock rate is increased to a value greater than that specified for the number of bits required, the linearity error will be substantially increased.

The CLOCK RATE CONTROL can also be connected to negative voltages as large as –15V, and this will decrease the clock rate.

The clock rates and conversion times listed are nominal values. To adjust the clock rate accurately, pin 17 may be connected to a voltage divider as shown in Figure 5. R is a multi-turn trim potentiometer with a tempco of ±100 ppm/°C or less. The range of adjustment of the clock rate will be nominally as follows:

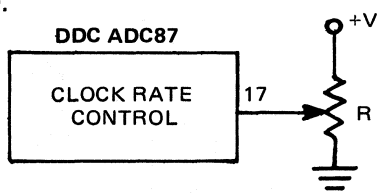


FIGURE 5. OPTIONAL CLOCK RATE FINE ADJUSTMENT

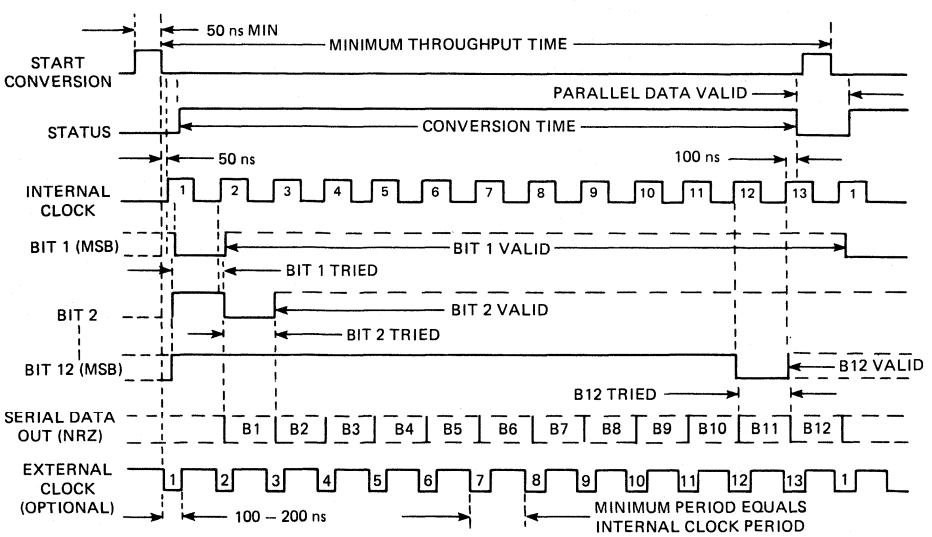


FIGURE 4. DDC ADC87 TIMING DIAGRAM

OFFSET AND GAIN TRIM

The gain and offset of the DDC ADC87 are factory trimmed to the values listed in the specifications table. Both errors can be trimmed to zero in the final application by using the potentiometer adjustment circuits shown in Figure 2.

To reduce noise, the GAIN ADJUST, pin 27, should be bypassed with a 0.01μF ceramic capacitor to analog ground as shown in Figure 2 even if no gain trim potentiometers are installed.

ACCURACY TESTING

The accuracy of the DDC ADC87 is specified by its linearity error, gain, offset, and differential linearity.

The arrangement shown in Figure 6 may be used to measure the bit transitions. Offset trim, gain trim, and other standard connections are not shown. Shielded twisted pair cable is used to connect the Precision Voltage Standard, and each of the twelve bits requires its own LED indicator. The inverting register is used to increase the duty cycle of the LSB bits since they are held at logic "1" during most of the timing cycle as indicated in the timing diagram. The NOT outputs ($\overline{Q}$) from the register are used so that a lighted LED will represent logic "1" Readings should be taken with the converter energized, in thermal equilibrium at 25°C, and after a warm-up time of 5 minutes. The Pulse Generator can be set at any frequency up to the maximum allowed for the converter. The power supply voltages should be at their nominal values.

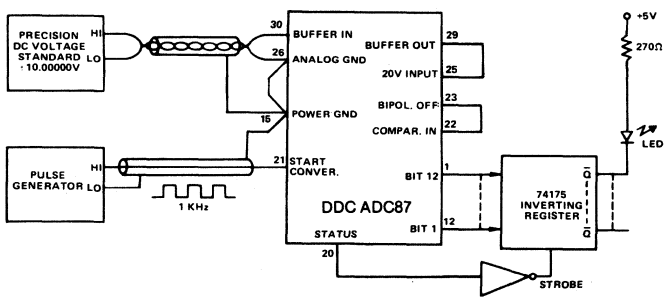


FIGURE 6. CIRCUIT TESTING ACCURACY

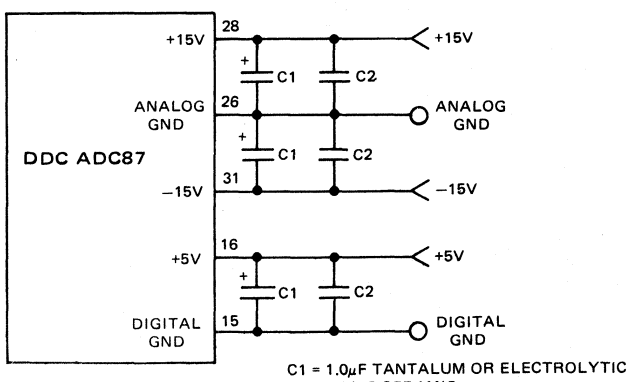


FIGURE 7. POWER SUPPLY DECOUPLING CAPACITORS

The suggested test procedure is as follows:

(1) Trim the offset by sweeping the input through the transition at −FS + 1/2 LSB in the transition value table, Figure 3. Adjust the Offset potentiometer until there is a 50% dither of the LSB.

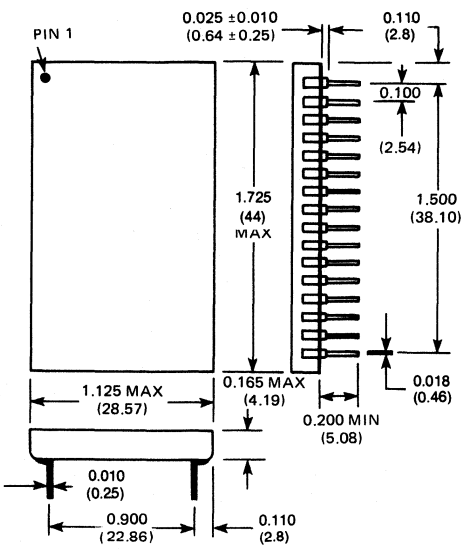
(2) Trim the gain by sweeping the input through the transition at all bits ON in Figure 3 (+FS + 3/2 LSB for bipolar coding). Adjust the Gain potentiometer for a 50% dither of the LSB.

(3) Repeat steps (1) and (2) in case there is a slight interaction between the offset and gain trims.

(4) Measure the input voltage levels at which other transitions occur. The differences between these voltages and the theoretical values will be within ±1/2 LSB.

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	17	CLOCK RATE CNTL
2	BIT 11	18	REF. OUT (+6.3V)
3	BIT 10	19	CLOCK OUT
4	BIT 9	20	STATUS
5	BIT 8	21	START CONVERT
6	BIT 7	22	COMPARATOR IN
7	BIT 6	23	BIPOLAR OFFSET
8	BIT 5	24	10V RANGE
9	BIT 4	25	20V RANGE
10	BIT 3	26	ANALOG GND
11	BIT 2	27	GAIN ADJ
12	BIT 1 (MSB)	28	+15 SUPPLY
13	BIT $\overline{1}$ ($\overline{\text{MSB}}$)	29	BUFFER OUT
14	SHORT CYCLE	30	BUFFER IN
15	DIG. GND	31	−15V SUPPLY
16	+5V SUPPLY	32	SERIAL OUT

MECHANICAL OUTLINE
32 PIN TRIPLE DIP



NOTES:
1. Dimensions shown are in inches, (millimeters)
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with capacitors as shown in Figure 7 to assure noise free operation. These capacitors should be located as close to the converter as possible. The 0.01μF ceramic capacitors imporve high frequency performance.

RELIABILITY

The use of MSI and thin film resistance networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All DDC ADC 87 hybrid converter products are manufactured to meet military standards for high reliability. DDC hybrids are built in conjunction with the requirements of MIL-STD-883 Test Methods and Procedures for Microelectronics. The screening procedures are based on Methods 5004/5008 except for burn-in, which is optional. Preburn-in may be included by adding-883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn-in) is 1,600,000 hours, Ground Fixed, at 25°C.

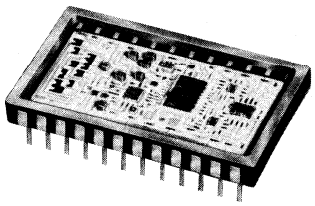
ORDERING INFORMATION

DDC ADC87–12–883B

MIL-STD-883 Processing:
- 883B = Conforms to MIL-STD-883 DDC procedures.
- Blank = Same, except burn-in is omitted.

Linearity:
- 12 = 12 bits (±.012% F.S.R.)
- 10 = 10 bits (±.048% F.S.R.)

HIGH SPEED 8 BIT A/D CONVERTER



DESCRIPTION AND APPLICATIONS

The DDC 5101 is a very high speed, 8 bit, successive approximation A/D converter, packaged in a 24 pin hermetic double DIP. All specifications are met with a conversion time of 900 nsec. Linearity error of 1/2 LSB and no missing codes are guaranteed over the entire operating temperature range. Functional laser trimming of a thin film resistor network results in extremely accurate and highly stable adjustment-free performance (See figure 1).

The DDC 5101 provides 9 user selectable input ranges, as well as 0°C to +70°C or −55°C to +125°C temperature ranges. The DDC 5101 is a pin for pin replacement for the MN5101 A/D Converter.

Because of its high reliability, hermetically sealed small package, and adjustment free operation over a wide temperature range, the DDC 5101 is ideally suited for the most demanding military and industrial requirements. Typical applications include systems for radar signal digitizing, high speed data acquisition and electronic countermeasures.

FEATURES

- *PIN FOR PIN REPLACEMENT FOR MN5101*
- *HIGH SPEED CONVERSION 900 nsec Max*
- *24 PIN HERMETIC DOUBLE DIP*
- *± 1/2 LSB LINEARITY No Missing Codes Over Temperature*
- *ADJUSTMENT FREE*
- *AVAILABLE SCREENED IN ACCORDANCE WITH MIL-STD-883*

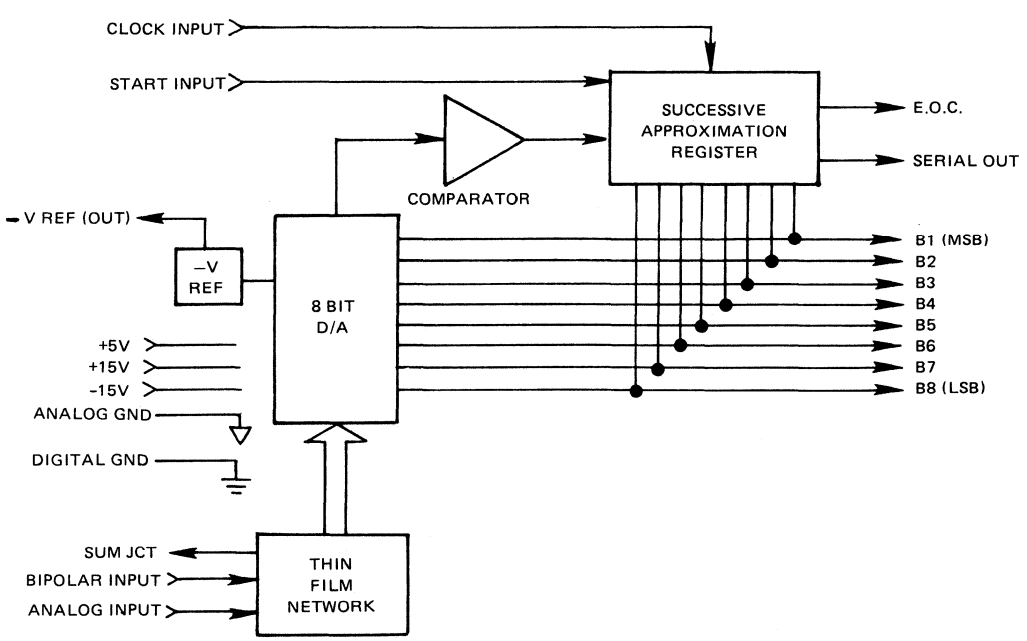


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS					
PARAMETER	UNITS	VALUE			
RESOLUTION		8			
ACCURACY AND DYNAMICS		MIN	TYP	MAX	
Absolute Accuracy*					
+25°C	LSB			±1/2	
0°C to +70°C (–3)	LSB			±1	
–55° C to +125° C (–1)	LSB			±2	
Linearity					
0°C to +70°C (–3)	LSB			±1/2	
–55° C to +125° C (–1)	LSB			±1/2	
Conversion Time (see * in Technical Information)	ns			900	
ANALOG INPUTS					
Unipolar Ranges			Unipolar		
Input Voltages	V	0 to +5	0 to +10	0 to +20	
Input Impedance (ohms)	Ω	1.5k	3.0k	6.0k	
Biopolar Ranges			Biopolar		
Input Voltage	V	+2.5	+5.0	+10.0	
Input Impedance (ohms)	Ω	1.5k	3.0k	6.0k	
Maximum Input Without Damage	V			+25	
DIGITAL INPUT/OUTPUT					
Threshold Logic Levels					
Logic "1" Input	V	2.0			
Logic "0" Input				0.8	
Clock Input					
Frequency	MHz	8.8 must have drive capability of 1 std TTL load			
Srart Conversion Input		2 std TTL loads. Start conversion pulse duration must be a 25nsec, min			
8 Bit Parallel Output		Positive logic, bits 1 through 8			
Serial Data Output		Non return zero (NRZ)			
Drive Capability		5 std TTL loads			
Digital Coding					
Unipolar Ranges		Complementary Binary			
Bipolar Ranges		Complementary Offset Binary			
POWER SUPPLY CHARACTERISTICS					
Power Supply Range	V	+15V ±3%	–15V ±3%	+5V ±5%	
Current	mA	24 typ 27 max	16 typ 25 max	89 typ 125 max	
Power Supply Rejection	%FSR/%PS	±0.01 typ	±0.03 typ	±0.01 typ	
Power Consumption	mW	1045 typ 1405 max			
PHYSICAL CHARACTERISTICS					
Size	in	1.3 x 0.8 x 0.2 (34 x 21 x 5mm)			
Weight	oz	0.25 (7.2g)			

line stays low. The conversion begins on the first low to high clock pulse after the START line goes high. Eight bits are tried in succession, MSB through LSB and serial data is available as each bit is set. Parallel data is valid 900nsec after the conversion begins.* Data is valid as long as E.O.C. is low. A new conversion may be commenced at any time during a conversion by driving the START line to logic "0".

*900 nsec conversion time is achieved with clock input frequency of 8.8 MHz. Faster conversion times are available; please contact DDC for details.

INPUT CONFIGURATIONS

INPUT RANGE	INPUT PIN	INPUT IMPEDANCE (Ω)	PIN JUMPERS
0 to - 5V	11	1.5K	8 to 12, 10 to 7, 9.
0 to -10V	11	3.0K	10 to 7, 9.
0 to -20V	12	6.0K	10 to 7, 9.
0 to + 5V	11	1.5K	8 to 7, 9, 12.
0 to +10V	11	3.0K	8 to 7, 9.
0 to +20V	12	6.0K	8 to 7, 9.
±2.5V	11	1.5K	8 to 9,12; 10 to 7.
±5.0V	11	3.0K	8 to 9; 10 to 7.
±10V	12	6.0K	8 to 9; 10 to 7.

TECHNICAL INFORMATION

The DDC 5101 A/D Converter resets after a low logic signal is applied to the START pin. This signal must be at least 25nsec in duration, to insure proper reset (See figure 2). The converter remains initialized as long as the start

DIGITAL OUTPUT CODING

The digital output coding for the DDC 5101 is Complementary Binary (unipolar input ranges) and Complementary Offset Binary (bipolar input ranges). The table below shows the specific code and voltage at which that code occurs for each of the nine input ranges.

ANALOG INPUT (VOLTS)									DIGITAL CODE	
0 to –5V	0 to –10V	0 to –20V	0 to +5V	0 to +10V	0 to +20V	±2.5V	±5.0V	±10.0V	MSB	LSB
0.000	0.000	0.000	+4.981	+9.961	+19.922	+2.500	+5.000	+10.000	0000	0000
–0.019	–0.039	–0.078	+4.961	+9.922	+19.844	+2.481	+4.961	+ 9.922	0000	0001
–2.481	–4.961	–9.922	+2.500	+5.000	+10.000	+0.019	+0.039	+ 0.078	0111	1111
–2.500	–5.000	–10.000	+2.481	+4.961	+ 9.922	0.000	0.000	0.000	1000	0000
–4.961	–9.922	–19.844	+0.019	+0.039	+ 0.078	–2.461	–4.922	– 9.844	1111	1110
–4.981	–9.961	–19.922	0.000	0.000	0.000	–2.481	–4.961	– 9.922	1111	1111

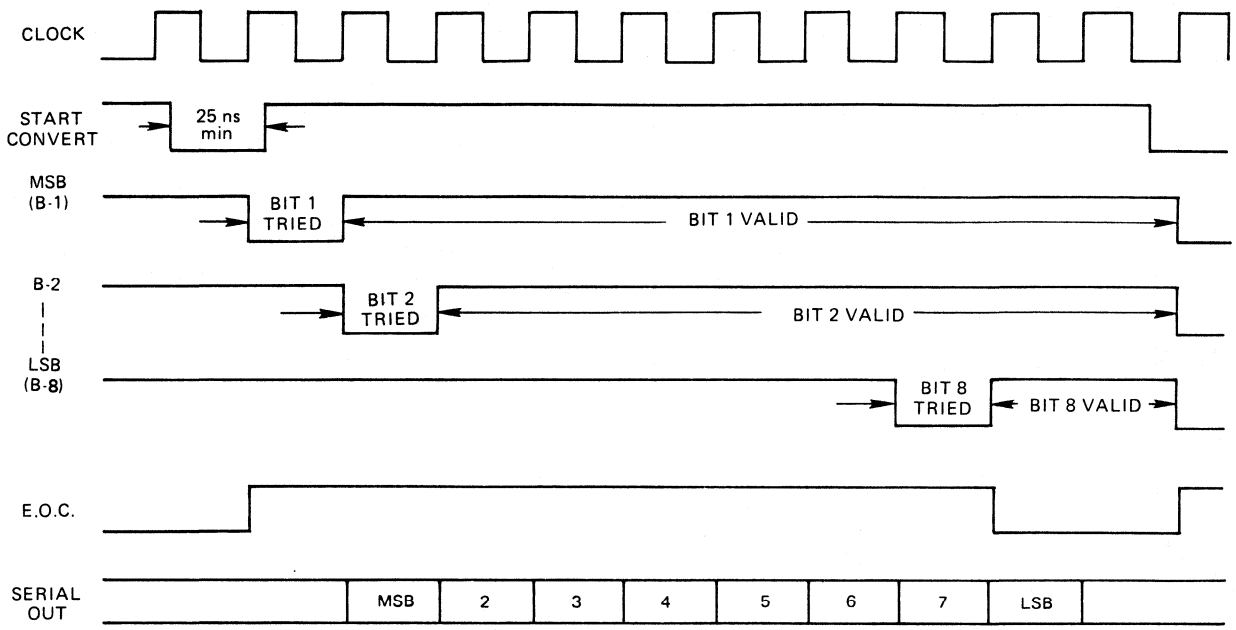


FIGURE 2. TIMING DIAGRAM

POWER SUPPLY DECOUPLING

The recommended power supply decoupling procedure is illustrated in Figure 3. The by-pass components shown in the diagram are 1.0 μF electrolytic capacitors paralleled with 0.01 μF disc ceramic capacitors.

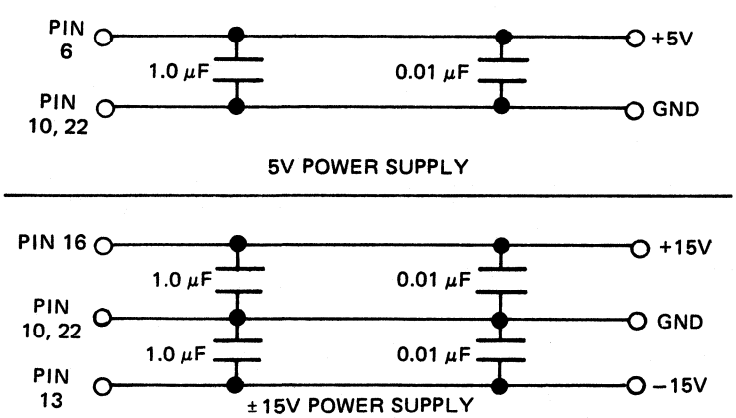
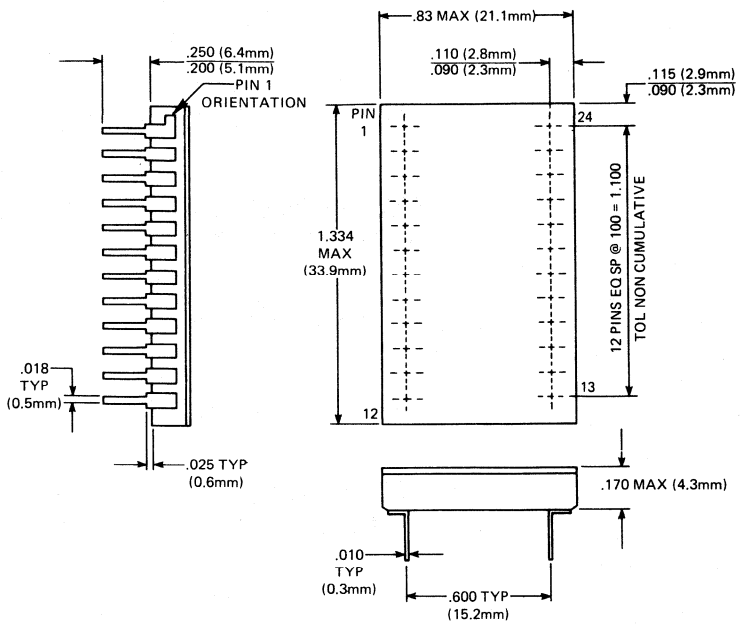


FIGURE 3. POWER SUPPLY DECOUPLING

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	SERIAL OUT	13	−15V
2	B4	14	−V REF
3	B3	15	NC
4	B2	16	+ 15V
5	B1 (MSB)	17	B8 (LSB)
6	+ 5V	18	B7
7	BIPOLAR	19	B6
8	SUM JCT	20	B5
9	BIPOLAR	21	E.O.C.
10	ANALOG GND	22	DIGITAL GND
11	INPUT	23	CLOCK
12	INPUT	24	START

MECHANICAL OUTLINE



Notes:
1. Dimensions in inches (millimeters)

HYBRID PROCESSING

All DDC-5101 converter products are manufactured to meet military standards for high reliability. DDC hybrids are build in conjunction with the requirements of MIL-STD-883, Test Methods and Procedures for Microelectronics. The screening procedures are based on methods 5008.

ORDERING INFORMATION

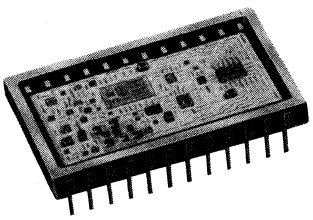
DDC 5101 — 1 — 883B

- MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883 DDC procedures.
  - Blank = Same, except pre burn in test and burn in are omitted.
- Operating Temperature Range:
  - -1 = -55° C to +125° C
  - -3 = 0° C to +70° C

NOTE: MIL-STD-883 screening available in —1 temperature range only.

DDC
ILC DATA DEVICE CORPORATION

12 BIT 50 μsec HYBRID A/D CONVERTER



DESCRIPTION

The DDC 5200 Series A/D Converters are 12 bit, successive approximation devices, in hermetically sealed 24 pin double DIP hybrid packages. All specifications are met with an externally applied 240 KHz clock, providing a conversion time of 50 μsec. Functional laser trimming of a thin film resistor network results in extremely accurate and highly stable adjustment free converters. Linearity error is guaranteed to be better than 1/2 LSB, with no missing codes over the specified temperature range.

These converters are available in two unipolar and two bipolar input ranges and will operate with full accuracy at temperatures of 0°C to + 70°C or −55°C to +125°C. The DDC 5200 Series converters are form-fit-function replacements for the MN5200 Series A/D converters.

APPLICATIONS

Because of their high reliabilty, hermetically sealed package, low power consumption, wide temperature and dynamic range, the DDC 5200 Series will meet the most demanding military and industrial requirements. Typical application include data acquisition systems, automatic test equipment and electronic countermeasures.

FEATURES

- *FORM-FIT-FUNCTION REPLACEMENT FOR MN5200 SERIES*
- *24 PIN, HERMETIC SEAL DOUBLE DIP HYBRID*
- *LOW POWER CONSUMPTION*
- *50 μSEC CONVERSION TIME*
- *ADJUSTMENT FREE WITH ACCURACY TO ±0.05% FSR*
- *AVAILABLE SCREENED IN ACCORDANCE WITH MIL-STD-883B*

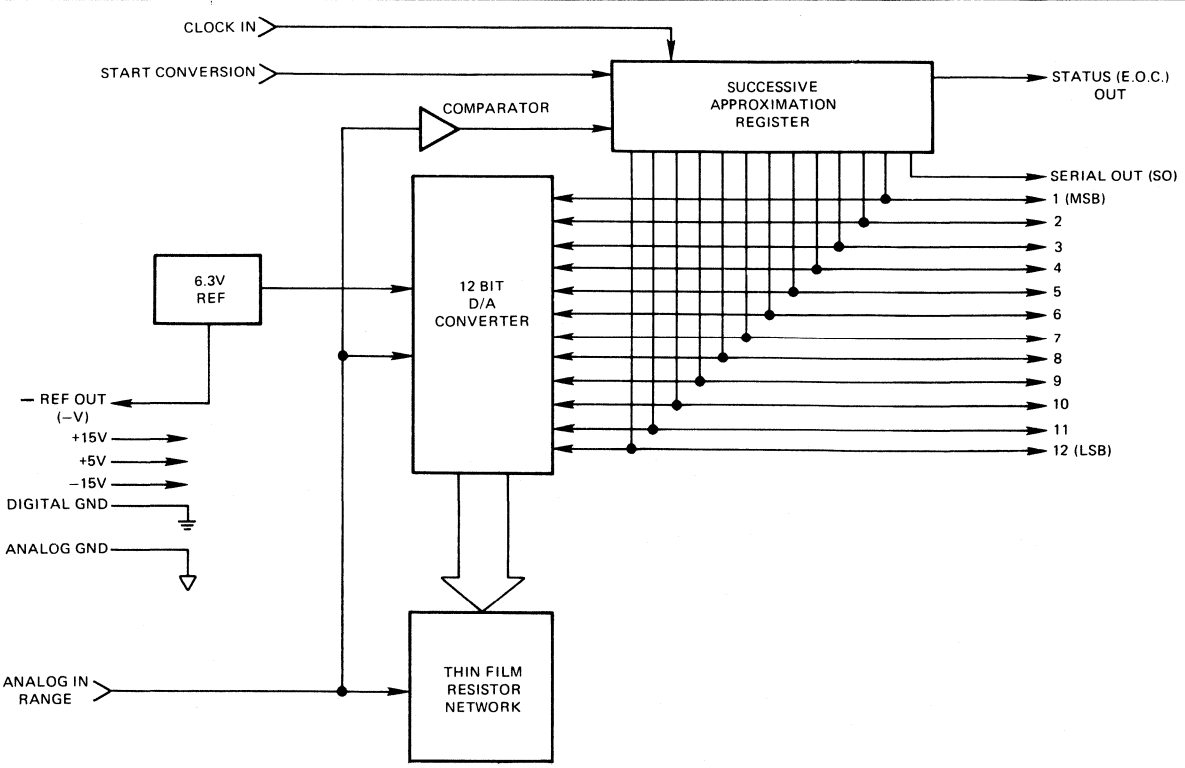


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Typical values at +25° C ambient temperature and nominal power supply voltages

PARAMETER	UNIT	VALUE			
ANALOG INPUTS		DDC 5200	DDC 5201	DDC 5202	DDC 5206
Input Ranges	V	0 to −10	−5 to +5	−10 to +10	0 to +10
Input Impedance	kΩ	6.7	6.7	13.4	13.4
Maximum without damage	V	±25	±25	±25	±25
RESOLUTION	bits	12			
ACCURACY AND DYNAMICS					
Linearity Error	LSB	TYP		MAX	
+25° C		±1/4		±1/2	
0° C to +70° C (−3)		±1/4		±1/2	
−55° C to +125° C (−1)				±1/2	
Differential Linearity Error	LSB	1/2			
No Missing Codes		Guaranteed over temperature			
Full Scale Absolute Accuracy Error					
+25° C	%FSR	±0.025		±0.05	
0° C to +70° C (−3)	%FSR	±0.2		±0.4	
−55° C to +125° C (−1)	%FSR			±0.4	
Zero Error					
+25° C	%FSR	±0.01		±0.025	
0° to 70° C (−3)	%FSR	±0.025		±0.05	
−55° C to +125° C (−1)	%FSR			±0.05	
Gain Error	%	±0.025			
Gain Drift	ppm/° C	±10			
Conversion Time	µs			50	
DIGITAL INPUTS		MIN	TYP	MAX	
Clock Input (External)					
High Pulse	ns	125			
Low Pulse	ns	175			
High Loading	µA		2	20	
Low Loading	mA		−0.25	−0.4	
Frequency	KHz			240	
Start Conversion Input					
High Loading	µA		4	40	
Low Loading	mA		−0.25	−0.4	
Setup Time	ns	25			
Logic Levels					
Logic "1"	V	2.0			
Logic "0"	V			0.7	
DIGITAL OUTPUTS					
Logic Coding					
Unipolar Ranges		Complementary Straight Binary			
Bipolar Ranges		Complementary Offset Binary			
Logic Levels		MIN	TYP	MAX	
Logic "1"	V	2.4	3.6		
Logic "0"	V		0.15	0.3	
Output Drive Capability					
Logic "1"	TTL Loads	8			
Logic "0"	TTL Loads	2			
REFERENCE OUTPUT		MIN	TYP	MAX	
Internal Reference					
Voltage	V		−6.3		
Accuracy	%		±2		
Drift Tempco	ppm/° C		±5		
Max External Current (without buffer)	µA			100	
POWER SUPPLIES					
Power Supply Range					
+15V Supply	%			±3	
+5V Supply	%			±5	
Power Supply Rejection					
+15V Supply	%FSR/%ps		±0.005	±0.02	
−15V Supply	%FSR/%ps		±0.01	±0.05	
Current					
+15V Supply	mA		+9	+13	
−15V Supply	mA		-20	-30	
+5V Supply	mA		+44	+54	
Power Consumption	mW		650	915	
PHYSICAL CHARACTERISTICS					
Size	in	1.3 X 0.8 X 0.2	(33.9 X 21.1 X 0.5mm)		
Weight	oz	0.2			

TECHNICAL INFORMATION

The DDC 5200 Series A/D converters reset internal logic on a low to high clock transition, while the Start Conversion (pin 1) is low. The Start line must be low 25nsec. (min) prior to a low to high clock transition (see Figure 2). The converter will remain reset until the Start line is allowed to go high. Conversion commences upon the next low to high clock transition. Data is available 50 µsec after the clock transition (commencing the conversion) occurs. A status (EOC) output signal (logic "1"), is presented on pin 22, at a maximum of 120 nsec after the Start line is driven low. Twelve bits are tried in succession, MSB through LSB, and serial data is immediately available on pin 3 during the conversion. Parallel data is available 30 nsec (max) after the Status (EOC) line returns to logic "0". Output data is held in the latch until another Start Conversion signal is input on pin 1. The drive capability of output data is two TTL loads. Continuous conversions may be accomplished by connecting the Status (EOC) output (pin 22) to the Start Conversion (pin 22).

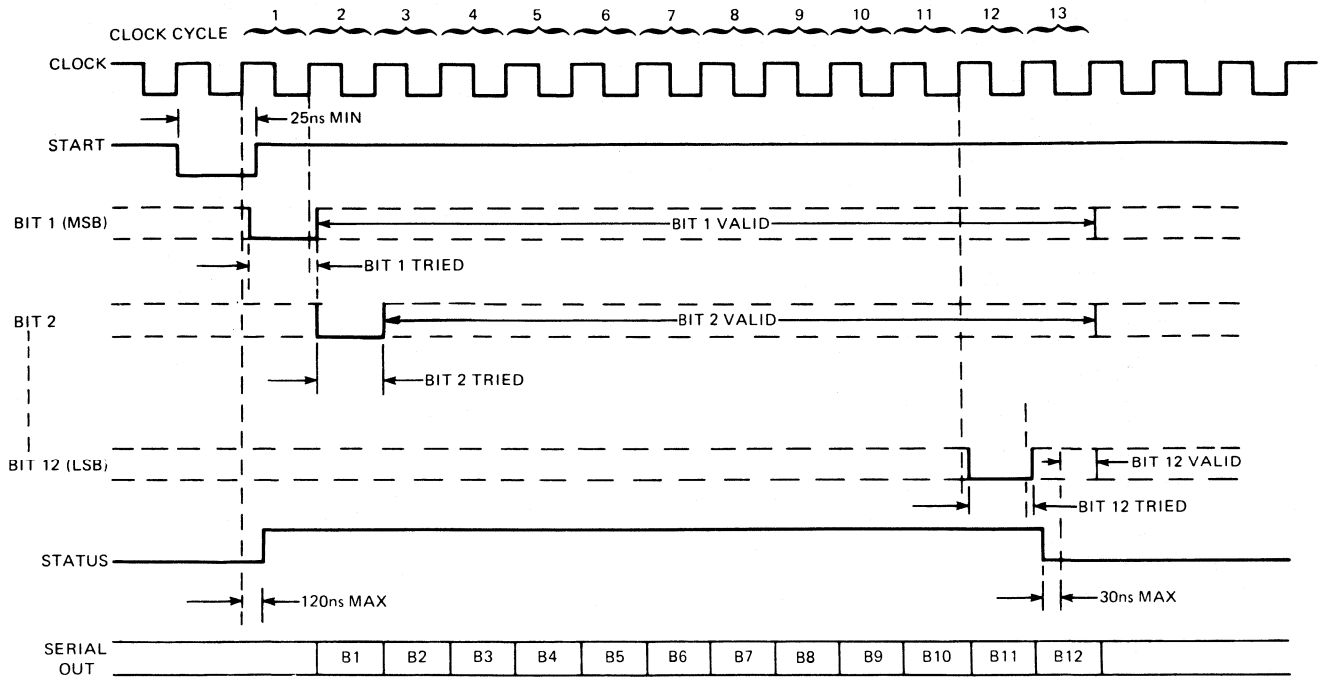


FIGURE 2. CONVERTER TIMING

ANALOG INPUT RANGE				DIGITAL CODING		
DDC 5200	DDC 5201	DDC 5202	DDC 5206	MSB		LSB
0.0000V	+5.0000V	+10.0000V	+10.0000V	0000	0000	0000
– 0.0024V	+4.9976V	+ 9.9951V	+ 9.9976V	0000	0000	0000
– 4.9976V	+0.0024V	+ 0.0049V	+ 5.0024V	0111	1111	1110
– 5.0000V	0.0000V	0.0000V	+ 5.0000V	0111	1111	1111
– 5.0024V	–0.0024V	– 0.0049V	+ 4.9976V	1000	0000	0000
– 9.9976V	–4.9976V	– 9.9951V	+ 0.0024V	1111	1111	1110
–10.0000V	–5.0000V	–10.0000V	0.0000V	1111	1111	1111

FIGURE 3. TYPICAL DIGITAL OUTPUT CODES

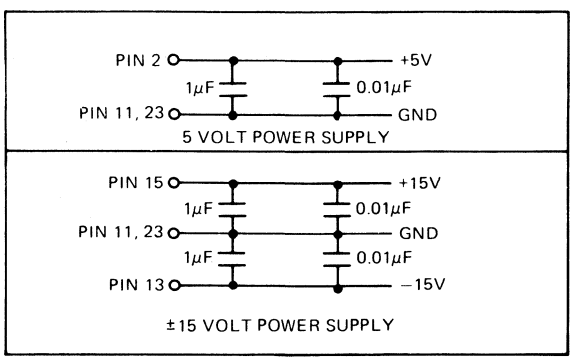


FIGURE 4. POWER SUPPLY DECOUPLING

DIGITAL OUTPUT CODING

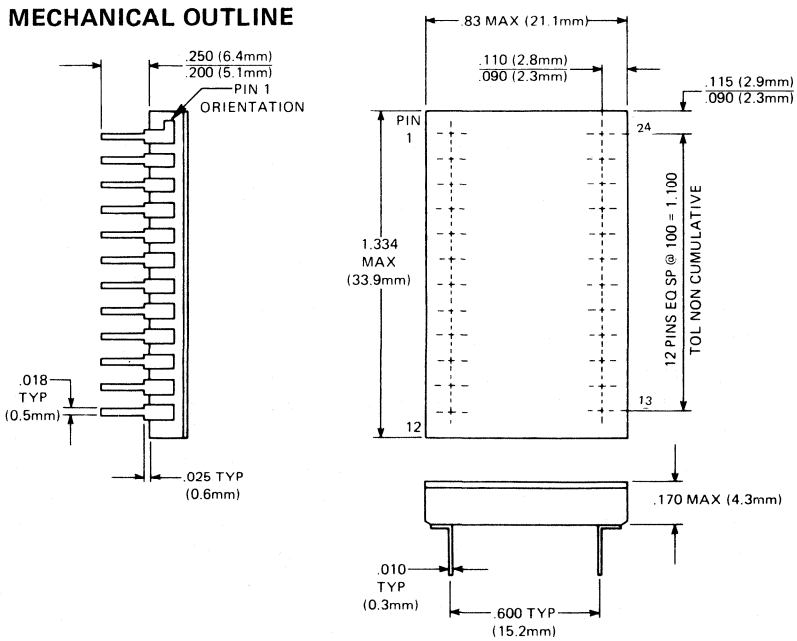
Figure 3 illustrates the digital output codes for typical analog inputs. Each column under the Analog Input Range heading represents a different input range of the DDC 5200 Series.

For example an analog input of +10.000 volts to the DDC 5202 results in a digital output code of 000---------0. For the DDC 5201, an analog input of –4.9976 volts will produce a digital output code of 11----------10.

POWER SUPPLY DECOUPLING

To insure full accuracy of the DDC 5200 Series converters it is advisable to adopt the power supply decoupling configuration illustrated in Figure 4. To optimize this decoupling technique the capacitors should be tantalum or electrolytic and located in close proximity to the converter.

MECHANICAL OUTLINE



PIN CONNECTION TABLE			
PIN	FUNCTION	PIN	FUNCTION
1	START CONVERT	13	–15V
2	+5V	14	ANA IN
3	SERIAL OUT	15	+15V
4	B6	16	(LSB) B12
5	B5	17	B11
6	B4	18	B10
7	B3	19	B9
8	B2	20	B8
9	(MSB) B1	21	B7
10	N/C	22	EOC
11	ANA GND	23	DIG GND
12	–V REF OUT	24	CLK INPUT

HYBRID PROCESSING

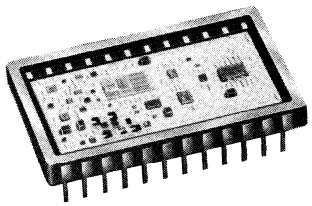
The DDC 5200 Series converters are manufactured to meet military standards for high reliability. They are built in accordance with requirements of MIL-STD-883 and the screening is based on Method 5008.

ORDERING INFORMATION

DDC 5200-1-883B

- MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883 DDC procedures (option 1 only)
  - Blank = Same, except pre burn in test and burn in are omitted
- Temperature Ranges
  - 1 = –55°C to +125°C
  - 3 = 0°C to +70°C
- Input Range
  - 00 = 0 to –10V
  - 01 = –5V to +5V
  - 02 = –10V to +10V
  - 06 = 0 to +10V

DDC
ILC DATA DEVICE CORPORATION



12 BIT 13μsec SUCCESSIVE APPROXIMATION A/D CONVERTER

DESCRIPTION

The DDC 5210 Series A/D Converters are 12 bit, high speed, successive approximation devices, in hermetically sealed 24 pin double DIP hybrid packages. All specifications are met with an externally applied 1 MHz clock, providing a conversion time of 13μsec. Functional laser trimming of a thin film resistor network results in extremely accurate and highly stable adjustment free converters (see Figure1). Linearity error is guaranteed to be better than 1/2 LSB, with no missing codes over the specified temperature range (see Specifications).

These converters are available in two unipolar and two bipolar input ranges and will operate with full accuracy at temperatures of 0°C to +70°C or −55°C to +125°C (consult Ordering Information). The DDC 5210 Series converters are form-fit-function replacements for the MN5210 Series A/D converters.

APPLICATIONS

Because of their high reliability, hermetically sealed package, low power consumption, wide temperature and dynamic range, the DDC 5210 Series will meet the most demanding military and industrial requirements. Typical applications include data acquisition systems, automatic test equipment and electronic countermeasures.

FEATURES

- *FORM-FIT-FUNCTION REPLACEMENT FOR MN5210 SERIES*
- *24 PIN, HERMETIC SEAL DOUBLE DIP HYBRID*
- *LOW POWER CONSUMPTION*
- *FAST, 13 μSEC CONVERSION TIME*
- *ADJUSTMENT FREE WITH ACCURACY TO ±0.05% FSR*
- *MEETS MIL-STD-883*

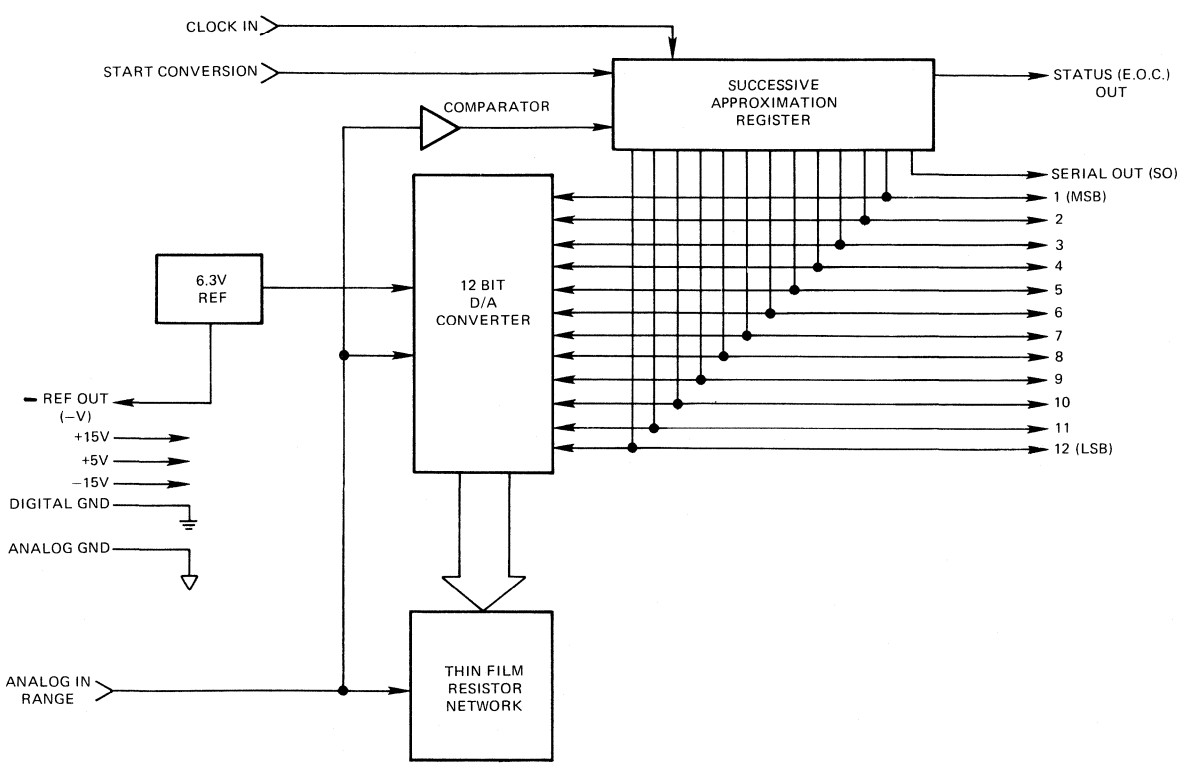


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Typical values at +25° C ambient temperature and nominal power supply voltages

PARAMETER	UNIT	VALUE			
ANALOG INPUTS		DDC 5210	DDC 5211	DDC 5212	DDC 5216
Input Ranges	V	0 to −10	−5 to +5	−10 to +10	0 to +10
Input Impedance	kΩ	6.7	6.7	13.4	13.4
Maximum without damage	V	±25	±25	±25	±25
RESOLUTION	bits	12			
ACCURACY AND DYNAMICS					
Linearity Error	LSB	TYP		MAX	
+25° C		±1/4		±1/2	
0° C to +70° C (−3)		±1/4		±1/2	
−55° C to +125° C (−1)				±1/2	
Differential Linearity Error	LSB	1/2			
No Missing Codes		Guaranteed over temperature			
Full Scale Absolute Accuracy Error					
+25° C	%FSR	±0.025		±0.05	
0° C to +70° C (−3)	%FSR	±0.2		±0.4	
−55° C to +125° C (−1)	%FSR			±0.4	
Zero Error					
+25° C	%FSR	±0.01		±0.025	
0° to 70° C (−3)	%FSR	±0.025		±0.05	
−55° C to +125° C (−1)	%FSR			±0.05	
Gain Error	%	±0.025			
Gain Drift	ppm/° C	±10			
Conversion Time	µs			13	
DIGITAL INPUTS		MIN	TYP	MAX	
Clock Input (External)					
High Pulse	ns	125			
Low Pulse	ns	175			
High Loading	µA		2	20	
Low Loading	mA		−0.25	−0.4	
Frequency	MHz			1	
Start Conversion Input					
High Loading	µA		4	40	
Low Loading	mA		−0.25	−0.4	
Setup Time	ns	25			
Logic Levels					
Logic "1"	V	2.0			
Logic "0"	V			0.7	
DIGITAL OUTPUTS					
Logic Coding					
Unipolar Ranges		Complementary Straight Binary			
Bipolar Ranges		Complementary Offset Binary			
Logic Levels		MIN	TYP	MAX	
Logic "1"	V	2.4	3.6		
Logic "0"	V		0.15	0.3	
Output Drive Capability					
Logic "1"	TTL Loads	8			
Logic "0"	TTL Loads	2			
REFERENCE OUTPUT		MIN	TYP	MAX	
Internal Reference					
Voltage	V		−6.3		
Accuracy	%		±2		
Drift Tempco	ppm/° C		±5		
Max External Current (without buffer)	µA			100	
POWER SUPPLIES					
Power Supply Range					
+15V Supply	%			±3	
+5V Supply	%			±5	
Power Supply Rejection					
+15V Supply	%FSR/%ps		±0.005	±0.02	
−15V Supply	%FSR/%ps		±0.01	±0.05	
Current					
+15V Supply	mA		+9	+13	
−15V Supply	mA		−20	−30	
+5V Supply	mA		+44	+54	
Power Consumption	mW		650	915	
PHYSICAL CHARACTERISTICS					
Size	in	1.3 X 0.8 X 0.2 (33.9 X 21.1 X 0.5mm)			
Weight	oz	0.2		(7g)	

TECHNICAL INFORMATION

The DDC 5210 Series A/D converters reset internal logic on a low to high clock transition, while the Start Conversion (pin 1) is low. The Start line must be low 25nsec. (min) prior to a low to high clock transition (see Figure 2). The converter will remain reset until the Start line is allowed to go high. Conversion commences upon the next low to high clock transition. Data is available 13 usec after the clock transition (commencing the conversion) occurs. A status (EOC) output signal (logic "1"), is presented on pin 22, at a maximum of 120 nsec after the Start line is driven low. Twelve bits are tried in succession, MSB through LSB, and serial data is immediately available on pin 3 during the conversion. Parallel data is available 30 nsec (max) after the Status (EOC) line returns to logic "0". Output data is held in the latch until another Start Conversion signal is input on pin 1. The drive capability of output data is two TTL loads. Continuous conversions may be accomplished by connecting the Status (EOC) output (pin 22) to the Start Conversion (pin 22).

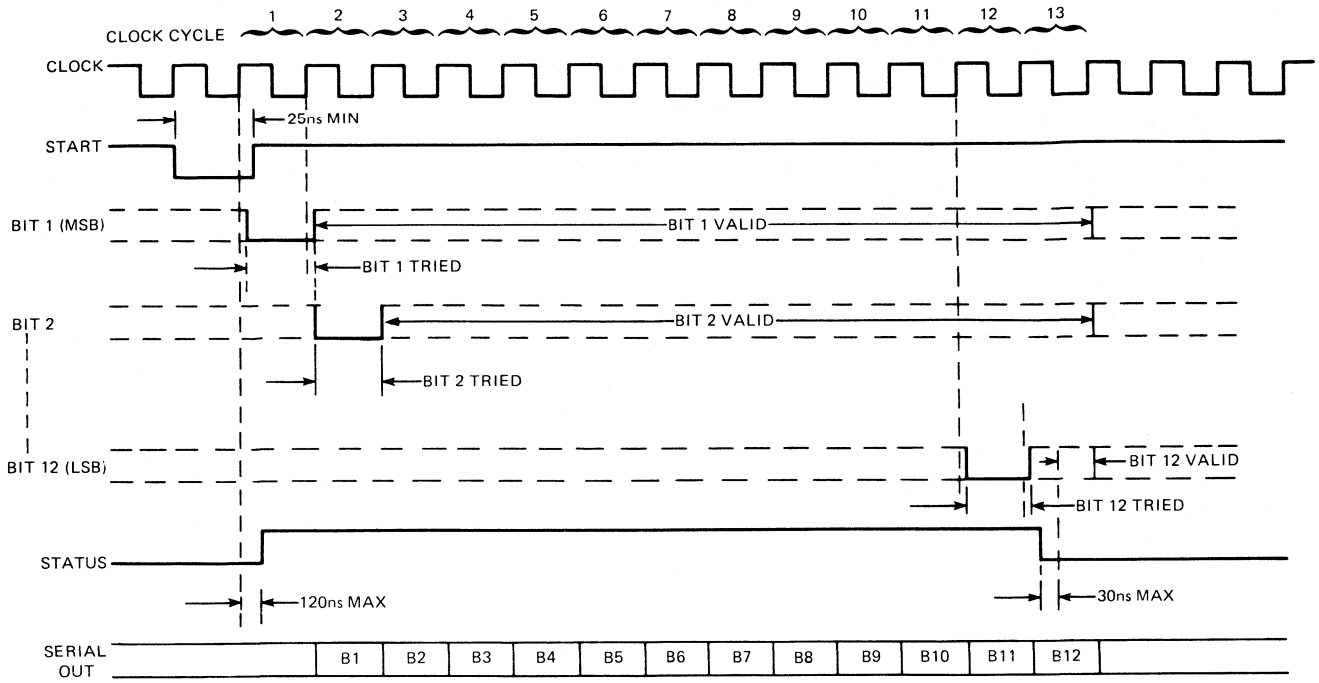


FIGURE 2. CONVERTER TIMING

ANALOG INPUT RANGE				DIGITAL CODING		
DDC 5210	DDC 5211	DDC 5212	DDC 5216	MSB		LSB
0.0000V	+5.0000V	+10.0000V	+10.0000V	0000	0000	0000
− 0.0024V	+4.9976V	+ 9.9951V	+ 9.9976V	0000	0000	0001
− 4.9976V	+0.0024V	+ 0.0049V	+ 5.0024V	0111	1111	1110
− 5.0000V	0.0000V	0.0000V	+ 5.0000V	0111	1111	1111
− 5.0024V	−0.0024V	− 0.0049V	+ 4.9976V	1000	0000	0000
− 9.9976V	−4.9976V	− 9.9951V	+ 0.0024V	1111	1111	1110
−10.0000V	−5.0000V	−10.0000V	0.0000V	1111	1111	1111

FIGURE 3. TYPICAL DIGITAL OUTPUT CODES

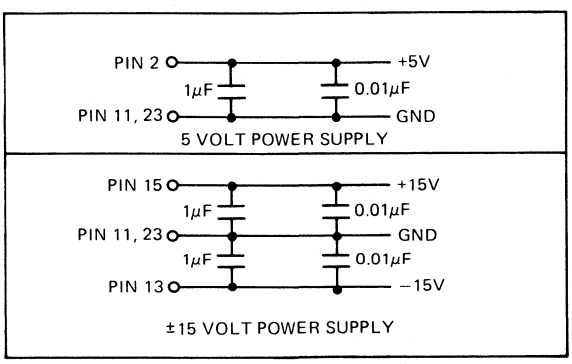


FIGURE 4. POWER SUPPLY DECOUPLING

DIGITAL OUTPUT CODING

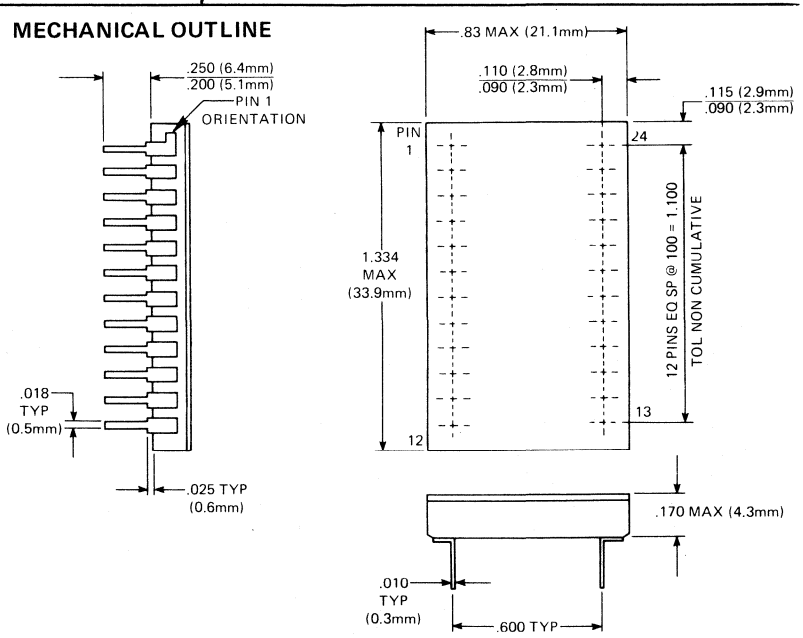
Figure 3 illustrates the digital output codes for typical analog inputs. Each column under the Analog Input Range heading represents a different input range of the DDC 5210 Series.

For example an analog input of +10.000 volts to the DDC 5212 results in a digital output code of 000----------0. For the DDC 5211, an analog input of −4.9976 volts will produce a digital output code of 11----------10.

POWER SUPPLY DECOUPLING

To insure full accuracy of the DDC 5210 Series converters it is advisable to adopt the power supply decoupling configuration illustrated in Figure 4. To optimize this decoupling technique the capacitors should be tantalum or electrolytic and located in close proximity to the converter.

MECHANICAL OUTLINE



PIN CONNECTION TABLE			
PIN	FUNCTION	PIN	FUNCTION
1	START CONVERT	13	–15V
2	+5V	14	ANA IN
3	SERIAL OUT	15	+15V
4	B6	16	(LSB) B12
5	B5	17	B11
6	B4	18	B10
7	B3	19	B9
8	B2	20	B8
9	(MSB) B1	21	B7
10	N/C	22	EOC
11	ANA GND	23	DIG GND
12	–V REF OUT	24	CLK INPUT

HYBRID PROCESSING

All DDC 5210 hybrid converter products are manufactured to meet military standards for high reliability. These products are built in accordance with requirements of MIL-STD-883 and the screening is based on Method 5008.

ORDERING INFORMATION

DDC 5210-1-883B

- MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883 DDC procedures (option 1 only)
  - Blank = Same, except pre burn in test and burn in are omitted
- Temperature Ranges
  - 1 = –55°C to +125°C
  - 3 = 0°C to +70°C
- Input Range
  - 10 = 0 to –10V
  - 11 = –5V to +5V
  - 12 = –10V to +10V
  - 16 = 0 to +10V

DDC
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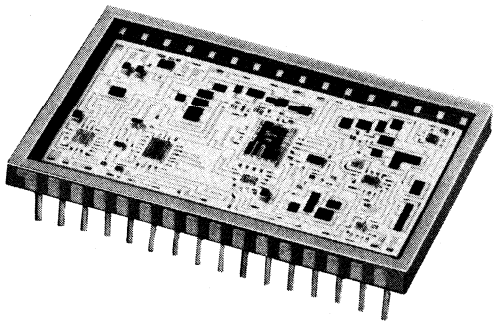
12 BIT 5 μSEC HYBRID A/D CONVERTER
Industry Standard Pin Out



DESCRIPTION

The DDC-5240 is a 12 bit 5μsec A/D converter packaged in a hermetically sealed ceramic 32 TDIP. It is a pin for pin replacement for MN5240 types, and a higher speed replacement for ADC85 and ADC-HZ12B. Offering wide operating temperature (–55° C to +125°C) and low power dissipation (1.6 watts), the DDC-5240 is available screened to MIL-STD-883B. It also features internal clock and both serial and parallel data outputs.

APPLICATIONS

With its high reliability (1,600,000 hour MTBF), wide operating temperature, low power and small hermetic package, the DDC-5240 meets the most demanding military and industrial requirements. Typical applications include data acquisition systems, automatic test equipment and EW systems.

FEATURES

- *PIN FOR PIN REPLACES MN5240 TYPES*
- *HIGH SPEED REPLACEMENT FOR ADC85 AND ADC-HZ12B TYPES*
- *–55°C TO +125°C OPERATING TEMPERATURE*
- *LOW POWER DISSIPATION –1.6 W*
- *MIL-STD-883B SCREENING AVAILABLE (1,600,000 HOUR MTBF)*

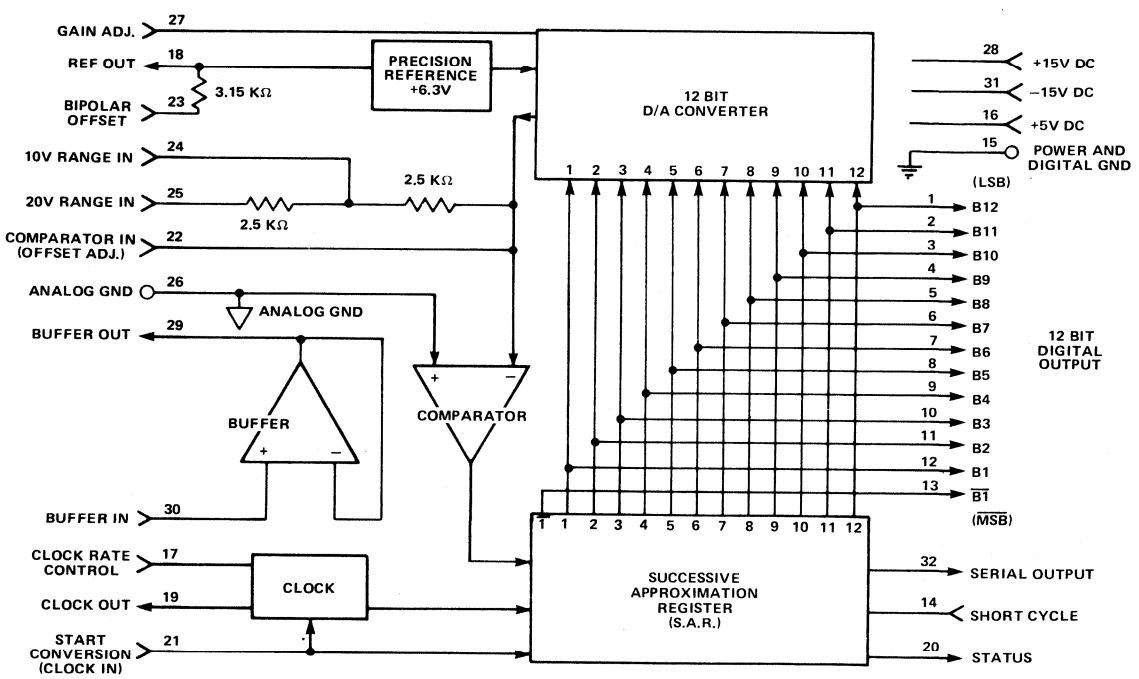


FIGURE 1. DDC-5240 BLOCK DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION AND BLOCK DIAGRAM

The main elements of the DDC-5240 as shown in the block diagram, Figure 1, are a voltage comparator, a 12 bit successive approximation register (S.A.R.), and a 12 bit digital to analog converter connected in a closed loop. The analog input and the D/A converter output are superimposed at the sum point of the comparator. Successive approximation is used to make the D/A output equal to the analog input. Conversions are initiated by an external START CONVERSION pulse, and a STATUS logic output indicates when a conversion has been completed and output data is available.

The 10V RANGE INPUT or 20V RANGE INPUT is connected to the analog input (depending on scaling) and the BIPOLAR OFFSET is used to select unipolar or bipolar operation. An input buffer amplifier is provided for higher input impedance, but its use has been made optional. The buffer amplifier must be allowed to settle before a conversion can be initiated.

The rate of the internal clock is determined by the voltage provided at the CLOCK RATE CONTROL input. When this input is connected to +5V the internal clock rate is appropriate for the full accuracy 12 bit converter. However, it may be necessary to adjust the voltage to obtain the optimum clock rate.

The conversion rate can be increased by truncating the conversion at 10 or 8 bits using the SHORT CYCLE pin. Short cycling allows the clock to be speeded up. The internal clock rate can be increased by applying a more positive voltage to the CLOCK RATE CONTROL, thereby increasing the conversion rate still further. It is also possible to use an external clock.

There are two grounds in the system. The analog ground for the analog input signal is designated by ⏚. The power supply ground, designated by ⏚, is also used as a ground for all logic signals. To minimize crosstalk, the analog and power grounds are not connected internally. They should be connected as directly as possible externally, preferably with a ground plane beneath the module.

INPUT SCALING AND OUTPUT CODING

There are five input voltage ranges, with pin connections as shown in Figure 2, Connections for Normal Operation. For unipolar input (ranges 0 to +5V or 0 to +10V) the output coding using bits 1 through 12 is complementary offset binary. For bipolar input (ranges ±2.5V, ±5V, or ±10V) the output coding is either complementary straight binary using bits 1 through 12, or complementary two's complement if bits 2 through 12 and bit 1 (the MSB complement) is used. The coding is described by the transition table in Figure 3. The analog input voltage levels shown in the left hand column should correspond to the transition points between the digital codes shown at the right.

SPECIFICATIONS
Typical values at +25°C case temperature and nominal power supply voltages.

PARAMETER	UNITS	VALUE			
		10 BIT LIN		12 BIT LIN	
		TYP	MAX	TYP	MAX
RESOLUTION	Bits		12		12
ACCURACY AND DYNAMICS					
Linearity Error					
−3 Temp Range	LSB		±2		±1/2
−1 Temp Range	LSB		±2		±1
Absolute Accuracy					
Unipolar +25°C	% F.S.R.	±0.1	±0.5	±0.1	±0.3
−3 Temp Range	% F.S.R.	±0.2	±0.6	±0.2	±0.4
−1 Temp Range	% F.S.R.	±0.2	±0.7	±0.2	±0.5
Bipolar +25°C	% F.S.R.	±0.15	±0.6	±0.15	±0.4
−3 Temp Range	% F.S.R.	±0.2	±0.7	±0.2	±0.5
−1 Temp Range	% F.S.R.	±0.2	±0.8	±0.2	±0.6
OFFSET					
Unipolar +25°C	% F.S.R.	±0.05	±0.10	±0.05	±0.10
−3 Temp Range	% F.S.R.	±0.07	±0.12	±0.07	±0.12
−1 Temp Range	% F.S.R.	±0.07	±0.12	±0.07	±0.12
Bipolar +25°C	% F.S.R.	±0.10	±0.20	±0.10	±0.20
−3 Temp Range	% F.S.R.	±0.15	±0.25	±0.15	±0.25
−1 Temp Range	% F.S.R.	±0.15	±0.25	±0.15	±0.25
Conversion Time	μsec		5		5
Cycle Time	μsec		5.25		5.25
ANALOG INPUTS					
Input Ranges					
Unipolar	V	0 to +5; to +10			
Bipolar	V	±2.5; ±5; ±10			
Max Voltage Without Damage	V	Two times full scale range			
Impedance (Direct Input)					
0 to +5V and ±2.5V	KΩ	1.25 typ			
0 to 10V and ±5V	KΩ	2.5 typ			
±10V	KΩ	5 typ			
Buffer Amplifier					
Impedance	MΩ	100min			
Bias Current	nA	100 typ; 250 max			
Settling Time (to .01% for 20V step)	μs	2 typ			
DIGITAL INPUT/OUTPUT (TTL COMPATIBLE)					
12 Bit Parallel Output		Positive logic, bits 1 through 12 plus MSB complement Drive capability 5 std TTL loads Unipolar coding; Complementary Binary Bipolar coding; Complementary Offset Binary or Complementary Two's Complement			
Serial Data Output		Non return to zero (NRZ); drive capability and coding same as for parallel output			
Start Conversion Input		Positive pulse, 50 ns min, trailing edge initiates conversion Loading is 1 std TTL load			
Status		Logic "1" during conversion; drops to "0" to indicate parallel data is available Drive capability is 2 std TTL loads			
Internal Clock Output		Train of 13 positive pulses initiated by the Start Conversion trailing edge Drive capability is 2 std TTL loads Clock Frequency can be changed by pin programming or by external potentiometer adjustment			
INTERNAL PREFERENCE OUTPUT					
Voltage Level	V	+6.3 ±5%			
Current	mA	0.2 max for no degradation in specifications			
Voltage Tempco	ppm/°C	±10 typ			

PARAMETER	UNITS	VALUE		
POWER SUPPLIES				
Supply Voltages	V	+15 ±5%	−15 ±5%	+5 ±5%
Max Voltage Without Damage	V	+18	−18	+7
Current	mA	40 typ 50 max	30 typ 45 max	110 typ 150 max
Power Supply Sensitivity	%FSR/%PS	±0.002	±0.002	±0.001
THERMAL CHARACTERISTICS				
Temperature Ranges (Case)				
Operating				
−1 Option	°C	−55 to +125		
−3 Option	°C	−25 to +85		
Storage	°C	−55 to +135		
Thermal Impedances				
Case to Air	°C/Watt	θ_{CA} = 15		
Junction to Case	°C/Watt	θ_{JC} = 2		
PHYSICAL CHARACTERISTICS				
Type of Package		Ceramic case, hermetically sealed, 32 pin triple DIP		
Size	inches	1.75 x 1.15 x 0.22 (4.45 x 2.92 x 0.56 cm)		
Weight	oz	0.67 typ (19g)		

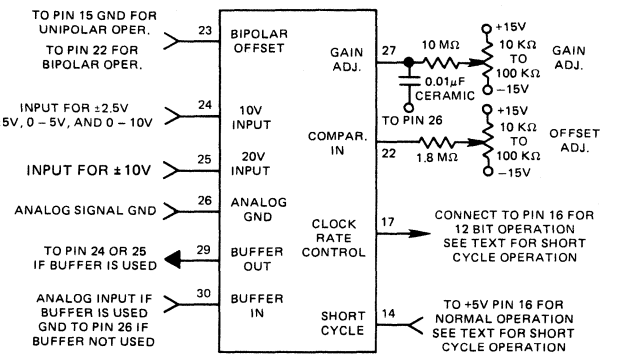


FIGURE 2. CONNECTIONS FOR NORMAL OPERATION

TIMING DIAGRAM AND EXTERNAL CLOCK

The timing for normal 12 bit operation of the DDC-5240 is shown in Figure 4. The trailing edge of the START CONVERSION pulse starts the conversion by initiating the first of the 13 equal positive pulses of the internal clock. The leading edge of the first clock pulse then causes the STATUS to go to logic "1" and also causes the first bit to be tried. The leading edge of the second clock pulse causes Bit 2 to be tried, and Bit 1 then becomes valid. The twelfth clock pulse causes Bit 12 to be tried. Bit 12 becomes valid after the leading edge of the clock pulse 13, and the STATUS then drops to logic "0" to indicate that the conversion has been completed.

The SERIAL DATA OUTPUT is a non return to zero type (NRZ). Data for each bit becomes valid at the same time as the corresponding parallel data for the same bit, and remains valid for one clock cycle. A recommended way to clock data from the SERIAL OUTPUT is to use the trailing edge of each clock pulse to shift the data into a twelve bit shift register.

An EXTERNAL CLOCK can also be used as indicated in Figure 4. If the START CONVERSION input is at logic "1" at a time when any internal clock would normally be initiated, the clock is turned off and neither that pulse nor subsequent pulses will exist. Because of this feature an external clock with negative pulses can be applied to the Start Conversion input, pin 21. The leading edge of the first negative external clock pulse turns on the internal clock and Bit 1 is tried. If the external clock pulse is shorter than 200 ns, the Start Conversion input will be at logic "1" at the time when the second internal clock would normally be initiated, so the internal clock will turn off. The external clock is then free to initiate the trial of Bit 2 at any time. The only limitation on the rate of the external clock is that it must be no faster than twice the rate of the internal clock. The clock rate control could be used to adjust the internal clock rate to meet this criterion.

SHORT CYCLING AND CLOCK RATE CONTROL

The minimum conversion time and minimum cycle time depend on the number of bits tried and on the clock period. The clock period must be long enough to allow the comparator to settle out.

The number of bits tried can be reduced for both units by changing the SHORT CYCLE pin connection. Pin 14 is connected to the next higher bit than the number of bits to be tried. For instance, for 10 bits, connect pin 14 to pin 2 (bit 11). For 8 bits, connect pin 14 to pin 4 (bit 9).

When fewer bits are tried, it is possible to increase the clock rate because less accuracy is required. For full 12 bit operation when no particular or optimum conversion time is required, the Clock Rate Control, pin 17, is usually connected as shown in Figure 2. In the same way, when rates are not critical, pin 17 can be connected to +10V for 10 bit operation and +15V for 8 bit operation. Optimum clock rates will generally require fine adjustment of the clock voltage. The approximate clock rates with the three standard voltage levels are:

PIN 17 Voltage	Approximate Clock Rate
0V	1.8 MHz
+5V	2.6 MHz
+15V	4.0 MHz

If both short cycling and pin-programmed clock rate control are used to increase the conversion rate, the following nominal conversion times are obtained for 10 and 8 bits:

Resolution	Pin 17 Voltage	Conversion Time
12 Bits	+5V	5μs
10 Bits	+10V	3μs
8 Bits	+15V	2μs

TRANSITION VALUE		DIGITAL BIT OUTPUTS											
UNIPOLAR	BIPOLAR	MSB											LSB
COMPLEMENTARY BINARY	COMPLEMENTARY OFFSET BINARY	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12
+F.S. – 3/2 LSB	+F.S. – 3/2 LSB	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
+3/4 F.S. – 1/2 LSB	+1/2 F.S. – 1/2 LSB	0 0	0 1	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
+1/2 F.S. + 1/2 LSB	+ 1/2 LSB	0 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	0 1
+1/2 F.S. – 1/2 LSB	–1/2 LSB	0 1	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
+1/4 F.S. +1/2 LSB	–1/2 F.S. + 1/2 LSB	1 1	0 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	0 1
+3/2 LSB	–F.S. + 3/2 LSB	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	0 1	1 0
+1/2 LSB	–F.S. + 1/2 LSB	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	0 1

3A. Theoretical transition values for Complementary Binary and Complementary Offset Binary coding. For Complementary Two's Complement coding, all values are the same as for Complementary Offset Binary, except that the MSB is reversed (MSB bits "0" become "1" and "1" become "0").

VOLTAGE RANGE	FULL SCALE (VOLTS)	1/2 LSB (VOLTS)
±2.5V	2.50000	0.00061
±5V	5.00000	0.00122
±10V	10.00000	0.00244
0 – 5V	5.00000	0.00061
0 – 10V	10.00000	0.00122

3B. Full Scale (F.S.) and 1/2 LSB for 12 bit accuracy.

FIGURE 3. THEORETICAL TRANSITION VALUES

The clock rates and conversion times listed are nominal values. To adjust the clock rate accurately, pin 17 may be connected to a voltage divider as shown in Figure 5. R is a multi-turn trim potentiometer with a tempco of ±100 ppm/°C or less.

Note that if the clock rate is increased to a value greater than that specified for the number of bits required, the linearity error will be substantially increased.

The CLOCK RATE CONTROL can also be connected to negative voltages as large as –15V, and this will decrease the clock rate.

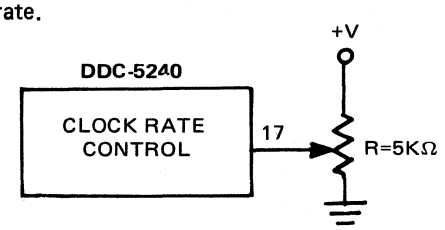


FIGURE 5. OPTIONAL CLOCK RATE FINE ADJUSTMENT

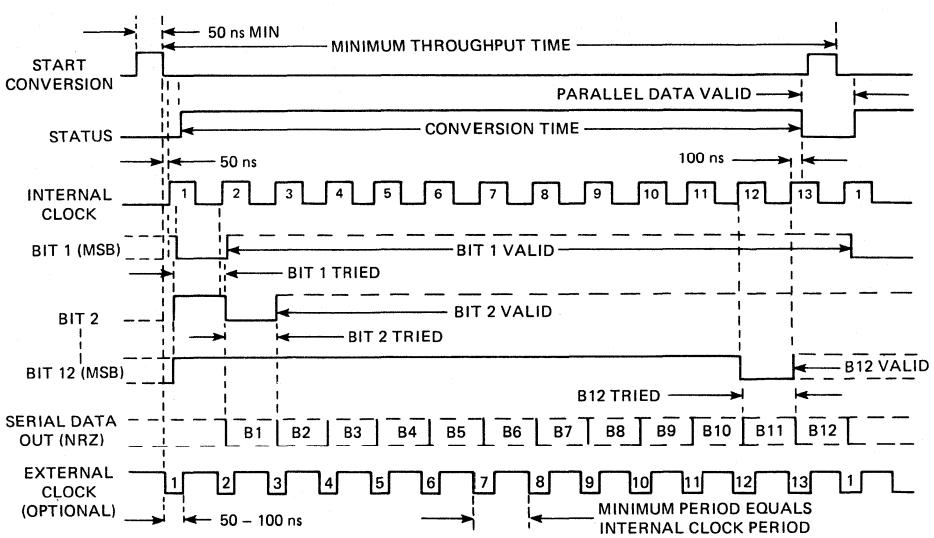


FIGURE 4. DDC-5240 TIMING DIAGRAM

OFFSET AND GAIN TRIM

The gain and offset of the DDC-5240 are factory trimmed to the values listed in the specifications table. Both errors can be trimmed to zero in the final application by using the potentiometer adjustment circuits shown in Figure 2.

To reduce noise, the GAIN ADJUST, pin 27, should be bypassed with a 0.01μF ceramic capacitor to analog ground as shown in Figure 2 even if no gain trim potentiometers are installed.

ACCURACY TESTING

The accuracy of the DDC-5240 is specified by its linearity error, gain, offset, and differential linearity.

The arrangement shown in Figure 6 may be used to measure the bit transitions. Offset trim, gain trim, and other standard connections are not shown. Shielded twisted pair cable is used to connect the Precision Voltage Standard, and each of the twelve bits requires its own LED indicator. The inverting register is used to increase the duty cycle of the LSB bits since they are held at logic "1" during most of the timing cycle as indicated in the timing diagram. The NOT outputs ($\overline{Q}$) from the register are used so that a lighted LED will represent logic "1" Readings should be taken with the converter energized, in thermal equilibrium at 25°C, and after a warm-up time of 5 minutes. The Pulse Generator can be set at any frequency up to the maximum allowed for the converter. The power supply voltages should be at their nominal values.

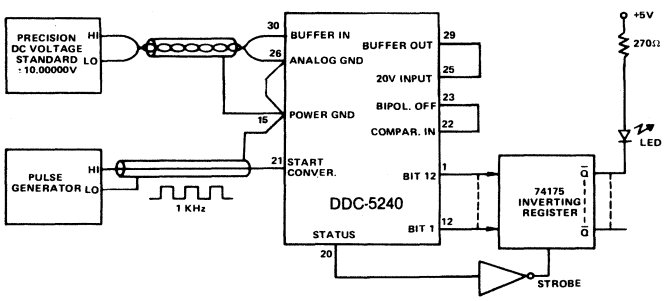


FIGURE 6. CIRCUIT TESTING ACCURACY

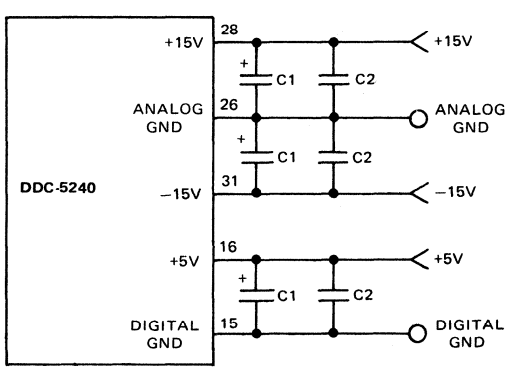


FIGURE 7. POWER SUPPLY DECOUPLING CAPACITORS

The suggested test procedure is as follows:

(1) Trim the offset by sweeping the input through the transition at −FS + 1/2 LSB in the transition value table, Figure 3. Adjust the Offset potentiometer until there is a 50% dither of the LSB.

(2) Trim the gain by sweeping the input through the transition at all bits ON in Figure 3 (+FS + 3/2 LSB for bipolar coding). Adjust the Gain potentiometer for a 50% dither of the LSB.

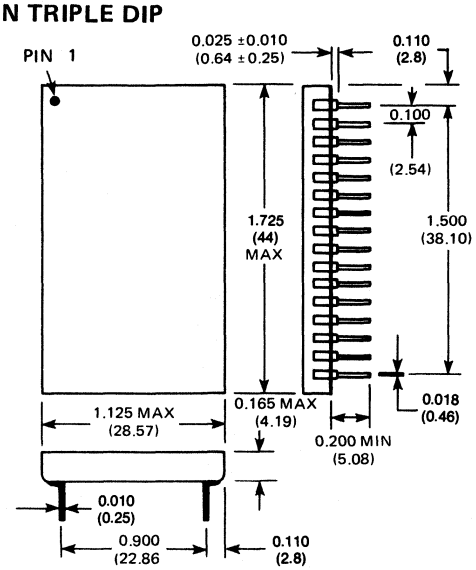
(3) Repeat steps (1) and (2) in case there is a slight interaction between the offset and gain trims.

(4) Measure the input voltage levels at which other transitions occur. The differences between these voltages and the theoretical values will be within ±1/2 LSB.

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	17	CLOCK RATE CNTL
2	BIT 11	18	REF. OUT (+6.3V)
3	BIT 10	19	CLOCK OUT
4	BIT 9	20	STATUS
5	BIT 8	21	START CONVERT
6	BIT 7	22	COMPARATOR IN
7	BIT 6	23	BIPOLAR OFFSET
8	BIT 5	24	10V RANGE
9	BIT 4	25	20V RANGE
10	BIT 3	26	ANALOG GND
11	BIT 2	27	GAIN ADJ
12	BIT 1 (MSB)	28	+15 SUPPLY
13	$\overline{\text{BIT 1 (MSB)}}$	29	BUFFER OUT
14	SHORT CYCLE	30	BUFFER IN
15	DIG. GND	31	−15V SUPPLY
16	+5V SUPPLY	32	SERIAL OUT

MECHANICAL OUTLINE
32 PIN TRIPLE DIP



NOTES:
1. Dimensions shown are in inches, (millimeters)
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with capacitors as shown in Figure 7 to assure noise free operation. These capacitors should be located as close to the converter as possible. The 0.01μF ceramic capacitors imporve high frequency performance.

RELIABILITY

The use of MSI and thin film resistance networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All DDC-5240 hybrid converter products are manufactured to meet military standards for high reliability. DDC hybrids are built in conjunction with the requirements of MIL-STD-883 Test Methods and Procedures for Microelectronics. The screening procedures are based on Methods 5004/5008 except for burn-in, which is optional. Preburn-in may be included by adding-883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn-in) is 1,600,000 hours, Ground Fixed, at 25°C.

ORDERING INFORMATION

DDC-5240–12–1–883B

- MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883, DDC procedures.
  - Blank = Same, except burn-in is omitted.
- Temperature Range (Case):
  - 1 = –55°C to +125°C
  - 3 = –25°C to +85°C
- Linearity:
  - 12 = 12 bits (±.012% F.S.R.)
  - 10 = 10 bits (±.048% F.S.R.)

SECTION B

D/A CONVERTERS

SUMMARY TABLE

1. FIXED REFERENCE D/A CONVERTERS

Name	Form Factor	Resolution	Linearity Error (max)	Settling Time (typ to ±1/2 LSB) F.S. Output Change	Settling Time (typ to ±1/2 LSB) ±LSB Change	Features	Page
ADH-0301l	24 pin DDIP hybrid	12 bits	±0.0125% F.S.R. ±0.05% F.S.R.	35 ns (I)	20 ns (I)	Low glitch: 2.5 mA·ns Very fast settling.	58
DAC-02900	24 pin DDIP hybrid	16 bits	±0.0008% F.S.R.	15 μs	3 μs	Small hermetic HI REL hybrid with 10V F.S. output, 6.4V precision internal Reference.	63
DDC-1250	24 pin DDIP hybrid	12 bits	±0.012% F.S.R.	35 ns (I)	20 ns (I)	Fast settling Low glitch. Pin for pin replaces HDS 1250.	65
DDAC	2 or 3 hybrids or P.C. Board	13 bits	±0.0125% F.S.R. ±0.025% F.S.R. ±0.05% F.S.R.	600-1800 ns (V)	75-100 ns (V)	Deglitched: 750 mV·ns glitch energy. 10 MHz update rate. Optional cable driver.	69
DAC-8528	24 pin DDIP hybrid	12 bits	±0.0125% F.S.R. ±0.025% F.S.R.	60 ns (I) 1000 ns (V)	20 ns (I) 50 ns (V)	Low glitch: 3 mA·ns or 2500 mV·ns glitch energy. Fast settling.	77
DAC-SL	24 pin DDIP hybrid	12 bits	±0.0125% F.S.R. ±0.025% F.S.R.	5 us (V)	1.5 us (V)	Digital input register with strobe.	81
DDC DAC87	24 pin DDIP hybrid	12 bits	±0.0125% F.S.R.	100 ns (I) 3 μs (V)	50 ns (I) 1.5 μs (V)	Low cost HI REL version of DAC87. Fast settling.	85
SDAC and 2615	24 pin DDIP hybrid	13 bits	±0.0125% F.S.R. ±0.025% F.S.R. ±0.05% F.S.R.	50 ns (I) 500-1600 ns (V)	30 ns (I) 200-600 ns (V)	Fast settling. No trim adjustments.	90

2. MULTIPLYING D/A CONVERTERS

Name	Form Factor	Resolution	Linearity Error (max)	Ref Voltage	Full Scale Settling Time to ±1/2 LSB	Features	Page
DAC-02701	24 pin DDIP hybrid	12 bits	±0.05% F.S.R. over temp range	±10 VDC DC to 10KHz	25 μsec	Double buffered latches. 12 bit data transfer. ±10 volt output.	94
DAC-M	Encapsulated module 3.1 x 2.6 x o.4"	15 bits	±0.003% F.S.R.	±10 VDC DC to 10 KHz	Reference 10 μs max Digital 5 μs max	4 quadrant. Very high accuracy. Differential input, remote ground. Low feed through capacitance. No trim required.	98

ADDENDUM

DAC-02310	32 Pin TDIP hybrid	14 Bit	±0.006% F.S.R.	600 ns (V)	50 ns	14 bit deglitched D/A converter with 10MHz update rate, pin programmable output ranges and 10mV peak to peak glitch voltage.	A-2

BACKGROUND INFORMATION

INTRODUCTION

DDC's digital to analog converters are divided into two categories. The Fixed Reference D/A Converters are calibrated with a fixed internal reference voltage, and provide a current output and/or voltage output determined by the digital input word. The Multiplying D/A converters listed in this catalog will accept an external reference, and provide a voltage output equal to the product of the reference voltage and the fraction represented by the digital word. In addition to high speed and high resolution, DDC offers fixed reference D/A converters with very low glitch and pin-programmable current and/or voltage ranges. One converter includes a track/hold deglitch and cable driver, and one has a strobed input register. The 13 to 15 bit multiplying D/A converters all have 4 quadrant operation and an output common-mode rejection capability, and will provide full rated accuracy from DC to 400 Hz.

All of DDC's D/A converters include a resistance network and switches which together provide a current output. The simplest concept of a D/A converter is shown in Figure 1. The resistance network produces a series of binary weighted currents. These are connected to the output by switches controlled by the digital input. The summed current is available directly as an output current I_{OUT} or is transformed by an op-amp into a voltage output V_{OUT}. The chief requirements for the converter are linearity (which depends on the bit current ratios), scale factor accuracy and low offset drift.

A difficulty with the arrangement in Figure 1 is that turning the bit currents off and on changes voltages in the resistance network and so may affect stability. This problem is eliminated by an arrangement such as shown in Figure 2 where the resistor currents are constant because they are switched either to actual ground or to the virtual ground of an op-amp.

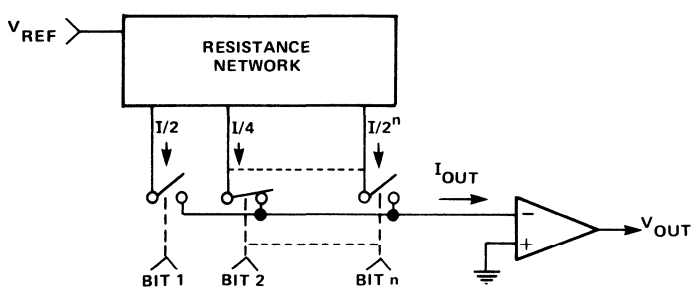


FIGURE 1. BASIC D/A DIAGRAM

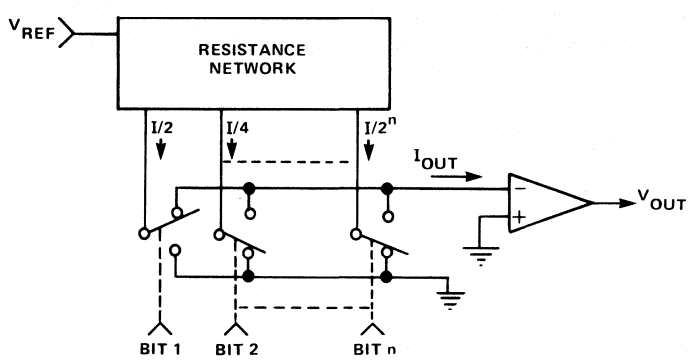


FIGURE 2. ARRANGEMENT WITH CONSTANT RESISTOR CURRENTS

There are many other possible types of resistance networks and switching arrangements. Currents, for instance, can be switched as equal currents before they are given binary weighting by the network, as shown in Figure 3. The method chosen for a particular D/A converter depends on the best compromise of characteristics and cost.

For a multiplying D/A converter, the output current must remain proportional to the reference voltage without saturation effects over an acceptable range of bipolar input voltages (usually ±10V) and frequencies. Otherwise, multiplying and fixed reference D/A converters are quite similiar in basic design concepts.

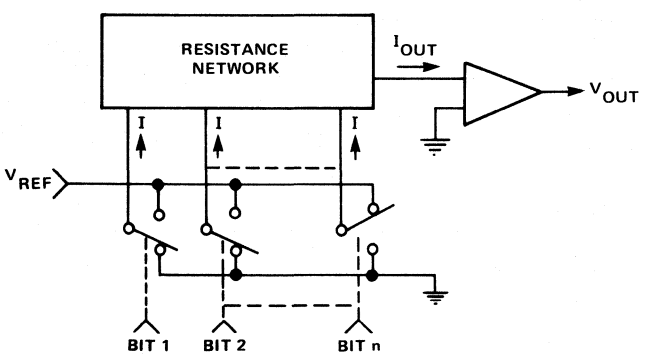


FIGURE 3. ANOTHER D/A ARRANGEMENT

TRANSFER CHARACTERISTICS AND ACCURACY

The transfer characteristics of a D/A converter will be discussed in terms of a 3 bit converter with straight binary and offset binary coding. The difference between these two codings is just an analog offset equal to one half of full scale. This offset is generally pin programmable in converters which offer both unipolar and bipolar coding.

For a D/A converter, analog output values such as 1 LSB, 2 LSB etc. should coincide with the input bit codes. This is shown by the ideal transfer characteristic for a 3 bit D/A converter illustrated in Figure 4. For straight binary coding, for instance, the 0 LSB output level coincides with 000 and the 1 LSB level coincides with 001. Intermediate values of analog output should not exist except as brief transitions while a code change occurs.

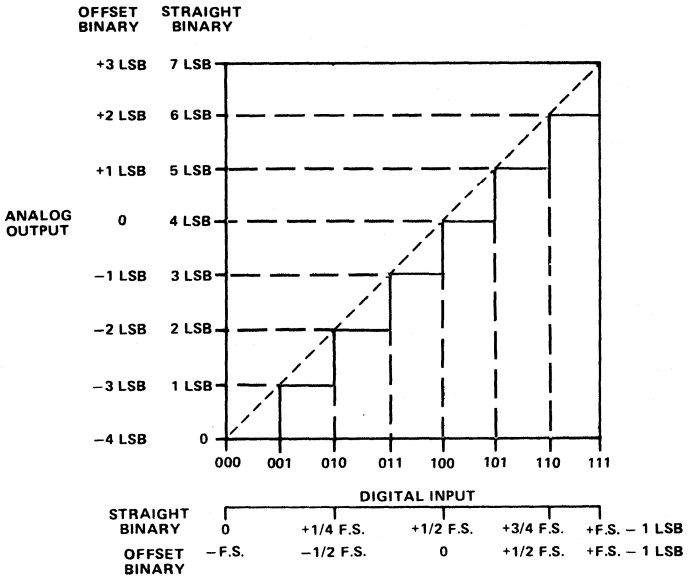


FIGURE 4. IDEAL TRANSFER CHARACTERISTIC FOR A 3 BIT D/A CONVERTER

It can be seen from Figure 4 that the largest analog output obtained in both straight and offset binary coding is F.S. − 1 LSB. In some converters with offset binary coding the output is offset by 1 LSB so that the largest positive value is F.S. and the largest negative value is −F.S. + 1 LSB. The bit table equivalent to the transfer characteristic in Figure 4 is shown in Figure 5.

The accuracy of a D/A converter is measured by determining the analog output for each input digital code. The total error is the sum of the offset error, the gain error, and the linearity error.

For a unipolar converter the offset is usually specified to be at the code for zero analog output, but it could be designated by the manufacturer to be at the code at either end of the range. For a bipolar converter, the offset could also be assigned to the code for zero output near the center of the range. The offset error is the difference between the measured and the theoretical output value at the code designated for offset.

ANALOG OUTPUT		DIGITAL CODE		
Unipolar Straight Binary	Bipolar Offset Binary	(MSB) Bit 1	Bit 2	(LSB) Bit 3
+ F.S. − 1 LSB	+ F.S. − LSB	1	1	1
+ 3/4 F.S.	+ 1/2 LSB	1	1	0
+ 1/2 F.S. + 1/2 LSB	+ 1 LSB	1	0	1
+ 1/2 F.S.	0	1	0	0
+ 1/2 F.S. − 1 LSB	− LSB	0	1	1
+ 1/4 F.S.	− 1/2 F.S.	0	1	0
+ 1 LSB	− F.S. + 1 LSB	0	0	1
0	− F.S.	0	0	0

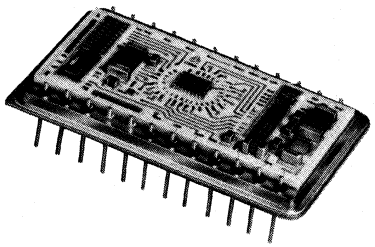
FIGURE 5. BIT TABLE FOR 3-BIT D/A CONVERTER

The gain error is measured at the codes at opposite ends of the range. The gain is equal to the difference between the measured outputs at these two codes (keeping negative signs for negative output), divided by the theoretical output span between them. For the 3 bit converter just discussed, the input span is F.S. − 1 LSB for unipolar coding, and 1 F.S. − 1 LSB for bipolar coding.

The linearity is obtained by determining the difference between the measured and theoretical output at all other codes. Before substracting the theoretical value, the measured value at each point must be corrected by first substracting the offset error and then multiplying by the gain correction. The calculations are greatly simplified if the converter offset and gain errors are both trimmed to zero before linearity is measured.

Monotonicity is usually also required. If the converter is monotonic, the analog output will never decrease if the digital code increases, and will never increase if the digital code decreases. All DDC converters are monotonic.

12 BIT 35 NSEC HYBRID D/A CONVERTER
High Reliability; One Monolithic Active Component



FEATURES

- *FAST: 35 NSEC SETTLING*
- *HIGH RELIABILITY: 3,000,000 HOUR MTBF*
- *LOW GLITCH: 50 MV • NSEC*
- *–55° to +125°C OPERATING TEMPERATURE*
- *HERMETICALLY SEALED 24 DDIP PACKAGE*

DESCRIPTION

The Monobrid ADH-030 II is a 12 bit 35 nanosecond hybrid D/A converter packaged in a hermetically sealed 24 DDIP. It pin for pin replaces an earlier multiple component design with a single monolithic integrated circuit. Thin film resistors and decoupling capacitors complete the (monolithic-hybrid) Monobrid. Featuring 3,000,000 hour MTBF, 50 mV • nsec glitch, and -55°C to +125°C operating temperature range, the Monobrid ADH-030 II is offered with MIL-STD-883B screening.

APPLICATIONS

With its small size, wide operating temperature range and hermetically sealed package, the Monobrid ADH-030 II is ideal for the most demanding military and industrial requirements. Its high speed and low glitch are well suited for numerous CRT display applications, including TV and radar video reconstruction, and X-Y deflection positioning. Additional applications include digitally controlled frequency agile oscillators and high speed A/D converters.

Note: Monobrid® is a registered trademark of ILC Data Device Corp.

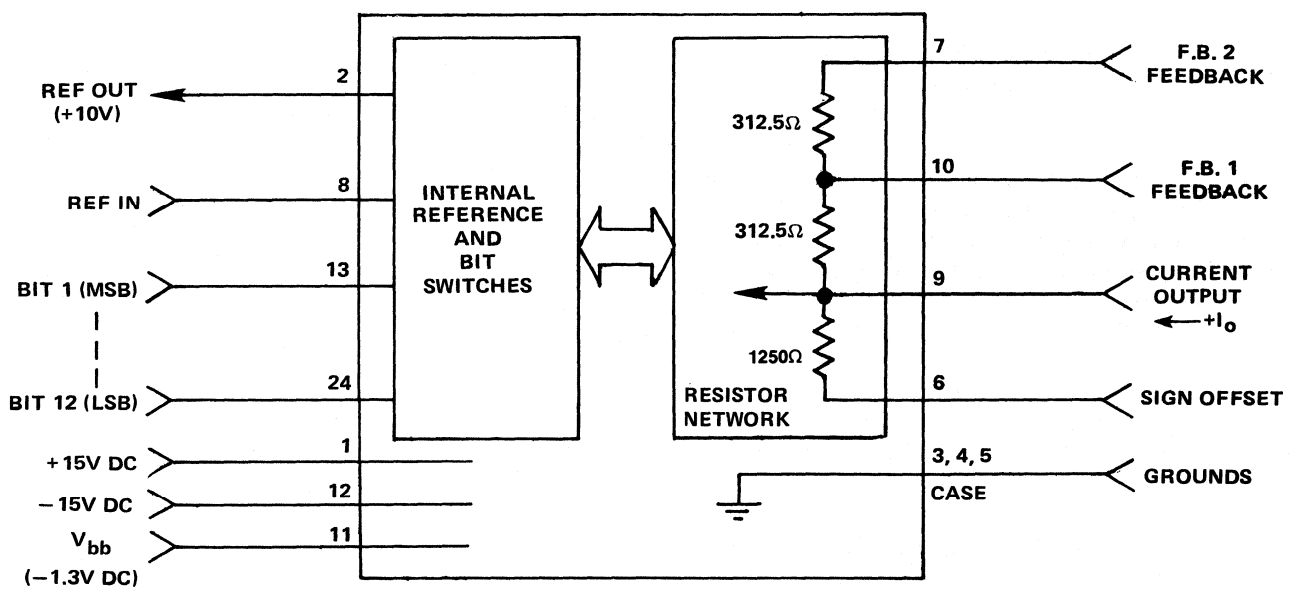


FIGURE 1. ADH-030 II BLOCK DIAGRAM

SPECIFICATIONS
Typical values at 25°C and at nominal power supply voltages unless otherwise noted.

PARAMETER	UNIT	-10	-12
RESOLUTION	Bits	12	12
ACCURACY			
Linearity Error (Max)	% F.S. Range	± 0.05	± 0.0125
Linearity Tempco*	ppm/°C	± 5	± 5
Gain Accuracy	% F.S. Range	± 0.1	± 0.05
Gain Tempco*	ppm/°C	50	25
Zero Offset			
Unipolar Offset (Max)	μA	4	1
Bipolar Offset (Max)	μA	8	4
Offset Tempco	ppm/°C	20	10
Monotonic to	bits	10	12
*Lower Tempco values are available – consult factory.			
DYNAMIC CHARACTERISTICS			
Update Rate	MHz	50 min	
Settling Time to 0.01% of Final Value			
For F.S. Input Change	ns	35 typ; 50 max	
For 1 LSB Change (From 01...11 to 10...00)	ns	20 typ	
Internal Skewing Time	ps	400 typ; 800 max	
Output Time Constant	ns	1.3 typ into 100Ω load	
Glitch Energy	LSB·nsec	200	
	mV·nsec	50 into 100Ω	
DIGITAL INPUT (VALUES GIVEN FOR V_{bb} = −1.30V DC)			
Input Coding		Positive logic Complementary Binary gives unipolar output. Complementary Offset Binary or Two's Complement (if MSB is provided) give bipolar output	
		Logic "1"	Logic "0"
Digital Voltage Level	V	−0.81 to −0.96	−1.65 to −1.85
Max Voltage Without Damage	V	0	−6
Current Loading	μA	100 max	1 max
REFERENCE AND SIGN OFFSET			
Internal +10.000V Reference		- 10	-12
Accuracy	% of Ref	± 0.1	±0.05
Max Current Output	mA	15 max	
External Ref. Requirements (Optional)			
Voltage Range	V	+ 10 ± 10%	
Current Requirements			
For Ref Input	mA	4.0 typ; 4.4 max	
For Sign Offset	mA	8.0 typ; 8.8 max	
Ref. Input Impedance	KΩ	2.5 ± 1%	
Sign Offset Impedance	KΩ	1.25 ± 1%	
OUTPUT (CURRENT TYPE)			
Unipolar Current	mA	0 to −16	
Bipolar Current	mA	± 8	
Compliance	V	− 0.5 to +5.0	
Voltage Output Ranges			
With External Amplifier	V	Full accuracy; 0 to 5 0 to 2.5, ± 5, ± 2.5, ± 1.25 Reduced Accuracy: 0 to 10	
Output Capacitance	pF	20 typ	
POWER SUPPLIES			
Voltage	V	+15	−15	−1.3 (V_{bb})
Regulation for Full Accuracy	%	± 2	± 2	± 3
Absolute Max Limit	V	+18	−18	−4
Current Typ	mA	13	57	0.5
Max	mA	15	60	2
TEMPERATURE RANGE (CASE)			
Operating			
−1 Option	°C	−55 to +125	
−3 Option	°C	0 to +70	
Storage	°C	−55 to +125	
THERMAL IMPEDANCE			
Junction to Air, θ_{JA}	°C/Watt	20 max	
Junction to Case, θ_{JC}	°C/Watt	2 max	
Max Junction Temperature is 150°C. Heat Passes Through Header (Case Bottom).			
PHYSICAL			
Package		24 Pin, Double DIP	
Size	inch	1.4 x 0.8 x 0.2 (36 x 20.3 x 5.1 mm)	
Weight	oz	0.4 (11.3 g) typ	

TECHNICAL INFORMATION

INTRODUCTION

The ADH-030 II generates analog output currents which are digitally controlled, binary weighted, discrete fractions of a reference voltage. The reference voltage is fixed so that the output current has a single value for each digital input code. A reference is generated internally, as indicated in the block diagram Figure 1, but a properly regulated external reference voltage may be substituted. The analog output is controlled by a ladder network of thin film precision resistors, controlled by bipolar transistor switches turned on and off in accordance with the digital input code.

Figure 2 is an internal schematic for the ADH-030 II showing the 8 mA current generators, the R-2R ladder network, and the external connections. Feedback resistors are provided to assist in converting the current output into a voltage output with an external amplifier, as discussed below. The sign offset (pin 6) is used for bipolar operation, as discussed below. Note that the current direction is defined as positive for currents entering the output, pin 9.

The ADH-030 II accepts complementary binary or complementary offset binary input coding. The MECL/ECL input logic requirements are detailed in the specifications table. Figure 3 shows the current outputs obtained for various bit weights. The values for Full Scale (F.S.) and 1 LSB are as follows:

RANGE	FULL SCALE	1 LSB
±8 mA	8.00000 mA	0.00391 mA
0 to −16 mA	16.00000 mA	0.00391 mA
±1.25*	1.25000V	0.00061V
±2.5*	2.50000V	0.00122V
±5V*	5.00000V	0.00244V
0 to +2.5V*	2.50000V	0.00061V
0 to +5V*	5.00000V	0.00122V
0 to +10V*	10.00000V	0.00244V

*With external output amplifier

NORMAL OPERATION

1. Normal Operation/Current Type Output

The input/output connections for normal operation of the ADH-030 II are shown in Figure 4.

For unipolar current output, the maximum output voltage is limited by the — 16 mA current capability to

$$V_{max} = -0.016R, \frac{1}{R} = \frac{1}{200} + \frac{1}{RL}$$

where RL is the load resistance and 200Ω is the resistance of the ladder network. The compliance limits V_{max} to −0.5V, so the load resistance should be 37Ω or less.

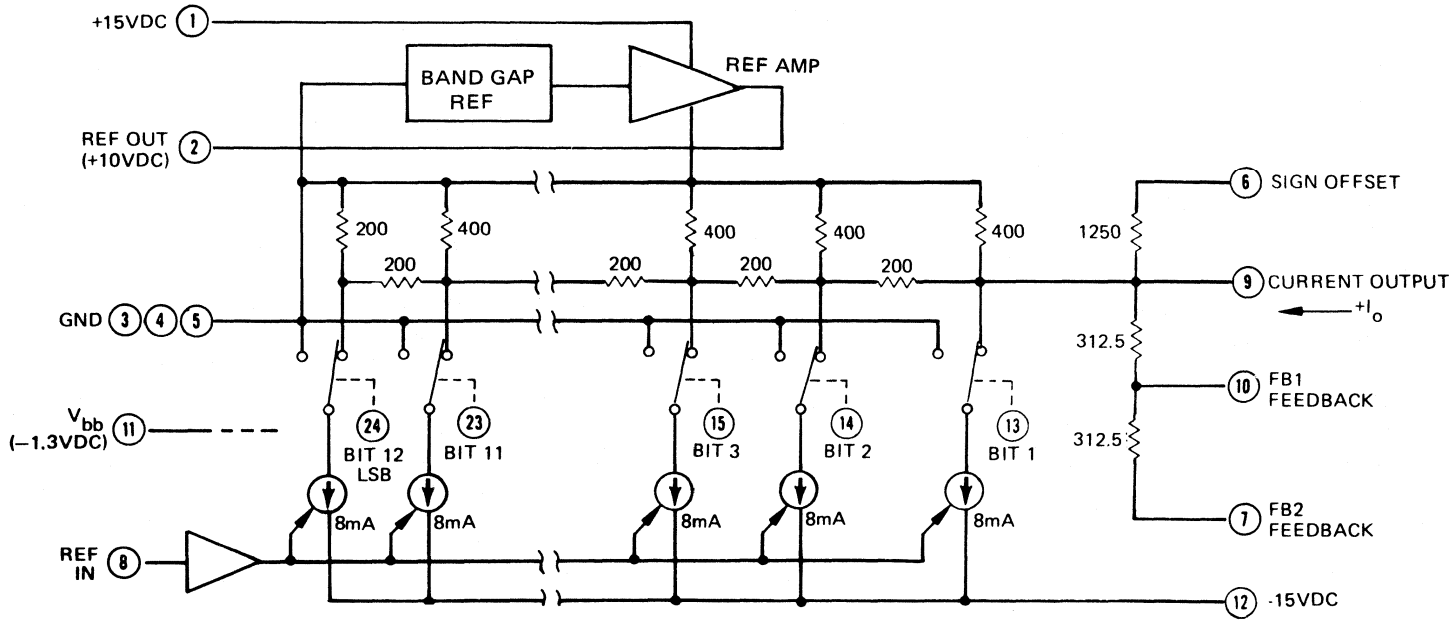


FIGURE 2. ADH-030II INTERNAL SCHEMATIC

ANALOG OUTPUT CURRENT*		DIGITAL BIT INPUTS											
UNIPOLAR COMPLEMENTARY BINARY	BIPOLAR COMPLEMENTARY OFFSET BINARY	MSB											LSB
		1	2	3	4	5	6	7	8	9	10	11	12
+F.S. −1LSB	+F.S. −1LSB	0	0	0	0	0	0	0	0	0	0	0	0
+ ¾F.S.	+ ½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1
+ ½ F.S.	+ 1LSB	0	1	1	1	1	1	1	1	1	1	1	1
+ ½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1
+ ½ F.S. −1LSB	−1LSB	1	0	0	0	0	0	0	0	0	0	0	0
¼ F.S.	− ½ F.S.	1	0	1	1	1	1	1	1	1	1	1	1
+ 1LSB	− F.S. + 1LSB	1	1	1	1	1	1	1	1	1	1	1	0

*Current direction defined as positive for currents entering the output.

FIGURE 3. BIT WEIGHT TABLE

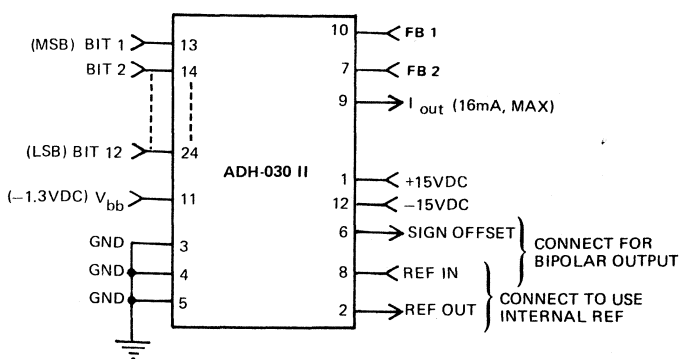


FIGURE 4. INPUT/OUTPUT CONNECTIONS FOR NORMAL OPERATION

For bipolar operation the sign offset must be connected to the REF IN. The 1250Ω sign offset resistor (see Figure 2) is in parallel with the 200Ω ladder network, reducing the internal impedance at the output to 172.4Ω. The maximum output voltage is limited by the ±8mA current to

$$V_{max} = \pm 0.008R, \frac{1}{R} = \frac{1}{172.4} + \frac{1}{RL}$$

Since the compliance is −.5 V to +5 V, the load resistance should be 98Ω or less.

2. Normal Operation/Voltage Type Output

The ADH-030 II provides up to −0.5V to +5.0V compliance, so external circuitry must be added if a larger voltage swing is required.

Figure 5 shows an optional circuit for converting the ADH-030 II current output to a voltage type output. The voltage range is determined by connections to the feedback pins FB1 and FB2 on the ADH-030II. Adding a jumper between pins 6 and 8 provides offset for bipolar operation. The following table shows jumper and feedback connections for all voltage ranges.

VOLTAGE RANGE	JUMPER CONNECTIONS	FEEDBACK CONNECTIONS
±1.25V	Sign to Ref In, FB2 to current out	FB1
±2.5V	Sign to Ref In	FB1
±5V	Sign to Ref In	FB2
0 to +2.5V	FB2 to current out	FB1
0 to +5V	None	FB1
Reduced Accuracy:		
0 to +10V	None	FB2

Note that on the 0 to +10 voltage range, the overall accuracy of the ADH-030 II is reduced to 0.2% F.S. range for all linearity grades.

3. Trimmed Operation

Without external trimming, the output accuracy of the ADH-030 II is affected by the gain accuracy and zero offset error listed in the specifications. Using external trim resistors the gain and offset errors can be trimmed to zero so that the overall accuracy is equal to the linearity.

Figure 6 shows input/output connections for trimmed operation. The zero offset adjustment range is approximately ±20 LSB. The gain adjustment is provided by a resistor which replaces the direct connection between REF OUT and REF IN. The gain adjustment range is 3% in the direction of *decrease* only. To provide for adjustments in the opposite direction, the gain must be offset. This can be accomplished in conjunction with the voltage output circuit of Figure 5 by inserting a 10 or 5Ω resistor in the feedback path, as indicated at pins 7 and 10 in Figure 6.

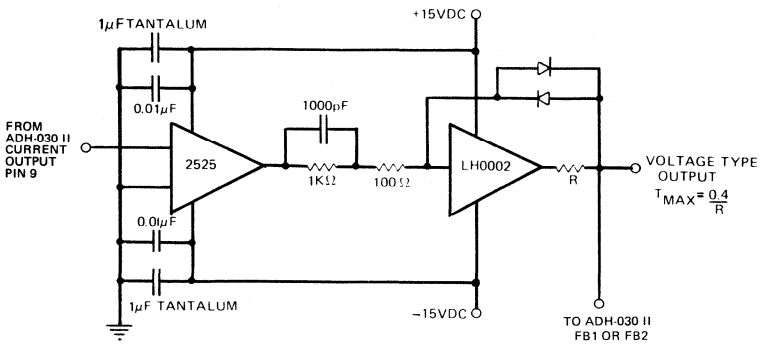


FIGURE 5. EXTERNAL CIRCUIT FOR VOLTAGE TYPE OUTPUT

LINEARITY AND ACCURACY TESTS

Accuracy may be tested as follows: Connect pins 2, 6, and 8 together. Install the voltage output circuit of Figure 5 with direct feedback to FB2 (±5.0V output). The table in Figure 3 can be used to calculate the appropriate bit weights. A voltmeter with ±0.001V accuracy is required to measure the output. Unless a computer program is available to analyze the data, the most convenient test procedure is as follows:

(1) Measure the offset at the code 4 zero voltage.

(2) Install offset trim resistors and trim the offset error to zero. Determine the gain by measuring the output at both the +F.S. −1 LSB and −F.S. The gain is the sum of the magnitudes of the two end point voltages divided by 2 F.S. −1 LSB = 9.99756V.

(3) Install gain trim resistors and trim the gain to unity. Measure the output at all other codes to determine the linearity error.

The measured errors shall all be within the limits listed in the specifications table.

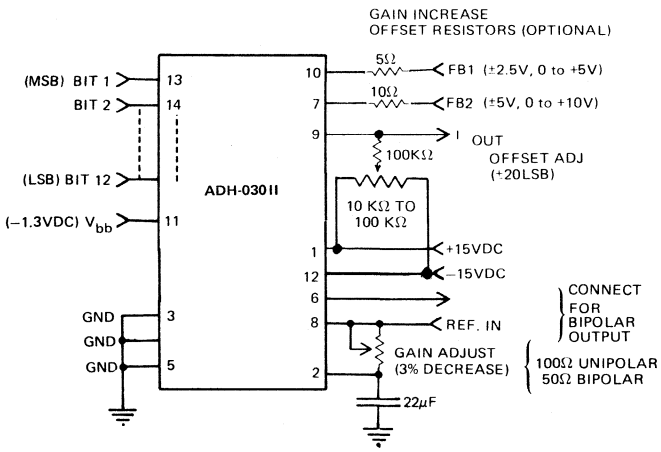


FIGURE 6. INPUT/OUTPUT CONNECTIONS FOR TRIMMED OPERATION

DYNAMIC CHARACTERISTICS

Skew is the difference in delay between individual bit transitions. When data changes, internal or external differences in delays between 0-1 and 1-0 transitions can cause the output to swing to intermediate states. For instance, if the input changes from 100 . . . 0 to 011 . . . 1 and the MSB changes before the lower order bits change, the output will swing to an intermediate state of 00 . . . 0. Internal skew is very low (400 ps typical) in the ADH-030 II because current mode switching is utilized. The MECL/ECL logic required by the digital input has inherently low skew properties, but to eliminate the last nanoseconds of skew it is necessary to clock the input with a register and match external circuit delays and line length differences. To maintain minimum skew with variations in temperature and power supplies, it is recommended that ADH-030 II pin 11 be connected to the V_{bb} output pin of an ECL logic circuit such as the MC10115.

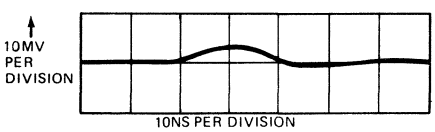


FIGURE 7. TYPICAL GLITCH SHAPE FOR 1 LSB CHANGE AT MAJOR CARRY (INTO 100Ω LOAD)

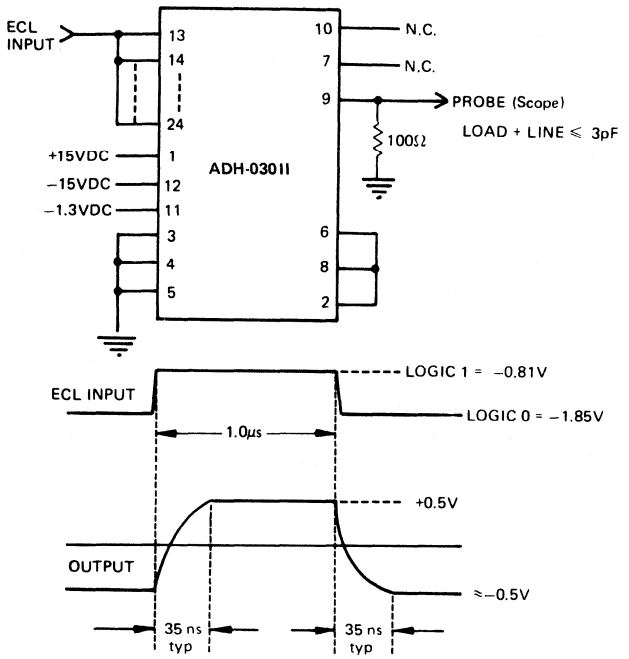
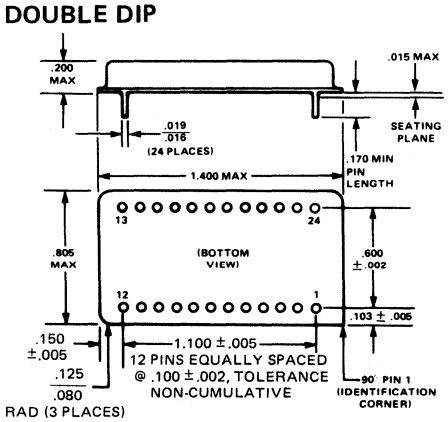


FIGURE 8. SETTLING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

ORDERING INFORMATION

ADH-030 II–12–1–883B

- 883B = Conforms to MIL-STD-883 DDC procedures
  Blank = Same except preburn in test and burn in are omitted.
- Operating Temperature Range:
  1 = –55°C to +125°C
  3 = 0°C to +70°C
- Linearity:
  10 = ±.05%
  12 = ±.0125%

Glitch energy is only 50 mV • nsec typ. Figure 7 shows glitch shape at major carry from 01 . . . 11 to 10 . . . 00 when the output is terminated by a 5 MHz filter and a 100 ohm resistor.

Settling time may be tested using the circuit shown in Figure 8. For a maximum output swing between —0.5V and +0.5V, the output will settle to 0.01% of final value within 50 ns (35 ns typical). For a swing of 1 LSB, the settling time depends on the skew and resulting glitch. For a 1 LSB change at major carry from 01 . . . 11 to 10 . . . 00, the settling time is 20 ns typical.

Ringing caused by long lead lengths or unterminated transmission line effects in the bit drives may lead to increased settling time or cause oscillation. If the lead length can not be shortened, the effect may be reduced or eliminated by placing RF beads on every other digital input lead.

REFERENCE

The ADH-030 II has an internal reference supply and is factory calibrated with this supply. Fixed external references of +10VDC ±10% can be accommodated and the output current will be linearity proportional to the reference voltage over this range.

RELIABILITY

The use of a single monolithic I.C. and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All Model ADH-030 II converters are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5008 except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) is 3,000,000 hours, Ground Fixed, at 25°C.

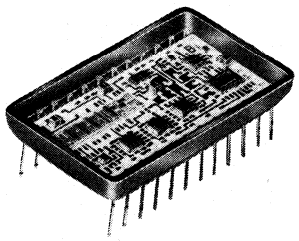
PIN CONNECTION TABLE

PIN No.	FUNCTION	PIN No.	FUNCTION
1	+15VDC	13	Bit 1 (MSB)
2	Ref. Out	14	Bit 2
3	Gnd*	15	Bit 3
4	Gnd*	16	Bit 4
5	Gnd*	17	Bit 5
6	Sign Offset	18	Bit 6
7	Feedback 2	19	Bit 7
8	Ref. In	20	Bit 8
9	Output	21	Bit 9
10	Feedback 1	22	Bit 10
11	–1.3VDC = V_{bb}	23	Bit 11
12	–15VDC	24	Bit 12 (LSB)

*All grounds are tied to the case.

DAC-02900

16 BIT D/A CONVERTER
±0.0008% Linearity; Voltage Output



ADVANCE INFORMATION*

FEATURES

- *±0.0008% FSR LINEARITY AVAILABLE*
- *10 V FULL SCALE VOLTAGE OUTPUT*
- *+6.4 V PRECISION INTERNAL REFERENCE*
- *−55°C to +125°C TEMPERATURE RANGE*
- *SMALL HERMETIC 24 PIN DDIP PACKAGE*
- *PIN FOR PIN REPLACES DAC-HP16 AND DAC72 TYPES WITH INCREASED LINEARITY*

DESCRIPTION

The DAC-02900 is a 16 bit 15 microsecond hybrid D/A converter with a 10 volt full scale output range. Packaged in a small hermetic 24 pin DDIP, it operates over the −55°C to +125°C temperature range and is available screened to MIL-STD-883B. DAC-02900 has a precision internal reference and is available in linearity grades of 16 bit (±0.0008%), 15 bit (±0.0015%) and 14 bit (±0.003%). It is a pin-for-pin replacement for DAC-HP16 and DAC72 types with increased linearity performance.

With its 16 bit linearity, broad operating temperature range, and small hermetic package, the DAC-02900 is ideal for the most demanding military and industrial requirements. It is particularly well suited for audio reconstruction, waveform generation, and precision test equipment applications.

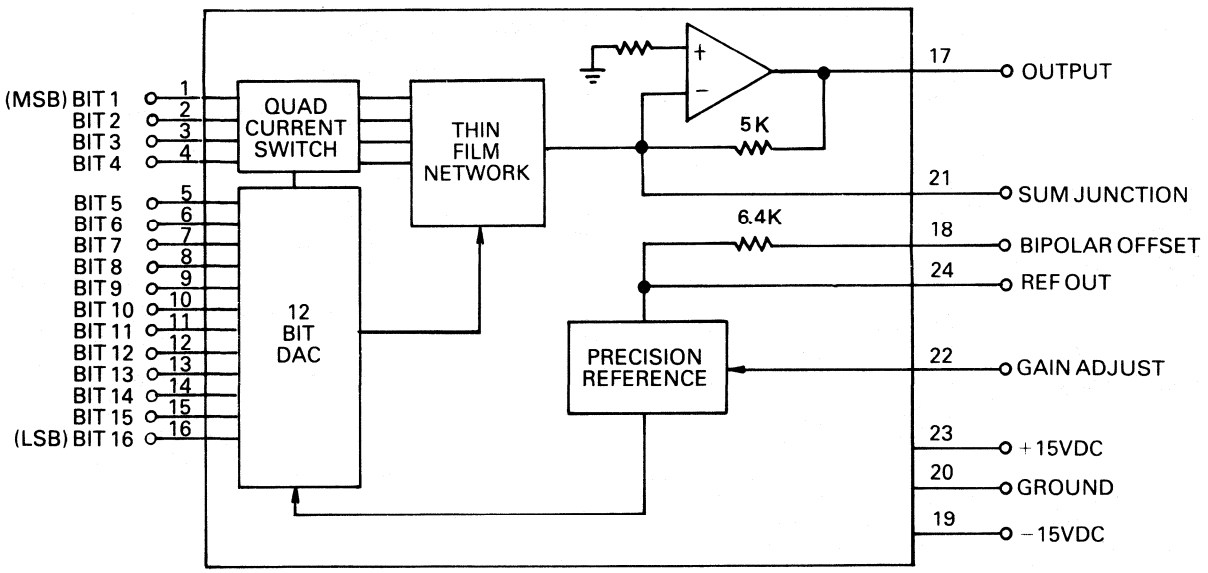


FIGURE 1. DAC-02900 BLOCK DIAGRAM

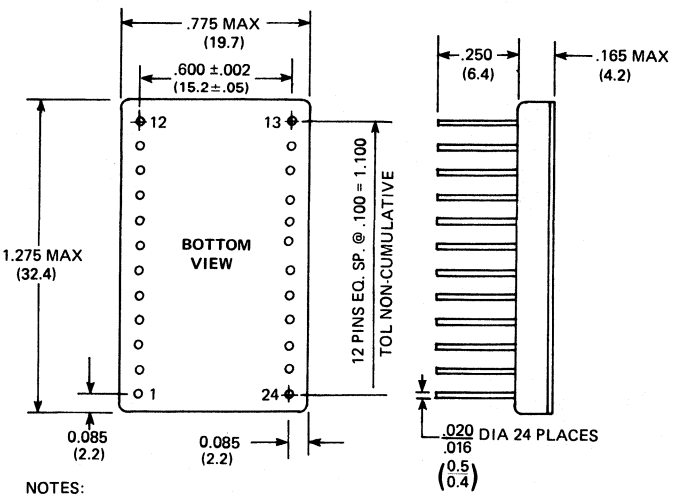
SPECIFICATIONS

Typical values at 25°C and nominal power supply voltages unless otherwise noted.

PARAMETER	UNITS	VALUE		
		14 BIT LIN	15 BIT LIN	16 BIT LIN
RESOLUTION	Bits	16	16	16
ACCURACY				
Linearity Error	%FSR	±0.003 max	±0.0015 max	±0.0008 max
Linearity Tempco	ppm/°C	0.5 max	0.5 max	0.5 max
Gain Error(1)	%FSR	0.1	0.1	0.1
Gain Tempco	ppm/°C	15 max	10 max	10 max
Zero Error(1) (Unipolar)	%FSR	0.1	0.1	0.1
Zero Tempco (Unipolar)	ppm/°C	4 max	4 max	4 max
Offset Tempco (Bipolar)	ppm/°C	6 max	6 max	6 max
Monotonicity (+10°C to +40°C)	bits	14	15	16
DYNAMIC CHARACTERISTICS				
Settling Time(2)	µsec	15 max		
DIGITAL INPUTS				
Logic Compatibility		TTL and 5V CMOS		
Voltage Input				
Logic "1"	V	0 to +0.8		
Logic "0"	V	2.4 to +5.5		
Current Load				
Logic "1"	µA	+40		
Logic "0"	µA	−400		
Coding				
Unipolar		Complementary Binary		
Bipolar		Complementary Offset Binary		
REFERENCE				
Output Voltage	V	+6.4		
Output Impedance	Ω	0.2		
Output Current	µA	±3 max		
ANALOG OUTPUT				
Voltage-Unipolar(3)	V	0 to +10		
Voltage-Bipolar	V	±5		
Current	mA	± 5 min		
Impedance	Ω	0.1 max		
Noise(4)	µV rms	20		
POWER SUPPLIES				
+15V Supply				
Tolerance	%	±5		
Max Voltage	V	+18 max		
Current Drain	mA	20 typ	30 max	
−15 Supply				
Tolerance	%	±5		
Max Voltage	V	−18 max		
Current Drain	mA	28 typ	42 max	
PS Rejection Ratio	%FSR/%	±0.001		
TEMPERATURE RANGE				
Operating (Case)				
−1 Option	°C	−55 to +125		
−2 Option	°C	−25 to +85		
Storage	°C	−65 to +150		
PHYSICAL CHARACTERISTICS				
Package		24 pin DDIP		
Size	in (mm)	1.3 x 0.8 x 0.2 (33 x 20.3 x 5.1)		
Weight	oz (g)	0.4 (11.3)		

Notes: (1) Gain and Offset errors are trimmable to zero.
(2) Settling time to ±0.005 %FSR for 10 volt change.
(3) Consult factory for other output voltage ranges.
(4) Noise specified for DC to 100 kHz bandwidth.

MECHANICAL OUTLINE



NOTES:
1. Dimensions shown are in inches.
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

PIN FUNCTION TABLE

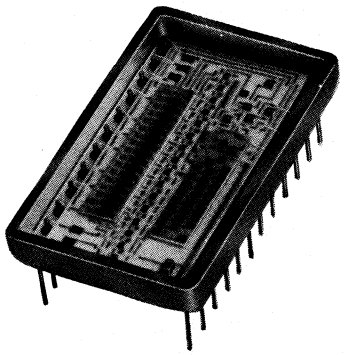
PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	13	BIT 13
2	BIT 2	14	BIT 14
3	BIT 3	15	BIT 15
4	BIT 4	16	BIT 16 (LSB)
5	BIT 5	17	OUTPUT
6	BIT 6	18	BIPOLAR OFFSET
7	BIT 7	19	−15VDC
8	BIT 8	20	GROUND
9	BIT 9	21	SUM JUNCTION
10	BIT 10	22	GAIN ADJUST
11	BIT 11	23	+15VDC
12	BIT 12	24	REF OUT

ORDERING INFORMATION

DAC-02900–1 0 6

- 6 = Linearity Grade:
  - 6 = 16 bit
  - 5 = 15 bit
  - 4 = 14 bit
- 0 = Reliability Grade:
  - 1 = Conforms to MIL-STD-883
  - 0 = Same except preburn in test and burn in are omitted
- 1 = Operating Temperature Range
  - 1 = −55°C to +125°C
  - 2 = −25°C to +85°C

12 BIT 35NSEC HYBRID D/A CONVERTER
Video Speed Settling; Low Glitch



DESCRIPTION

The DDC 1250 is a 12 bit 35 nanosecond hybrid D/A converter packaged in a hermetically sealed 24 DDIP. It is a pin for pin replacement for HDS 1250 types. Featuring −55°C to +125°C operating temperature range, 50 mV • nsec glitch under optimum conditions, and an MTBF of 4,000,000 hours, the DDC 1250 is offered with MIL-STD-883B screening. Other features include TTL logic compatibility and internal precision DC reference.

APPLICATIONS

With its small size, wide operating temperature range and hermetically sealed package, the DDC 1250 is ideal for the most demanding military and industrial requirements. Its high speed and low glitch are well suited for numerous CRT display applications, including TV and radar video reconstruction and vector stroke X-Y deflection. Additional applications include high speed A/D converters and waveform generators.

FEATURES

- *FAST SETTLING: 35 NSEC TO 0.02%*
- *LOW GLITCH: 50 MV•NSEC*
- *PIN FOR PIN REPLACES HDS 1250 TYPES AT LOWER POWER*
- *−55°C TO +125°C OPERATING TEMPERATURE*
- *HIGH RELIABILITY 4,000,000 HOUR MTBF*
- *HERMETICALLY SEALED 24 DDIP PACKAGE*

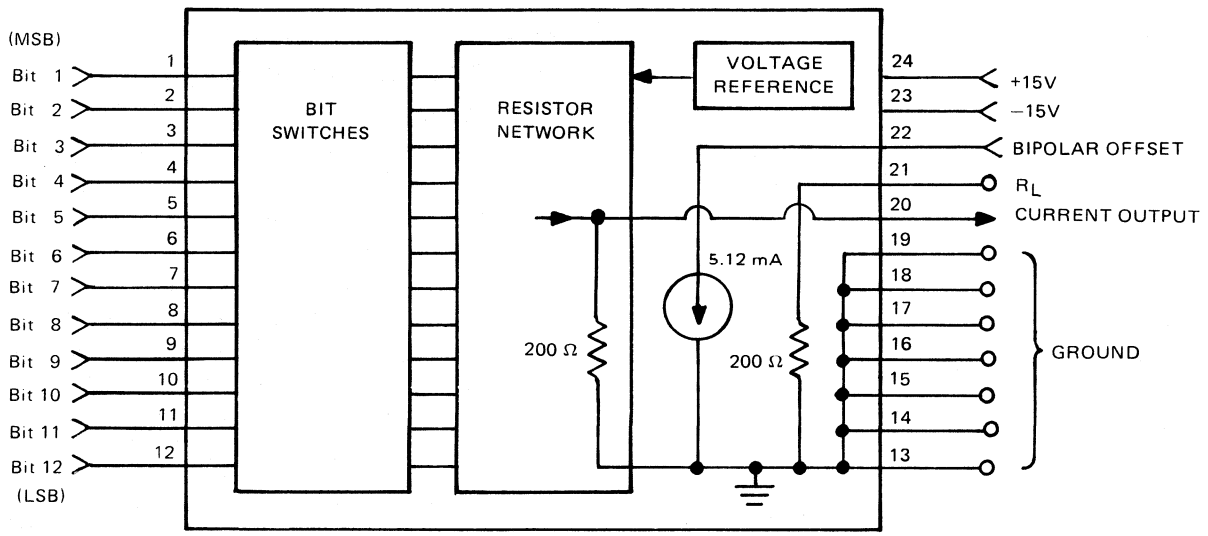


FIGURE 1. DDC 1250 BLOCK DIAGRAM

SPECIFICATIONS
Typical values at 25°C and at nominal power supply voltages unless otherwise noted.

PARAMETER	UNITS	VALUE 10 BIT LIN	VALUE 12 BIT LIN
RESOLUTION	bits	12	12
ACCURACY			
Linearity Error (Max.)	% F.S.R.	±0.05	±0.012
Linearity Tempco	ppm/°C	±3	±3
Gain Error (1)	% F.S.R.	±0.1	±0.05
Gain Tempco	ppm/°C	30	30
Zero Offset (Max)	nA	30	15
Offset Tempco			
Unipolar	ppm/°C	3	3
Bipolar	ppm/°C	15	15
Monotonocity		Guaranteed Over Operating Temp Range	
DYNAMIC CHARACTERISTICS (1)			
Settling Time (2)			
Current	nsec	35	
Voltage	nsec	60	
Glitch Energy (3)	mV · nsec	50	
DIGITAL INPUTS			
Logic Compatibility		TTL and 5V CMOS	
Voltage Input			
Logic "1"	V	+2 to +7.0	
Logic "0"	V	0 to +0.8	
Current Load			
Logic "1"	μA	1	
Logic "0"	μA	15	
Coding			
Unipolar		Binary	
Bipolar		Offset Binary	
OUTPUT			
Current			
Unipolar	mA	0 to +10.24	
Bipolar	mA	±5.12	
Voltage (1)			
Unipolar	V	0 to +1.024	
Bipolar	V	±0.512	
Compliance	V	−2 to +1.5	
Impedance	Ω	200	
POWER SUPPLIES			
Voltages	V	+14.5 to +15.5	−12 to −16
Current (Max)	mA	35	15
Power Supply			
Rejection Ratio	%/V	0.2	0.2
TEMPERATURE RANGE			
Operating			
−1 Option	°C	−55 to +125	
−3 Option	°C	0 to +70	
Storage	°C	−55 to +125	
PHYSICAL			
Package		24 pin DDIP	
Size	in (mm)	1.4 x 0.8 x 0.2 (36 x 20.3 x 5.1)	
Weight	oz. (g)	0.4 (11.3)	

Notes:
1. With internal 200 ohm R_L connected to output.
2. Full scale change to within 0.02% of final value.
3. With zero input logic skew and DAC logic threshold adjustment.

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a block diagram of the DDC 1250. Functional elements of the DAC include bit switches, a precision thin film resistor network, a DC voltage reference, a current source and a load resistor.

TTL compatible bit switches are used to steer equally weighted currents to either the resistor network or ground. The resistor network contains a precision R/2R ladder, which produces binarily weighted currents at the putput. The combination of equally weighted currents and R/2R ladder network yields the optimum fast settling and low glitch performance.

The precision DC voltage reference is used, along with bias resistors in the thin film network, to program the bit switch currents. The voltage reference also provides the bias for the 5.12 mA current source, which is used to generate a bipolar output. For a unipolar output the resistor network provides an output current of zero to +10.24 mA. When the bipolar offset current is connected to the output, ±5.12 mA is provided. The 200 ohm load resistor is provided as a convenient way to implement a zero to +1 volt output voltage swing. If other output voltages are required, the 200 ohm internal resistor may not be connected and an external load resistor will be used.

DYNAMIC CHARACTERISTICS AND GLITCH

The DDC 1250 is designed for fast settling operation, along with low output glitch. This is achieved by using equally weighted current mode switches and a binarily weighted R/2R ladder network. For a full scale input code change, the output current settles to within 0.02% of final value within 35 nanoseconds. Output glitch area of 50 mV · nsec can be achieved with zero input logic skew and adjustment of the DAC logic threshold.

All DACs exhibit output glitch when major carry code changes are made. Glitch is the response to a momentary erroneous code which occurs due to the input data skew and unequal bit switch turn on/off times. Glitch energy, rather than glitch amplitude, is used as a basis of comparison because it is the product of amplitude and time, and is therefore independent of bandwidth considerations. Glitch energy is defined as the net area contained under the glitch waveform.

To minimize DDC 1250 glitch area, great care was taken in design and layout to minimize unequal bit switch turn on and turn off times. To maintain this low glitch performance, care must be taken to keep input data skew as small as possible. The use of input latches, preferably LS logic types, placed close to the DAC is a good way to minimize data skew. Further reduction of output glitch can be achieved by monitoring the glitch as the +15 volt supply is varied slightly. Variation of the +15 volt supply causes small changes in the input logic switching threshold and therefore acts like a data skew trim.

INPUT CODING

The DDC 1250 requires Binary coded input data for unipolar analog outputs. Offset Binary input data is required

for bipolar analog outputs. Figure 2 illustrates the input coding for various analog outputs with each of the code configurations. It is to be noted that for unipolar operation +FS is equal to +10.24 mA. For bipolar operation +FS is equal to +5.12 mA and −FS is equal to −5.12 mA.

ANALOG OUTPUT RANGES

The DDC 1250 may be configured for a current output of either zero to +10.24 mA or ±5.12 mA. The output voltage corresponding to these currents depends on the equivalent resistance from the output to ground. Figure 3 illustrates the 3 most commonly used analog output ranges, along with the required connections for Bipolar Offset and R_L.

External load resistors can be used to obtain other output voltage ranges, as long as the compliance voltage limits are adhered to. The output voltage range is calculated by multiplying the output current times the parallel combination of external load resistance and 200 ohm internal resistance. External load resistors are typically metal film types. The load resistor tempco should be less than 100 ppm/°C since it directly affects DAC gain tempco.

EXTERNAL OP AMP

If a voltage output swing is required that is larger than the compliance voltage limits of the DDC 1250, then an external op amp can be used. Figure 4 illustrates the connection required to interface the DAC and the op amp. The selection of an appropriate op amp will depend primarily on the settling time requirements of the application. The op amp should be placed as close as possible to the DAC to minimize stray capacitance and inductive affects.

The output voltage range is calculated by multiplying the DAC output current times R_f. DAC output current will be either zero to +10.24 mA or ±5.12 mA, depending on the connection of the Bipolar Offset pin. The R_L pin should not be connected, since this would lower the loop gain of the op amp.

OFFSET TRIM

Some applications may require a lower output offset than the DDC 1250 exhibits after factory adjustment. This will be true only for bipolar output applications, since the offset for unipolar operation is a small fraction of 1 LSB. Figure 5 illustrates the connections required to trim the DDC 1250 offset to zero. A mulit-turn trimpot, with a temperature coefficient less than 100 ppm/°C, is recommended for best performance.

OUTPUT COMPLIANCE

Output compliance is the maximum voltage swing that is allowed on the current output pin. Voltages outside of this range will cause gross errors at the output. Permanent damage may result from externally applied voltages greater than the output compliance range. The DDC 1250 has an output compliance voltage range of −2 volts to +1.5 volts. An example of a violation of the output compliance spec is if the DDC 1250 is connected for unipolar operation with the internal R_L not connected. This configuration will result in an output voltage range of zero to +2.048 V, which is an out of spec condition.

LAYOUT PRECAUTIONS

Care must be taken in the printed circuit layout to achieve the optimum performance of the DDC 1250. To minimize

UNIPOLAR BINARY	BIPOLAR OFFSET BINARY	SCALE
1111 1111 1111	1111 1111 1111	+FS −1 LSB
1100 0000 0000	1110 0000 0000	+3/4 FS
1000 0000 0000	1100 0000 0000	+1/2 FS
0000 0000 0001	1000 0000 0001	+1 LSB
0000 0000 0000	1000 0000 0000	0
	0111 1111 1111	−1 LSB
	0100 0000 0000	−1/2 FS
	0010 0000 0000	−3/4 FS
	0000 0000 0000	−FS

FIGURE 2. INPUT CODING

OUTPUT RANGE	CONNECT BIPOLAR PIN 22 TO	CONNECT R_L PIN 21 TO	OUTPUT IMPEDANCE
0 to +10.24 mA 0 to +1.024 V	PIN 19	PIN 20	100 Ω
±5.12 mA ±1.024 V	PIN 20	N/C	200 Ω
±5.12 mA ±0.512 V	PIN 20	PIN 20	100 Ω

FIGURE 3. ANALOG OUTPUT RANGES

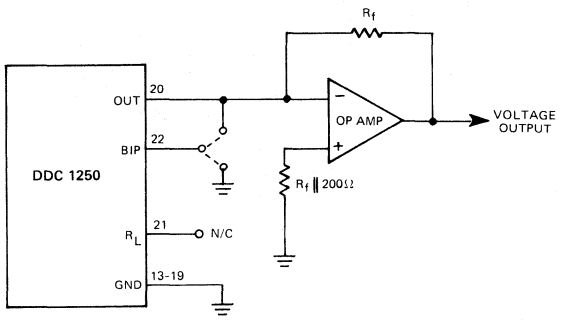


FIGURE 4. EXTERNAL OP AMP

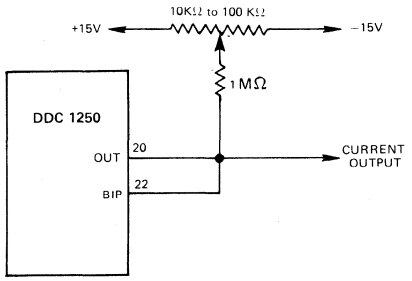


FIGURE 5. OFFSET TRIM

crosstalk and inductive effects, digital input lines and analog output lines should be separated from each other, and made as short as possible. To minimize ground noise, particular attention must be paid to achieving a low impedance ground path. A large area ground plane under the DAC is recommended for best results. Interface circuits such as input latches and output op amp should be placed as close as possible to the DAC.

POWER SUPPLY DECOUPLING

Capacitive decoupling of all power supplies is recommended to minimize noise. Tantalum or electrolytic capacitors of 1 μf or greater will filter out low frequency noise. Ceramic capacitors of 0.01 μf or greater will filter out high frequency noise. For best results, all capacitors should be placed as close to the DAC as possible.

RELIABILITY

The DDC 1250 is manufactured in accordance with the requirements of MIL-STD-883. Screening is based upon the requirements of Method 5008, except for burn-in which is optional.

Thick film and thin film circuits, as well as careful thermal design, have resulted in a very low calculated failure rate for the DDC 1250. The predicted MTBF is 4,000,000 hours, in accordance with MIL-HDBK-217C at +25°C in ground fixed applications.

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	13	GND
2	BIT 2	14	GND
3	BIT 3	15	GND
4	BIT 4	16	GND
5	BIT 5	17	GND
6	BIT 6	18	GND
7	BIT 7	19	GND
8	BIT 8	20	OUTPUT
9	BIT 9	21	R_L (200Ω)
10	BIT 10	22	BIPOLAR OFFSET
11	BIT 11	23	−15V
12	BIT 12 (LSB)	24	+15V

ORDERING INFORMATION

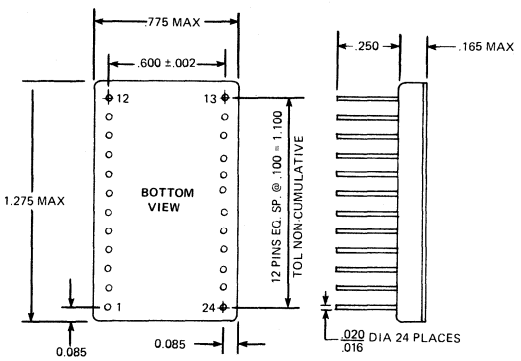
DDC 1250 – 12 – 1 – 883B

- 883B = Conforms to MIL-STD-883, DDC procedures
- Blank = Same except preburn in test and burn in are omitted.

Operating Temperature Range:
- 1 = −55°C to +125°C
- 3 = 0°C to +70°C

Linearity:
- 10 = ±.05%
- 12 = ±.012%

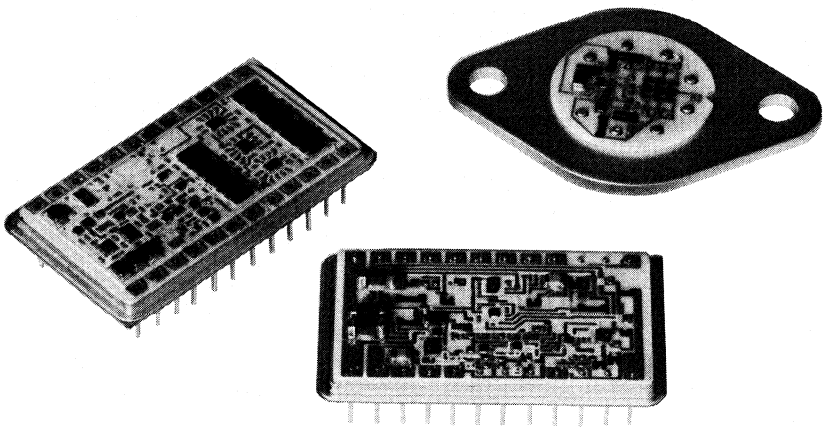
MECHANICAL OUTLINE



NOTES:

1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

13 BIT DEGLITCHED HYBRID D/A CONVERTER
10 MHz Update Rate, ±0.0125% Linearity Error



FEATURES

- *ULTRA LOW GLITCH D/A CONVERTER CONSISTS OF TWO HYBRID MODULES PLUS AN OPTIONAL HYBRID CABLE DRIVER*
- *AVAILABLE MOUNTED ON PC CARD WITH INPUT REGISTER*
- *F.S. SETTLING TIME: 600 ns to ±½ LSB*
- *CODING: Complementary offset binary (modules) Two's complement (P.C. mounted)*
- *OUTPUT RANGES: ±2.5V, ±5V and ±10V*

DESCRIPTION

With a maximum update rate of 10 MHz, a 30 mV max glitch, and a 500 mA coax drive capability, the DDAC offers exceptional performance. It may be purchased either as a complete PC card assembly or as a set of the three thick-film metal encased hybrid modules which comprise the major components of the card assembly. The DDAC is TTT/DTL compatible, with a strobe input to initiate conversion and provision for either internal or external reference voltage. The card configuration features a low power Schottky input register with 2's complement coding. Hybrid module processing is based on MIL-STD-883 with optional burn-in. Card mounted units conform to selected test methods and conditions of MIL-STD-202E and are suitable for military/aerospace applications without custom militarization.

APPLICATIONS

The DDAC series was designed for ultra-low glitch D/A conversions for critical CRT display systems where fast precise vector stroke writing is important. It usually precedes the CRT deflection driving circuitry which positions the electron beam. The DDAC is ideally suited to large screen applications such as air traffic control or situation displays. Its small size and high reliability, due to hybrid construction, enable significant size and weight savings in aircraft cockpit display systems such as Head-up and Head-down displays.

The DDAC's 13 bit resolution, high speed, and transient free output also make it an excellent choice as a programmable voltage source in automatic test equipment and in parametric testing.

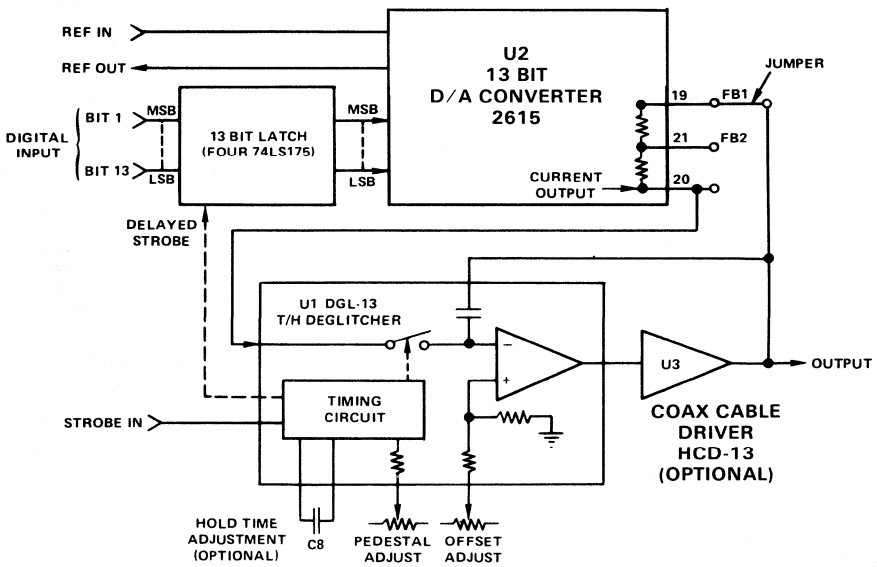


FIGURE 1. DDAC CARD ASSEMBLY SCHEMATIC (With Connections for ±10V Output)

TECHNICAL INFORMATION

INTRODUCTION

The DDAC is composed of three hybrid modules: a D/A converter, a track/hold deglitcher, and a coax cable driver. These modules may be purchased separately by the user to assemble in his own system. The card mounted (CM) DDAC includes, in addition to these modules, an input latch, trim potentiometers, and a careful layout with distributed capacitors to optimize glitch and settling time characteristics (Figure 5).

The following applications information includes the characteristics both of the card mounted DDAC and of the individual modules as part of a D/A converter. The D/A converter, T/H deglitcher, and coax cable driver can also be used separately for other purposes. More information about the D/A converter may be found in the SDAC/2615 data sheet, and about the deglitcher in the DGL-13 data sheet.

The card mounted DDAC contains either one DDAC channel (1 CM), or two separate channels (2 CM) which share the pins on the Elco card connector as shown in Figure 5.

CAUTION: DDC is not responsible for any damage to the PC board or its component resulting from changes in connections or other alterations made in the PC board by the customer.

1. CIRCUIT OPERATION

Glitches, (voltage spikes) in the output of conventional D/A converters are primarily caused by data skew and by switches which cause faster turn-on than turn-off times. Thus, whenever a code change occurs there will be a short period of time (measured in ns) when some spurious code will exist. The faster D/A's will attempt to follow this code, resulting in a transient known as a glitch. The worst case occurs at the major carry point when the input code is transitioning from 1000. . .0 to 0111. . .1. The spurious code may then be 1111. . .1, and the D/A output will momentarily slew full scale (or close to it).

The DDAC overcomes these glitches by using a carefully designed low transient track and hold amplifier (deglitcher) after the D/A. Thus, the deglitcher can be gated into the hold mode during the D/A output transient and released into the track mode after the transients have settled out. The resultant output then makes a very clean transition from one value to another. Using this technique glitches are not only greatly reduced but are only a function of deglitcher design and hence are the same for any transition and can be effectively filtered out.

As illustrated in Figure 1, the user's strobe pulse activates the timing circuit in the deglitcher. The timing circuit simultaneously opens the T/H amplifier switch so that its output remains constant, and activates the latch so that the input data bits are converted to an analog current by the D/A converter. After the analog current conversion has been completed, the T/H amplifier switch is closed again. The T/H amplifier then tracks the D/A converter, converting the D/A current into a voltage. The system output becomes stable after the T/H settles out.

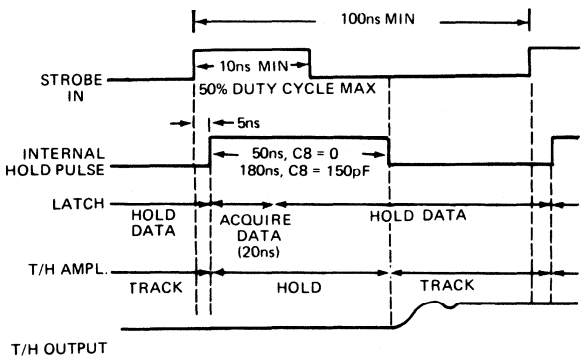


FIGURE 2. CARD ASSEMBLY TIMING DIAGRAM

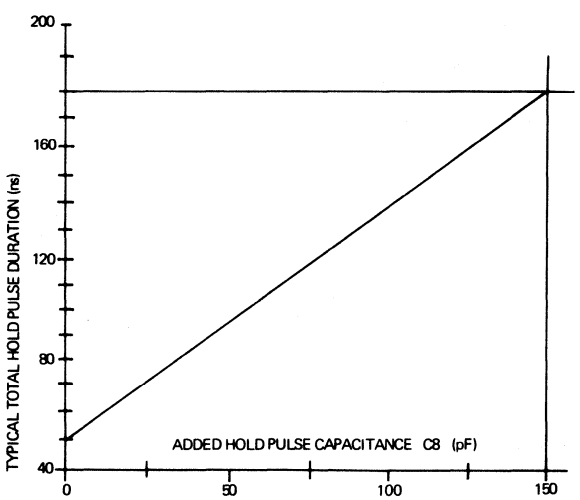


FIGURE 3. EFFECT OF C8 ON HOLD PULSE DURATION

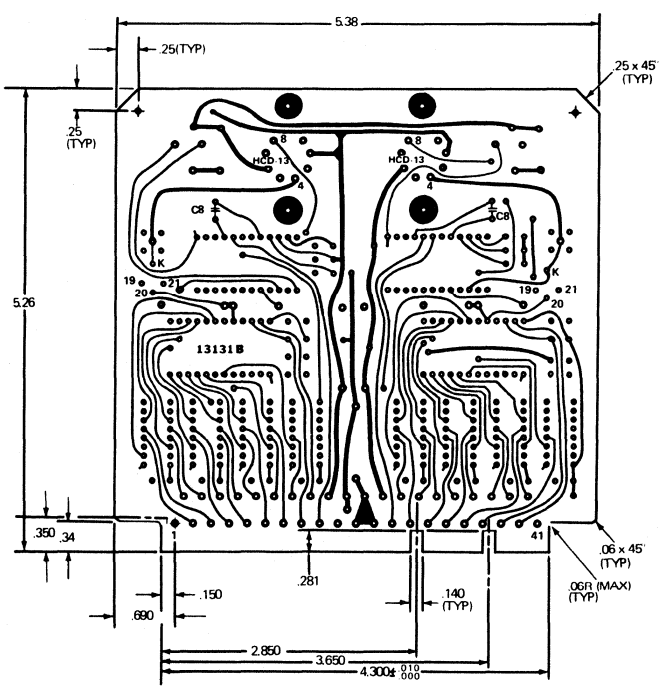


FIGURE 4. P.C. BOARD LAYOUT

2. TIMING

Figure 2 illustrates the timing of the PC card assembly DDAC. The leading edge of the input strobe triggers a one-shot in the deglitcher which, after a delay of 5 ns, generates a hold pulse. The leading edge of the hold pulse causes the latch to acquire the input data bits. This acquisition process takes up to 20 ns, and the latch bit values then remain constant. Note that the data bits are acquired during an interval of time between 5 and 25 ns after the leading edge of the strobe pulse and the input digital data should be held constant during this time interval.

The leading edge of the hold pulse also opens the switch to the T/H amplifier, so that the T/H retains the previous output while conversion is taking place.

Conversion takes place during the hold cycle pulse. The minimum hold pulse duration is 50 ns (Typical), but the customer may increase this interval to 180 ns or more by adding a capacitor to the P.C. board. Table I lists a recommended capacitor style, Figure 3 shows the capacitance required as a function of hold pulse duration, and an appropriate location for the capacitor C8 is shown on the P.C. board layout, Figure 4.

At the end of the hold pulse, the T/H amplifier switch closes and the T/H begins to track the D/A converter output again. The strobe pulse interval should be long enough to allow time for the T/H amplifier output to settle and for the analog signal to be read out.

3. DIGITAL INPUTS

(a) P.C. Card Assembly Inputs. The digital inputs consist of 13 data bits and a strobe input to load the input register. The data bits feed a low power TTL/DTL compatible Schottky input register. Coding is two's complement as shown in the table below. The strobe input must be a positive TTL pulse with a minimum pulse width of 10 ns. Loading is 3 std TTL unit loads.

TABLE 1 CARD ASSEMBLY PARTS LIST

Circuit Symbol	Description	Part Number
U1	T/H Deglitcher	DGL-13-
U2	D/A Converter	2615-
U3	Coax Driver	HCD-13
U4	Quad D Flip-Flop	SN74LS175J
R1, R2	5K, 10%, 3/4 Watt Pot.	Bourns 3069-P-1-502
C1	.01μF, 10%	Vitramon VK33
C5	4.7μF, 10%	CS-13
C6, C7	1μF, 10%	CS-13
C8 (optional)	TBD	Vitramon VK23
P1	41 pin connector	ELCO P/N 00-7022-041-000-001
—	Mates with:	ELCO P/N 7008-41
J1, J2	Coax sub-miniature	DDC P/N 5301-0900-0000
	R.F. connector	Selectro P/N 51-153-0000
	Mates with:	Selectro P/N 51-107-0000
		DDC P/N 5304-2900-0000

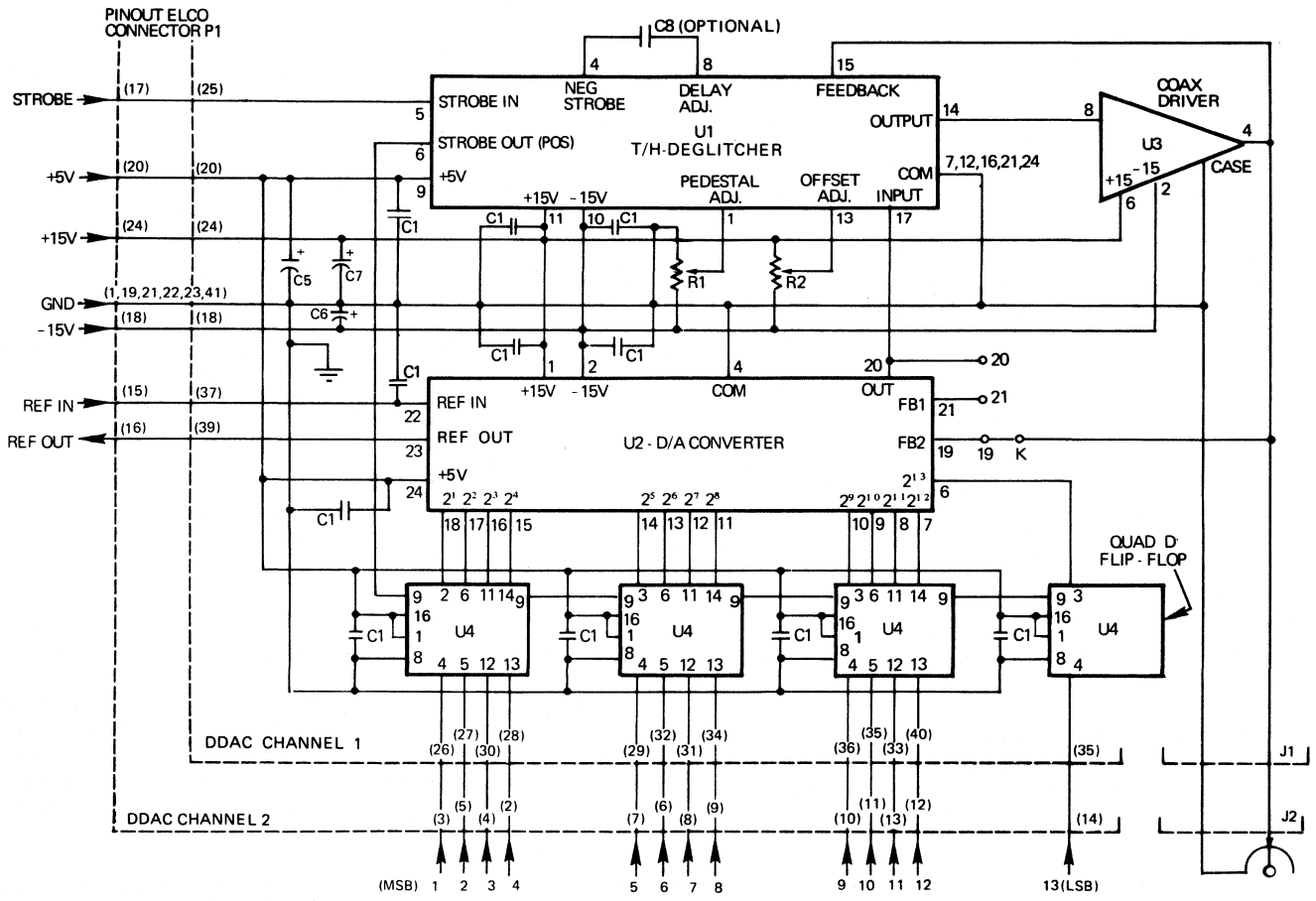


FIGURE 5. DDAC CARD ASSEMBLY CONNECTIONS (+10V OUTPUT).
SEE TABLE I FOR PARTS LIST.

(b) D/A Converter Input. The digital inputs to the D/A itself (P/N 2615) are DTL and TTL compatible and are one standard TTL unit load. The coding is inverted offset binary as shown in the table.

ANALOG OUTPUT	DIGITAL INPUT CODING	
	P.C. CARD INPUT TWO'S COMPLEMENT	D/A INPUT INVERTED O.B.
+F.S. - LSB	0111111111111	0000000000000
+1/2 F.S.	0100000000000	0011111111111
0	0000000000000	0111111111111
−1/2 F.S.	1100000000000	1011111111111
−F.S.	1000000000000	1111111111111

4. ANALOG OUTPUT

(a) Standard P.C. Card Assembly. In the standard P.C. card assembly (see Figure 5) the output voltage range is ±10V and the HCD-13 coax cable driver provides up to 500 mA. Since the deglitcher output itself can only provide ±10 mA, the coax driver is useful whenever a cable or a long length of wire is connected to the output. Glitch characteristics are not affected by the HCD-13, since the driver is wideband and within the feedback loop.

The driver output is protected against short circuits to ground as long as the case temperature does not exceed +85° C. The output of the deglitcher itself is not protected against short circuits to ground.

(b) Omission of Coax Cable Driver. If the user assembles the DDAC from components and chooses to omit the cable driver, the feedback pin 15 on the deglitcher should be connected to the output, pin 14 (Figure 5). The connection should be made as close as possible to the load to reduce the effects of line resistance.

The P.C. card assembly may be purchased without the coax cable driver, as described in the ordering information.

(c) ±5V and ±2.5V Output Ranges. As shown in Figure 1 and 5, the D/A converter has internal resistors for pin selection of alternative voltage outputs. These internal resistors are part of the feedback loop around the T/H amplifier, and so determine its gain characteristics. When a DDAC is assembled from components, output voltages of ±10V, ±5V, and ±2.5V, are pin selectable. The PC card assembly may be ordered as a special with a ±5V or ±2.5V output at slightly higher cost — consult factory for details. The customer can make minor wiring changes to change a standard ±10V card assembly to either ±5V or ±2.5V, as described below. See Figure 4 for the location of pins 19, 20, 21, and K.

Circuit connections for ±10V output are as shown in Figure 5. For ±5V, connect a jumper between pins 20 and 21 on the D/A converter, with the system output connected to pin 19. For ±2.5V connect the system output to pin 21 on the converter, and jumper pins 19 and 20.

The voltage output range affects the time constant, as discussed in the following section.

5. OUTPUT SETTLING

An allowance must be made for the settling time of the T/H amplifier after the T/H input switch is closed. As indicated in Figure 2, the T/H output tends to overshoot slightly before settling out when switched to the track mode. With large voltage changes, the output transition is limited by the 20V/μs slew rate of the amplifier. For 10V changes the output will settle to within ±0.01% of final value in 1800 ns. The settling time for small signal changes (not limited by slew) is limited by the bandwidth of the T/H amplifier and can be calculated from the following charts:

Output Voltage Range	Time Constant
±10V	90 ns
±5V	90 ns
±2.5V	50 ns

Number of Time Constants	Output Settles to Within
2.3	10%
4.6	1%
6.9	0.1%
9.2	0.01%

Note that the ±2.5V output range gives the fastest response. However, residual glitch is independent of range, so that the glitch is a minimum as a percent of full scale on the ±10V range.

The settling times given above also apply to the T/H DGL-13 deglitcher when it is used in other applications. The acquisition time of the DGL-13 will always be identical to its output settling time. This is because the DGL-13 can be used only in an inverting mode with a feedback capacitor.

The following example shows how to relate settling time and hold time to word rate.

Assume a ±10V output which has to make 0.10V steps and settle to .01V. Therefore, it must settle to $\left(\frac{.01 \times 100\%}{0.1}\right) = 10\%$ which takes 2.3 time constants. This is 207 ns (2.3 x 90 ns). If no external hold capacitor is used, the hold time is 50 ns. There is also a 5 ns delay from the strobe input until the T/H begins to go into the hold mode. The total time is:

207 ns	for Settling
50 ns	for Hold Time
5 ns	for Delay
262 ns	Total Interval

Word rate is 1/262 ns = 3.82 MHz. A slower rate is acceptable, but a faster rate will not allow sufficient time for settling.

At very fast word rates, the residual glitch may not have died out by the time a new hold command occurs. Since this residual glitch is the same for all transitions, the T/H acquires this glitch in addition to the transition, and it appears as a constant offset. However, since the glitch varies somewhat with temperature, this apparent offset also varies with temperature. At a 5 MHz work rate, the variation may be as much as ±30 mV over the temperature range. It can be minimized by reducing the word rate. At 2 MHz the effect is less than ±1 mV over the temperature range.

6. DC OFFSET AND PEDESTAL ADJUSTMENTS

There are provisions for DC offset and pedestal adjustments. Pedestal is the offset experienced during the hold mode due to charge being dumped on the hold capacitor during the track to hold transition. It is caused by unbalanced capacitances in the switch in the deglitcher. The values of DC offset and pedestal are nominally zero but may be ±50 mV and ±10 mV worst case respectively while the range of adjustment for the circuits shown is ±150 mV and ±20 mV respectively. The pedestal adjust should not be used to compensate for system errors.

Adjust the pedestal and offset as follows. Set the input digital bits for 0 volts, apply a normal strobe input, set the pedestal potentiometer to −15V on the wiper, and observe the system output on an oscilloscope. The output will be a series of steps with noise as is shown in Figure 6.

(a) Adjust pedestal potentiometer to zero the step height to within ±0.0005V.

(b) Adjust offset potentiometer to being the output level to 0 volts.

These two adjustments may interact slightly and should be repeated to minimize errors.

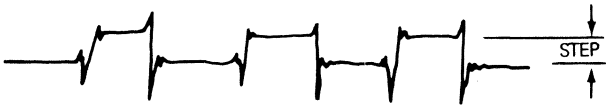


FIGURE 6. OUTPUT DIAGRAM FOR PEDESTAL ADJUSTMENT

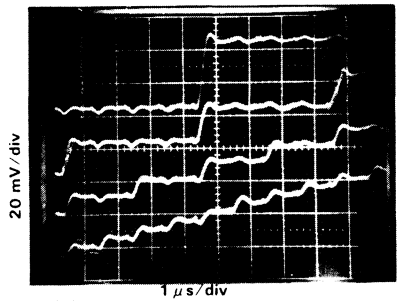


FIGURE 7. GLITCH OUTPUT WAVEFORMS

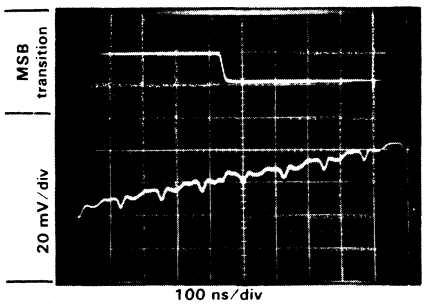


FIGURE 8. GLITCH AT MSB TRANSITION

7. REFERENCE VOLTAGE

The DDAC has an internal reference supply of 10V ±10% and is factory calibrated with this supply. Full specified performance can be obtained with ref out and ref in connected together. If an external 10V reference voltage is used, the accuracy may be affected by as much as 0.2% (Typical). The system output will be proportional to the reference voltage for external reference voltages from 0V to +10V. For reference voltages below +5V, there is an additional ±1 LSB linearity error.

Negative references cannot be accommodated. The reference input impedance is 4.44 KΩ.

8. GLITCH CHARACTERISTICS

The glitch characteristics of the DDAC are a function of interconnection layout and deglitcher design. Figures 7 and 8 illustrate the waveform of the DDAC on the PC card assembly.

Figure 7 illustrates the output waveform for incrementing at the 9th, 10th, 11th and 12th bit levels into 5 MHz filter. Update rate is 1 MHz, 20 mV/div vertical and 1μs/div horizontal.

Figure 8 illustrates the waveform around the MSB transition (upper trace). Conditions are 8 MHz word rate, 100 ns/div horizontal, 20 mV/div (lower trace) vertical, and into a 20 MHz filter. Note that while the output is incremented at the 12 bit level, there is no noticeable increase in the glitch during the MSB transition.

9. STATIC ACCURACY TEST

The linearity and gain accuracy may be tested using the arrangement shown in Figure 9. Bit weights are given in Section 3. After the pedestal and zero adjusts have been made as in Section 6, all output readings on the DVM will be within the limits stated in the specifications.

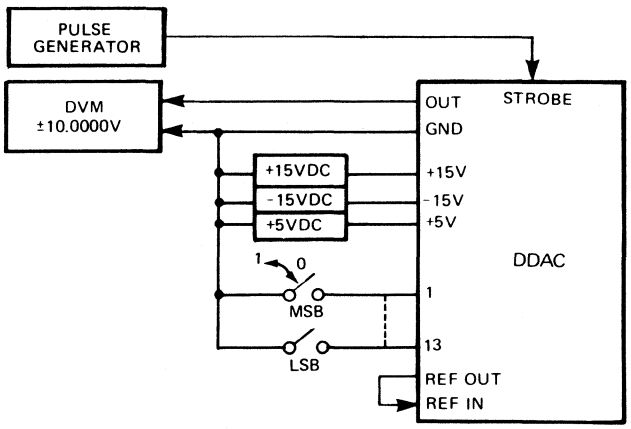


FIGURE 9. STATIC ACCURACY TEST

RELIABILITY FOR HYBRID MODULES

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All DDC hybrids are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5004/5008 except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) Ground Fixed, at 25°C, is as follows for the three DDAC hybrid modules.

	D/A Converter 2615	Deglitcher DGL-13	Coax Driver HCD-13
MTBF in Hours	967,000	783,000	4,690,000

PARTS LIST AND PIN ASSIGNMENTS

1. STANDARD P.C. CARD ASSEMBLY

Figure 5 shows pin connections for a one or two channel DDAC P.C. card assembly. One 41 pin Elco card connector is used for both channels, and only the pins labeled Channel 1 are utilized if only one channel is mounted on the card. A parts list is given in Table I. The power supply bypass capacitors labeled C1 in Figure 5 are identical and are used to reduce power supply impedances at high frequencies. Three C1 capacitors are connected at the deglitcher pins, four at the D/A converter pins, and one each at the four flip-flops, as indicated in Figure 5. The capacitors C5, C6, and C7, which serve a similar function, appear only once at the center of the P.C. board, whether one or two channels are installed. Capacitor C8, which is optional, is used to increase the hold mode pulse duration (see Section 2, Timing).

Table II is a pin assignment table for the Elco connector in the P.C. card assembly.

2. DDAC MODULE SET

The D/A Converter, deglitcher, and coax cable driver can be ordered as separate units. These units are completely interchangeable. When the user assembles his own DDAC circuit, it is recommended that the schematic of the P.C. card assembly (Figure 4) or its equivalent be used. It is important to use low power Schottky for the input register in order to keep ground currents to a minimum thereby reducing output glitch considerably. It is also important to insure a good case ground on both the D/A and deglitcher. DDC will supply prints of the P.C. card assembly artwork upon request.

Table III shows pin assignments for the three hybrid modules.

INFORMATION FOR HYBRID MODULES

SPECIFICATIONS — Typical values over full temperature range unless otherwise indicated.

I. D/A CONVERTER, P/N 2615

P/N 2615 is the same as DDC's SDAC, except that the SDAC output amplifier is not included so that only current output is available. The SDAC series data sheet may be consulted for further information.

PARAMETER	UNITS	2615-10	2615-11	2615-12
RESOLUTION	Bits		13	
ACCURACY (USING INTERNAL REF.)				
Linearity Including Offset	%F.S. Range	±0.05	±0.025	±0.0125
Linearity Tempco	ppm/°C		±2 (Max)	
Gain Accuracy at 25°C	%F.S. Range	±0.1	±0.05	±0.025
Gain Tempco	ppm/°C		±25	
DYNAMIC CHARACTERISTICS				
Settling Time to 1 LSB	ns	60 (Typ) for $R_L \leq 100\Omega$		
Output Capacitance	pF	20 (Typ)		
DIGITAL INPUTS				
Logic Type		TTL/DTL Compatible		
		Parallel Positive Logic		
13 Parallel Data Bits		Inverted offset Binary; Into One Std. TTL load		
OUTPUT (CURRENT TYPE)				
Current Range	mA	±2 (Min)		
Output Impedance	KΩ	3		
Compliance	V	−2 to +5 (Min)		
REFERENCE				
Same as Card Assembly				
POWER SUPPLIES				
+15 VDC (±2% For Full Accuracy)				
Current	mA	25 (Max)		
Abs. Max. Limits	V	0 to +18		
−15 VDC (±2% For Full Accuracy)				
Current	mA	35 (Max)		
Abs. Max. Limits	V	0 to −18		
+5 VDC (±5% For Full Accuracy)				
Current	mA	20 (Max)		
Abs. Max. Limits	V	0 to 5.5		
TEMPERATURE RANGES				
Same as Card Assembly				
PHYSICAL				
Size (24 Pin Double DDIP)	inch	0.8 x 1.4 x 0.2 (2 x 3.6 x 0.5cm)		
Weight	oz	0.38 typ (10.8g)		

II. DEGLITCHER, DGL-13 — For more detailed specifications, see the DGL-13 data sheet.

PARAMETER	UNITS	VALUE
INPUT CHARACTERISTICS		
Offset Voltage at 25°C	mV	50 (Max)
Offset Voltage Average Drift	μV/°C	40
Bias Current at 25°C	μA	1 (Typ); 5 (Max)
Abs. Max. Input Voltage	V	±15
TRANSFER CHARACTERISTICS		
Large Signal Voltage Gain		
At 25°C	V/V	25,000 (Typ); 15,000 (Min)
Full Temperature Range	V/V	10,000 (Min)
Gain Bandwidth Product for Voltage Gain ≥ 10	MHz	12
Aperture Time		
Time Delay	ns	5
Delay Uncertainty (Jitter)	ns	1
Acquisition Time		Equal to Settling Time – See Text, Sec. 5
Hold Time	ns	50 (Typ) May Be Increased by External Capacitor
Feedthrough Attenuation (Hold Mode)	dB	60 (Min)
Pedestal at 25°C	mV	±10
Droop Rate at 25°C	mV/μs	1 (Typ); 10 (Max)
Slew Rate	V/μs	20 (Typ); 15 (Min)
OUTPUT CHARACTERISTICS		
Output Voltage Swing ($R_L \geq 2K$)	V	±12 (Typ); ±10 (Min)
Output Current ($-10V \leq V_O \leq +10V$)	mA	±10 (Typ); ±5 (Min)
Abs. Max. Peak Output Current	mA	50
Full Power Bandwidth ($V_O = \pm 10V$)	KHz	330 (Typ); 250 (Min)
Short Circuit Protection		No
STOBE INPUT/OUTPUT		
Logic Type		TTL Compatible
Input Pulse		Positive Pulse, 10 ns (Min)
		Loading: 3 Std TTL Loads
Delayed Positive Output Pulse		Pulse Length Equal to Hold Time
		Drive Capability: 5 Std TTL Loads
Delayed Negative Output Pulse		Same as Positive Pulse, Except Inverted
POWER SUPPLIES		
Voltage	V	+15 ± 2% −15 ± 2% +5 ± 1%
Max Voltage Without Damage	V	+18 −18 +5.5
Current	mA	25 + load 40 + load 50 + load

INFORMATION FOR HYBRID MODULES (CONTINUED)

TEMPERATURE RANGES Same as Card Assembly		
PHYSICAL Size (24 Pin Double Dip) Weight	 inch oz	 0.8 x 1.4 x 0.2 (2 x 3.6 x 0.5 cm) .38 typ (10.8 g)

III. COAX CABLE DRIVER, HCD-13		
PARAMETER	**UNITS**	**VALUE**
TRANSFER CHARACTERISTICS		
Slew Rate (Non-Inverting)	V/μs	1000 (Min)
−3dB Bandwidth (Non-Inverting)	MHz	150 (Typ); 100 (Min)
Frequency for Full Output (Non-Inverting)	MHz	20 (Typ); 15 (Min)
Gain		1 (Typ)
INPUT CHARACTERISITCS		
Current at 25°C	μA	±100
Impedance	KΩ	100
Capacitance	pF	4 (Max)
OUTPUT CHARACTERISTICS		
Voltage	V	±11 (Typ); ±10 (Min)
Current	mA	500 (Min)
Open Loop DC Impedance	Ω	3
Short Circuit Protection		Up to 85°C Case Temperature
POWER SUPPLIES		
Voltages (±5%)	V	−15 and +15
Current Each Supply	mA	35+load
Abs. Max. Voltages	V	−18 and +18
TEMPERATURE RANGES		
Operating (Case Temp)	°C	−55 to +105
Storage	°C	−65 to +150
PHYSICAL		
Size (TO-3 Case)	inch	1.54 x 1 x 0.26 (3.9 x 2.5 x 0.7cm)
Weight	oz	0.41 typ (11.7g)

ORDERING INFORMATION FOR HYBRID MODULES

1. Order a set of three hybrid modules as follows:

DDAC − 12 − 1 − 883B

- MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883 DDC procedures
  - Blank = Same, except pre-burn in test and burn in are omitted.
- Operating Temperature Range (Case):
  - −1 = −55° C to +85° C
  - −3 = 0° C to +70° C
- Accuracy Grade:
  - 10 = ±0.05%
  - 11 = ±0.025%
  - 12 = ±0.0125%

2. Individual hybrid packages may be ordered separately as follows:

(a) D/A Converter

2615 − 12 − 1 − 883B

- MIL-STD-883 Processing:
  - 883 = Conforms to MIL-STD-883 DDC procedures
  - Blank = Same, except pre-burn in test = and burn in are omitted.
- Operating Temperature Range:
- Accuracy Grade

(b) Deglitcher Track/Hold

DGL-13 − 1 − 883B

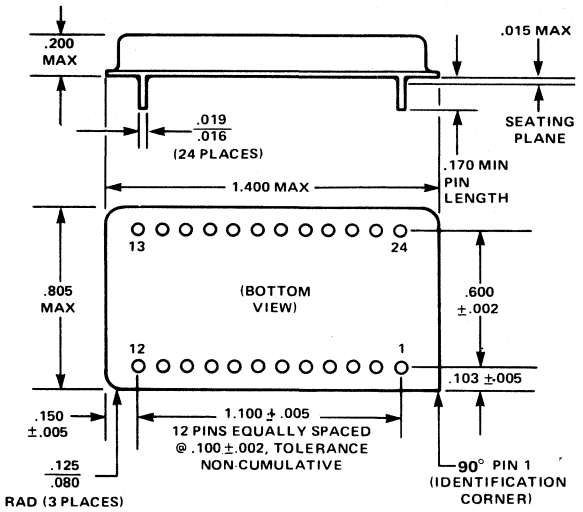
- MIL-STD-883 Processing:
  - 883 = Conforms to MIL-STD-883 DDC procedures
  - Blank = Same, except pre-burn in test and burn in are omitted.
- Temperature Range

(c) Coax Cable Driver

HCD-13 MIL-STD-883B Processing:
- 883 = Conforms to MIL-STD-883 DDC procedures
- Blank = Same, except pre-burn in test and burn in are omitted.

MECHANICAL OUTLINES

1. 24 PIN DOUBLE DIP



NOTES
1. Dimensions shown are in inches.
2. Load identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

2. COAX CABLE DRIVER (TO-3 CASE)

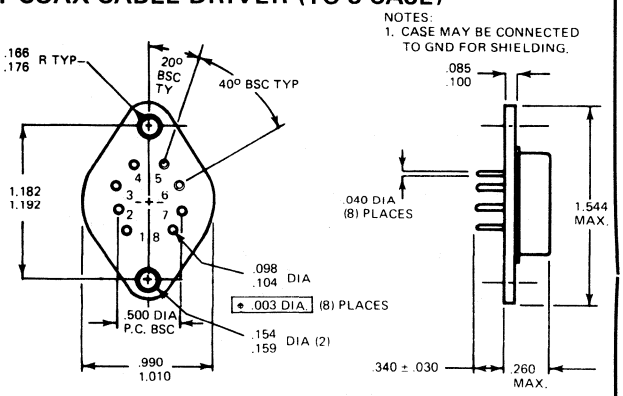


TABLE III MODULE PIN ASSIGNMENTS

Pin No.	D/A Converter P/N 2615	Deglitcher DGL-13	Driver HCD-13
1	+15VDC input	Pedestal Adjust	N.C.
2	−15VDC input	N.C.	−15VDC
3	N.C.	N.C.	N.C.
4	Ground (To Case)	Neg. strobe output	Analog output
5	N.C.	Strobe input	N.C.
6	Bit 13 (LSB) input	Positive strobe output	+15VDC
7	Bit 12 input	Ground (To Case)	N.C.
8	Bit 11 input	Delay adjust	Analog input
9	Bit 10 input	+5VDC	
10	Bit 9 input	−15VDC	
11	Bit 8 input	+15VDC	
12	Bit 7 input	Ground (To Case)	
13	Bit 6 input	Offset Adjust	
14	Bit 5 input	Analog output	
15	Bit 4 input	Feedback	
16	Bit 3 input	Ground (To Case)	
17	Bit 2 input	Analog input	
18	Bit 1 (MSB) input	N.C.	
19	Feed Back #2	N.C.	
20	±2mA Analog output	N.C.	
21	Feed Back #1	Ground (To Case)	
22	Reference input	N.C.	
23	Reference output	N.C.	
24	+5VDC input	Ground (To Case)	

INFORMATION FOR PC CARD ASSEMBLY

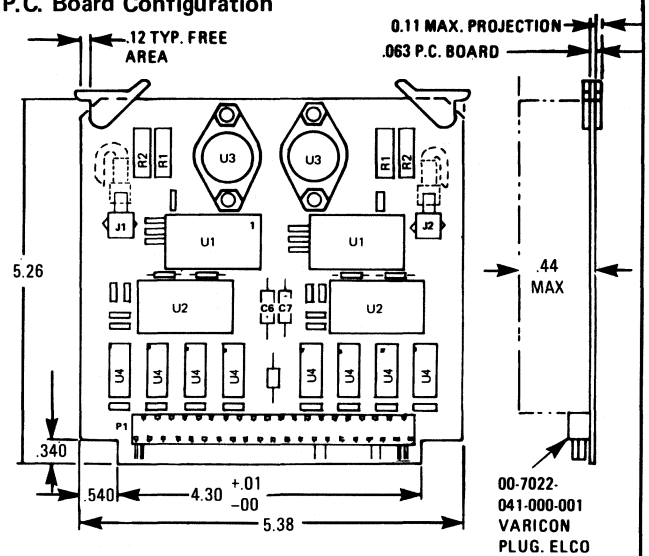
SPECIFICATIONS – PC CARD ASSEMBLY

Typical values over full temperature range and using internal reference, unless otherwise stated.

PARAMETER	UNITS	DDAC-10	DDAC-11	DDAC-12
RESOLUTION	Bits	13	13	13
ACCURACY				
Linearity Error at 25°C	%F.S. Range	±0.05	±0.025	±0.0125
Linearity Tempco	ppm/°C		2 (Max)	
Gain Accuracy at 25°C	%F.S. Range	±0.1	±0.05	±0.025
Gain Tempco	ppm/°C		±15	
Max. Zero Offset (Adjustable)	mV		±50 (Max)	
Pedestal (Adjustable)	mV		±10 (Max)	
Menotonic to	bits	10	11	12
DYNAMIC CHARACTERISTICS				
Settling Time to ±½ LSB				
±10V Full Scale				
F.S. Change	ns	1800 (Max)		
1 LSB Change	ns	50 (Max)		
±5V Full Scale				
F.S. Change	ns	1100 (Max)		
1 LSB Change	ns	50 (Max)		
±2.5V Full Scale				
F.S. Change	ns	600 (Max)		
1 LSB Change	ns	25 (Max)		
Slew Rate	V/μs	20 (Typ); 15 (Min)		
Glitch Characteristics		Typically 750 mV-ns at 1 MHz Update Rate T/H Glitch Amplitude 30mV P-P Max. into 5 MHz B.W. Filter		
DIGITAL INPUTS				
Logic Type		TTL/DTL Compatible; Two's Complement; Positive Logic; 13 Parallel Data Bits.		
Loading, Each Bit		1 Low Power Schottky Input		
Strobe (Positive Edge Triggered)		Positive Pulse ≥ 10ns into 3 Std. TTL loads.		
OUTPUT (VOLTAGE TYPE)				
Voltage Ranges	V	±10 Standard; ±5 and ±2.5 are Available as Option or With Minor Wiring Changes.		
Current	mA	±500 (Max.)		
Short Circuit Protection		Up to 85°C Case Temperature		

PARAMETER	UNITS	VALUE
REFERENCE		
Internal Reference		
Voltage	V	10 ± 10%
Current	mA	±3 (Max)
External Reference (Optional)		
Voltage	V	0 to 10
Input Impedance	KΩ	4.44 (Typ)
POWER SUPPLIES		
+15 VDC (±2% For Full Accuracy)		
Current	mA	Load + 85 (170 for 2 channels)
Abs. Max. Limits	V	0 to +18
−15 VDC (±2% For Full Accuracy)		
Current	mA	Load + 105 (210 for 2 channels)
Abs. Max. Limits	V	0 to −18
+5 VDC (±1% For Full Accuracy)		
Current	mA	Load + 125 (250 for 2 channels)
Abs. Max. Limits	V	0 to +5.5
TEMPERATURE RANGES		
Operating (Case Temperature)		
−3 Option	°C	0 to 70
−1 Option	°C	−55 to +85 (Degraded Performance to +105)
Storage	°C	−55 to +125
PHYSICAL		
Size (1 or 2 channels)	inch	5.26 x 5.38 x 0.44 (13.4 x 13.7 x 1.1cm)
Weight		
1 Channel	oz	5.21 typ (148g)
2 Channels	oz	7.26 typ (206g)

MECHANICAL OUTLINE
P.C. Board Configuration



ORDERING INFORMATION FOR CARD ASSEMBLY

Order a PC board with one or two DDAC converters as follows. Mating connectors will be supplied.

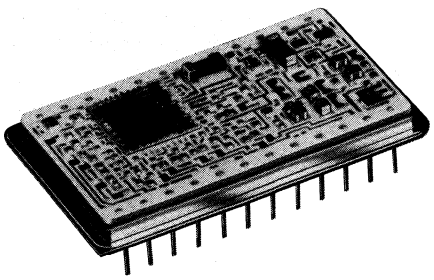
DDAC – 12 – 1 – 1CM – 883B

- MIL-STD-883 Processing:
  - 883B = Hybrid modules on PC and conform to MIL-STD-883 DDC procedures.
  - Blank = Same, except pre-burn in test and burn in are omitted.
- PC Card Configuration:
  - 1CM = One complete DDAC with cable driver
  - 2CM = Two complete DDAC channels with cable drivers
  - 1CMND = One DDAC without cable driver
  - 2CMND = Two DDAC channels without cable drivers
- Temperature Range (operating):
  - −1 = −55°C to +85°C
  - −3 = 0°C to +70°C
- Accuracy Grade:
  - 10 = ±0.05%
  - 11 = ±0.025%
  - 12 = ±0.0125%

TABLE II ELCO CONNECTOR PIN ASSIGNMENTS

Pin	Assignment	Pin	Assignment
1	Ground	21	Ground
2	Bit 4 ch 2 input	22	Ground
3	Bit 1 ch 2 (MSB) input	23	Ground
4	Bit 3 ch 2 input	24	+15VDC
5	Bit 2 ch 2 input	25	Ch 1 strobe input
6	Bit 6 ch 2 input	26	Bit 1 ch 1 (MSB) input
7	Bit 5 ch 2 input	27	Bit 2 ch 1 input
8	Bit 7 ch 2 input	28	Bit 4 ch 1 input
9	Bit 8 ch 2 input	29	Bit 5 ch 1 input
10	Bit 9 ch 2 input	30	Bit 3 ch 1 input
11	Bit 10 ch 2 input	31	Bit 7 ch 1 input
12	Bit 12 ch 2 input	32	Bit 6 ch 1 input
13	Bit 11 ch 2 input	33	Bit 11 ch 1 input
14	Bit 13 ch 2 (LSB) input	34	Bit 8 ch 1 input
15	Ch 2 reference input	35	Bit 13 ch 1 (LSB) input
16	Ch 2 reference output	36	Bit 9 ch 1 input
17	Ch 2 strobe input	37	Ch 1 reference input
18	-15VDC input	38	Bit 10 ch 1 input
19	Ground	39	Ch 1 reference output
20	+5VDC input	40	Bit 12 ch 1 input
		41	Ground

12 BIT HYBRID D/A CONVERTER
Fast Settling; Very Low Glitch; Voltage or Current Output



FEATURES

- *F.S. SETTLING TIME:*
  60 ns Max Current Output
  1 μs Max Voltage Output
- *GLITCH ENERGY*
  3 mA·ns Max Current Output
  2.5 V·ns Max Voltage Output
- *CODING:*
  Binary and Offset Binary
- *VOLTAGE RANGES:*
  ±2.5V, ±5V, ±10V, 0 to −5V, 0 to −10V
- *CURRENT RANGES:*
  ±2 mA, 0 to +4 mA
- *LINEARITY ERROR:*
  ±0.0125 % F.S.R.

DESCRIPTION

The DAC-8528 offers fast settling times and very low glitch at a moderate cost. It is a lower cost alternative to deglitched D/A converter systems. The converter is complete with an internal reference, feedback resistors, and an output amplifier. Each unit can be pin programmed for both voltage and current output ranges. The input is TTL compatible and standard packaging is a hermetically sealed 24 pin double DIP metal case.

APPLICATIONS

The high speed and low glitch of the DAC-8528 make it attractive for portable instrumentation, high speed automatic test equipment, aircraft and shipboard displays, and as the D/A in an A/D converter. The converter is a rugged, high reliability device, with standard processing based on MIL-STD-883, except for burn-in, which is an option. It can be used in remotely located and hard to access equipment where its small size and high MTBF are important.

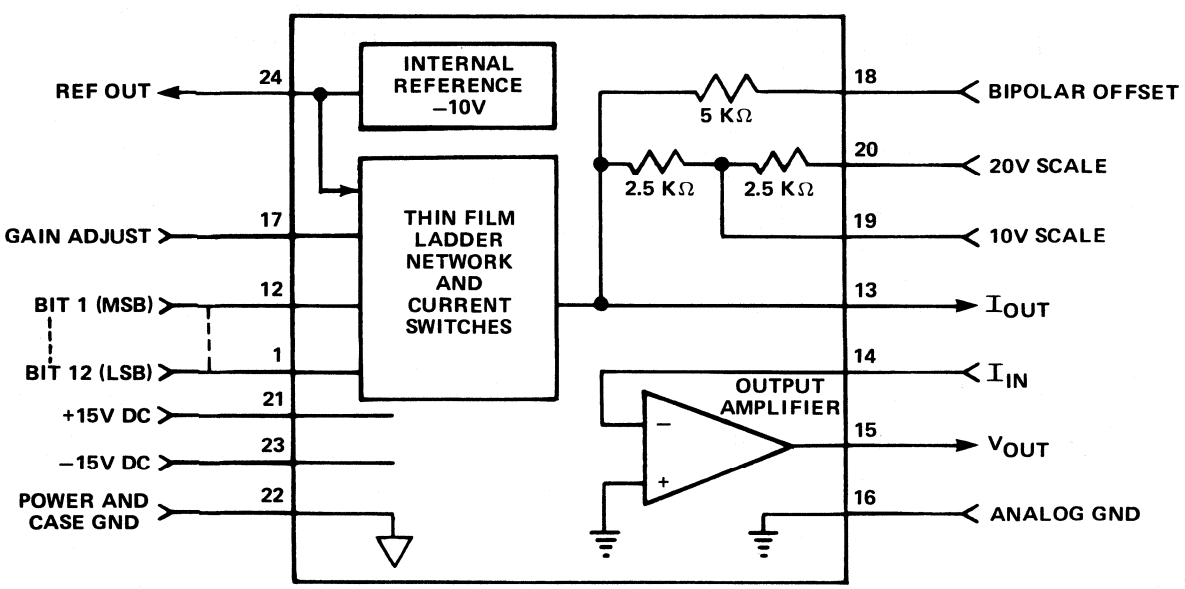


FIGURE 1. DAC 8528 BLOCK DIAGRAM

DAC-8528 SPECIFICATIONS

Typical values at 25°C and at nominal power supply voltages unless indicated otherwise.

PARAMETER	UNITS	VALUE DAC-8528-11	VALUE DAC-8528-12
RESOLUTION	Bits	12	12
ACCURACY			
Linearity Error	%F.S. Range	±0.025 max	±0.0125 max
Linearity Tempco	ppm/°C	2	1.0
Differential Nonlinearity	LSB	±2 max	±1 max
Gain Error*			
Voltage Mode	%F.S. Range	0 to ±0.4 max	0 to +0.2 max
Current Mode	%F.S. Range	±2.0 max	±1.0 max
Gain Tempco	ppm/°C	30	20
Voltage Offset			
Offset Error*	%F.S. Range	0 to +0.1	
Offset Tempco	ppm/°C	±15 max unipolar ±25 max bipolar	
Current Offset			
Offset Error*	%F.S. Range	±0.025	
Offset Tempco	ppm/°C	±1.0 max unipolar ±10 max bipolar	
*Gain and offset errors can be trimmed to zero.			
DYNAMIC CHARACTERISTICS			
		Voltage Mode	Current Mode
Update Rate	MHz	20	50
Settling Time to ±1/2 LSB			
For ±F.S. Input Change	ns	1000 max	60 max
For ±1 LSB Change	ns	50 max	20 max
Glitch			
Glitch Energy		2500 mV·ns max	3 mA·ns max
Peak-to-Peak Amplitude		120 mV max	0.3 mA max
Width at 10%		45 ns max	20 ns max
Time Constant (Small Signal)	ns	50	
Output Amplifier Bandwidth	MHz	15	
Slew Rate	V/μs	80 typ, 50 min	
OUTPUT			
Voltage Output			
Voltage Ranges	V	±2.5, ±5, ±10, 0 to −5, 0 to −10	
Max Output Current	mA	10 min	
DC Output Impedance	Ω	0.05 typ; 0.1 max	
Current Output			
Current Ranges	mA	±2, 0 to +4	
Compliance	V	±0.6 max	
Output Impedance	KΩ	1.5 typ	
Short Circuit Protection		Fully protected	
DIGITAL INPUT (TTL COMPATIBLE)			
Type		12 parallel data bits, positive logic	
Coding		Unipolar ranges: Binary Bipolar ranges: Offset Binary. Also Two's Complement if the MSB complement is supplied.	
Switching Levels			
Logic "0"		±40μA at 0V to 0.8V	
Logic "1"		±40μA at +2V to +5.5V	
INTERNAL REFERENCE OUTPUT			
Voltage	V	−10.000	
Accuracy	% of Ref	±2 max for DAC-8528-11 ±1.0 max for DAC-8528-12	
External Current Capability	mA	5 max for unipolar operation 3 max for bipolar operation (2 mA required for bipolar offset)	
POWER SUPPLIES			
Voltage	V	+15 ± 3%	−15 ± 3%
Max Voltage Without Damage	V	+18	−18
Current*	mA	30 typ 40 max	15 typ 20 max
Power Supply Rejection Ratio			
Without Trim Circuits or		DAC-8528-11	DAC-8528-12
With Trim in Voltage Mode	%F.S.R./%P.S.	±0.0048	±0.0024
With Trim in Current Mode	%F.S.R./%P.S.	±0.0060	±0.0030
*Plus load current when in voltage mode.			
TEMPERATURE RANGES (AMBIENT)			
Operating			
−1 Option	°C	−55 to +125	
−3 Option	°C	0 to +70	
Storage	°C	−65 to +125	
PHYSICAL CHARACTERISTICS			
Size (24 Pin Double DIP)	inch	1.4 x 0.8 x 0.2 (3.6 x 2.0 x 0.51 cm)	
Weight	oz	0.4 typ (11.3 g)	

TECHNICAL INFORMATION

INTRODUCTION

The DAC-8528 consists of a current output D/A converter plus an independent output amplifier, as shown in the block diagram, Figure 1. The ladder network generates currents which are discrete fractions of the ladder reference voltage. The fractions are determined by the digital inputs which control the current switches in the ladder. The ladder network operates from an internal reference, and this reference voltage is accessible at the REF OUT pin.

When the DAC-8528 is operated in the current mode, pin 13 serves at the output and the output amplifier is not used. For voltage mode operation pin 13 is connected to pin 14, and the voltage output is taken from the amplifier, pin 15.

CONNECTIONS FOR OUTPUT RANGES

Figure 2 shows pin connections for the five voltage output ranges using the internal feedback resistors and amplifier, and for two current ranges in which the current is taken directly from the ladder network. The feedback connection from pin 15 for voltage output should be made as close to the load as possible to minimize the effects of line and contact impedance.

CODING

Coding for the DAC-8528 is shown in the bit weight table, Figure 3. The current output coding conforms to the usual description of binary and offset binary coding. Because the output amplifier operates in an inverting mode, the voltage output has the opposite polarity. The values for full scale voltage (F.S.) and 1 LSB to be used in the bit weight table are as follows:

RANGE	FULL SCALE (F.S.)	1 LSB
±2.5V	2.50000V	0.00122V
±5V	5.00000V	0.00244V
±10V	10.00000V	0.00488V
0 to −5V	5.00000V	0.00122V
0 to −10V	10.00000V	0.00244V
±2 mA	2.00000 mA	0.00098 mA
0 to −4 mA	4.00000 mA	0.00098 mA

OUTPUT RANGE	BIPOLAR OFFSET CONNECTION	CONNECT LOAD TO	LOAD FEEDBACK CONNECTION	OTHER PIN CONNECTIONS
±2.5V	18 to 24	15	15 to 19	13 to 14, 13 to 20
±5V	18 to 24	15	15 to 19	13 to 14
±10V	18 to 24	15	15 to 20	13 to 14
0 to −5V	18 to 16	15	15 to 19	13 to 14, 13 to 20
0 to −10V	18 to 16	15	15 to 19	13 to 14
±2 mA	18 to 24	13	–	–
0 to −4 mA	–	13	–	–

FIGURE 2. CONNECTIONS FOR VOLTAGE AND CURRENT RANGES

CURRENT OUTPUT *		DIGITAL BIT INPUTS												VOLTAGE OUTPUT	
UNIPOLAR	BIPOLAR													UNIPOLAR	BIPOLAR
BINARY	OFFSET BINARY	MSB 1	2	3	4	5	6	7	8	9	10	11	LSB 12		
+F.S. −1 LSB	+F.S. −1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	−F.S. +1 LSB	−F.S. +1 LSB
+3/4 F.S.	+1/2 F.S.	1	1	0	0	0	0	0	0	0	0	0	0	−3/4 F.S.	−1/2 F.S.
+1/2 F.S. +1 LSB	+1 LSB	1	0	0	0	0	0	0	0	0	0	0	1	−1/2 F.S. −1 LSB	−1 LSB
+1/2 F.S.	0	1	0	0	0	0	0	0	0	0	0	0	0	−1/2 F.S.	0
+1/2 F.S. −1 LSB	−1 LSB	0	1	1	1	1	1	1	1	1	1	1	1	−1/2 F.S. +1 LSB	+1 LSB
1/4 F.S.	−1/2 F.S.	0	1	0	0	0	0	0	0	0	0	0	0	−1/4 LSB	+1/2 F.S.
+1 LSB	−F.S. +1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	−1 LSB	+F.S. −1 LSB
0	−F.S.	0	0	0	0	0	0	0	0	0	0	0	0	0	+F.S.

*Current direction is defined as positive for currents leaving the V output.

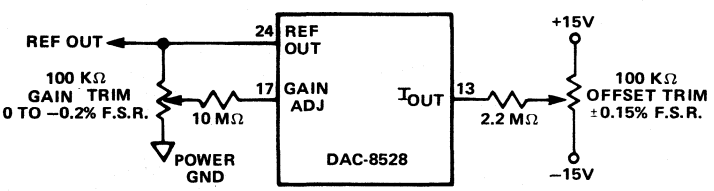
FIGURE 3. BIT WEIGHT TABLE

TRIM ADJUSTMENTS

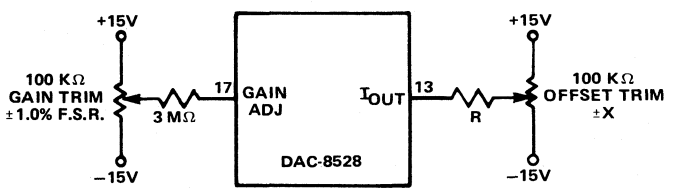
The gain and offset errors are trimmed at the factory to within the limits listed in the specifications table. With the optional trim adjustment circuits shown in Figure 4, both errors can be trimmed to zero, making the overall accuracy equal to the linearity. The fixed resistors shown in Figure 4 should be located close to the converter pins to reduce noise, and the potentiometers should have a tempco of 100 ppm/°C or less.

To trim the offset, apply the all zero's digital code. As shown in the bit table, Figure 3, this corresponds to 0 output for unipolar coding, −F.S. for bipolar current output, and +F.S. for bipolar voltage output. Adjust the offset trim potentiometer for the proper current or voltage output value in each case.

After trimming the offset, apply the all one's code to trim the gain. This corresponds to +F.S. −1 LSB for current output, and −F.S. +1 LSB for voltage output. Adjust the output to this value with the gain potentiometer.



A. VOLTAGE MODE TRIM



B. CURRENT MODE TRIM

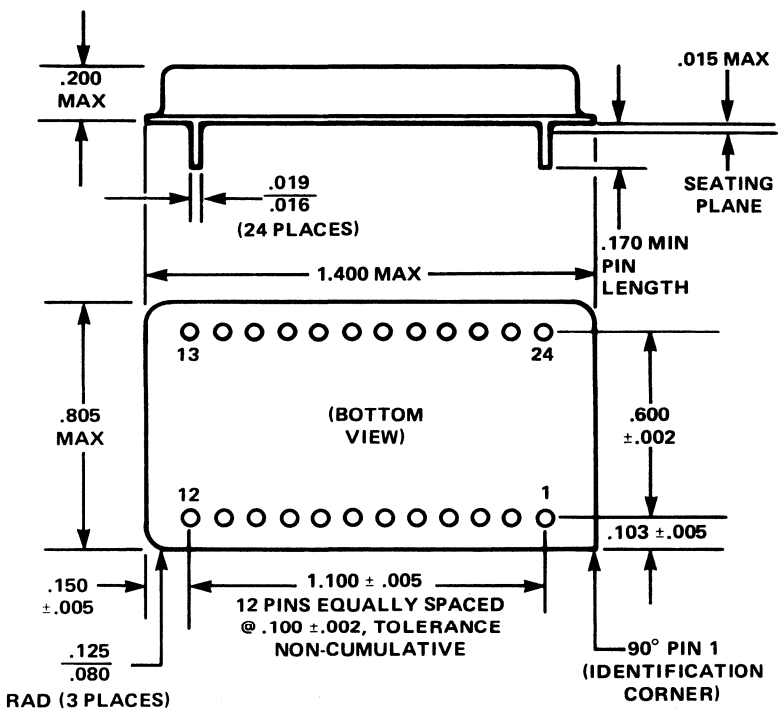
	R	X
UNIPOLAR	2.2 MΩ	±0.15% F.S.R.
BIPOLAR	0.62 MΩ	±0.6% F.S.R.

FIGURE 4. OPTIONAL TRIM CIRCUITS

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 12 (LSB)	13	I_{OUT}
2	Bit 11	14	I_{IN}
3	Bit 10	15	V_{OUT}
4	Bit 9	16	Analog GND
5	Bit 8	17	Gain Adjust
6	Bit 7	18	Bipolar Offset
7	Bit 6	19	10V Scale
8	Bit 5	20	20V Scale
9	Bit 4	21	+15V DC
10	Bit 3	22	Power & Case GND
11	Bit 2	23	−15V DC
12	Bit 1 (MSB)	24	Ref Out

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES
1. Dimensions shown are in inches.
2. Load identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Case tied to analog ground.

DYNAMIC CHARACTERISTICS

Glitches at the output of the DAC-8528 are caused by a combination of digital data skew and stray coupling between the digital inputs and the analog output. The data skew coming into the DAC-8528 can be decreased by using a low skew holding register such as AMD type 74LS175. The physical layout around the unit should also be done carefully to minimize external coupling from input to output. Techniques such as ground planes between digital and analog runs are recommended. To optimize settling time, and to make the settling time independent of the driver characteristics, 2.2 KΩ, 1/8W pullup resistors, to the +5V logic supply, are suggested for all logic inputs.

POWER SUPPLIES AND GROUNDS

Care must be taken when distributing power supplies and grounds in high speed system to obtain optimum performance. It is recommended that 1μF tantalum capacitors be used to bypass each supply to supplement internal bypassing. The power ground, which is connected to the case, is not internally connected to analog ground and the two grounds must be connected externally.

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

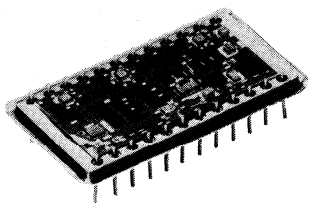
All DDC-8528's are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5004/5008 except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number.

ORDERING INFORMATION

DAC-8528 – 12 – 1 – 883B

- 883B: MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883, DDC procedures.
  - Blank = Same, except pre burn in test and burn in are omitted.
- 1: Operating Temperature Range (Ambient):
  - −1 = −55°C to +125°C
  - −3 = 0°C to +70°C
- 12: Linearity:
  - 12 = 12 bits (±0.0125%)
  - 11 = 11 bits (±0.025%)

12 BIT HYBRID D/A CONVERTER
Input Register With Strobe; 5μs Voltage Settling Time



FEATURES

- *STROBED REGISTER STORES DIGITAL INPUT*
- *CODING:*
  Complementary Binary
  Complementary Offset Binary
- *VOLTAGE RANGES:*
  ±5V, ±10V, 0 to +10V
- *LINEARITY ERROR:*
  ±0.0125% F.S.R.

DESCRIPTION

The key feature of the DAC-SL D/A converter is the input register which can be used to store the digital input. The DAC-SL is complete with an internal reference, feedback resistors, and an output amplifier included in a hermetically sealed 24 pin double DIP metal case. The input is TTL compatible and voltage ranges are pin programmable. An external reference can be used so that the output can track a system reference.

APPLICATIONS

The DAC-SL is used in applications which can take advantage of its input register and relatively fast settling time. It is a rugged, high reliability device; standard processing is based on MIL-STD-883 except for burn-in, which is an option. Applications areas include medical instrumentation, CRT displays, and avionics systems. The DAC-SL can be used in remotely located and hard to access equipment because of its small size and high MTBF.

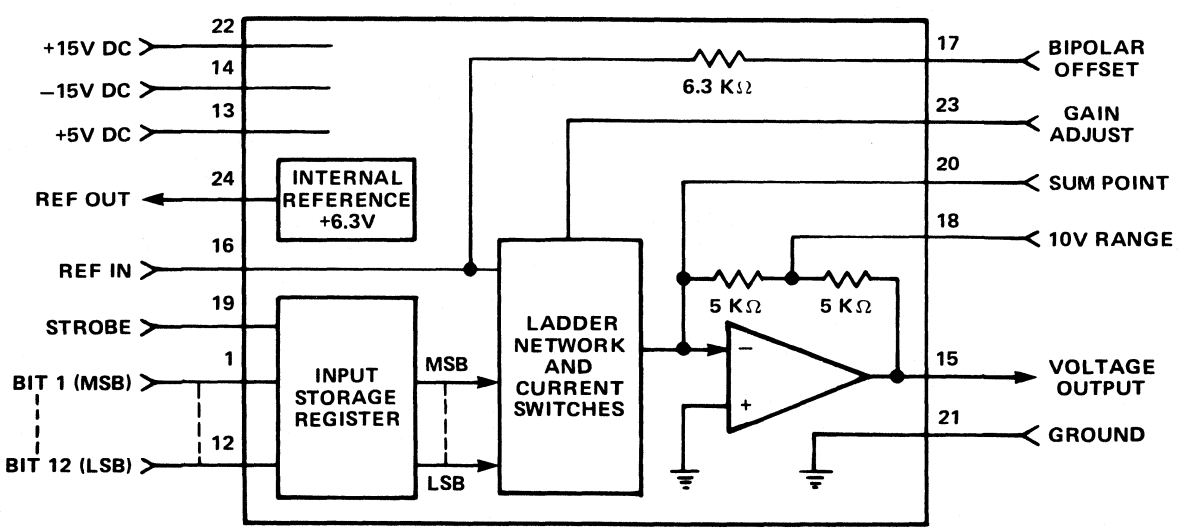


FIGURE 1. DAC-SL BLOCK DIAGRAM

DAC-SL SPECIFICATIONS

Typical values at 25°C and at nominal power supply voltages.

PARAMETER	UNITS	VALUE DAC-SL-11	DAC-SL-12
RESOLUTION	Bits	12	12
ACCURACY (USING INTERNAL REFERENCE)			
Linearity Error	% F.S. Range	±0.025 max	±0.0125 max
Linearity Tempco	ppm F.S.R./°C	±1.5 typ; ±3 max	±1.0 typ; ±2 max
Gain Error*	% F.S. Range	±0.4%	±0.2%
Gain Tempco	ppm F.S.R./°C	±20 typ; ±40 max	±15 typ; ±30 max
Offset Error*	% F.S. Range	±0.1 max	±0.05 max
Offset Tempco	ppm F.S.R./°C	±5 typ; ±8 max	±3 typ; ±5 max
Differential Linearity Error	LSB	±1.0 typ; ±2 max	±½ typ; ±1 max
Monotonic to	Bits	11	12
*Gain and Offset errors can be trimmed to zero.			
DYNAMIC CHARACTERISTICS			
Update Rate	MHz	3 max	
Settling Time to 0.01% F.S.R.			
F.S. Change on ±10V Range	µs	5 typ; 10 max	
F.S. Change on ±5V or 0 to +5V Ranges	µs	3 typ; 6 max	
LSB Change, All Ranges	µs	1.5 typ; 3 max	
Slew Rate	V/µs	15 typ; 10 min	
OUTPUT			
Voltage Ranges	V	±5, ±10, 0 to +10	
Max Current	mA	10 typ; 5 min	
DC Input Impedance	Ω	0.1 max	
DIGITAL INPUT (TTL COMPATIBLE)			
Input Voltage Levels	V	Logic "0": 0 to +0.8 Logic "1": +2 to +5.5	
Max Voltage Without Damage	V	7	
12 Parallel Data Bits			
Pulse Shape		Positive true pulse, 20 ns min, must remain valid until strobe returns to logic high	
Coding		Unipolar: Complementary Binary Bipolar: Complementary Offset Binary Also Complementary Two's Complement if the MSB Complement is provided.	
Loading		Logic "0": −400µA at 0.4V Logic "1": +20µA at 2.7V	
Strobe for Input Register			
Pulse Shape		Negative pulse, 20 ns min, leading edge simultaneous with or follows leading edge of parallel bits. Logic "0" = track digital input Logic "1" = hold data bits	
Loading		Logic "0": −720µA at 0.4V Logic "1": +40µA at 2.7V	
REFERENCE			
Internal Reference			
Voltage	V	6.3 ± 0.3	
Voltage Drift	ppm/°C	20 max	
Current Output	mA	0.1 max	
Output Impedance	Ω	20	
Reference Input			
Voltage	V	+6.3 ± 5%	
Current Requirement	mA	1.2	
POWER SUPPLIES			
Voltage	V	+15 ± 3% / −15 ± 3% / +5 ± 3%	
Max Voltage Without Damage	V	+18 / −18 / +7	
Current	mA	15 typ / 5 typ / 30 typ 25 max / 10 max / 45 max	
Power Supply Rejection Ratio	% F.S.R./% P.S.	.02 typ / .002 typ .05 max / .01 max	
Power Consumption	W	0.45 typ; 0.75 max	
TEMPERATURE RANGES (AMBIENT)			
Operating			
−1 Option	°C	−55 to +125	
Storage	°C	−65 to +125	
PHYSICAL CHARACTERISTICS			
Size (24 Pin Double DIP)	inch	0.8 x 1.4 x 0.2 (2 x 3.6 x 0.5 cm)	
Weight	oz	0.4 typ (11.3g)	

TECHNICAL INFORMATION

PIN CONNECTIONS AND VOLTAGE RANGES

In normal operation the following connections are made (see Figure 1, Block Diagram). The REFERENCE IN is tied to the REFERENCE OUT unless an external reference is used. The BIPOLAR OFFSET is tied to the SUM POINT for bipolar operation or to GND for unipolar operation. The load is connected between the VOLTAGE OUTPUT and GND. The SUM POINT should not be used as an output. On the ±10V range, the feedback is an internal connection, but on the ±5V and 0 to +10V ranges the feedback is connected externally between pin 15 and pin 18, the 10V RANGE. This feedback connection should be made as close to the load as possible to minimize the effects of line and contact impedance.

The bipolar and feedback connections which determine the voltage ranges are summarized in the following table:

VOLTAGE RANGE	BIPOLAR OFFSET CONNECTION	FEEDBACK CONNECTION
±5V	17 to 20	15 to 18
±10V	17 to 20	—
0 to +10V	17 to 21	15 to 18

CODING AND TRIM ADJUSTMENTS

Coding for the DAC-SL is shown in the bit weight table, Figure 2. The values for full scale voltage (F.S.) and 1 LSB to be used in the bit weight table are as follows:

RANGE	FULL SCALE (F.S.)	1 LSB
±5V	5.00000V	0.00244V
±10V	10.00000V	0.00488V
0 to +10V	10.00000V	0.00244V

The trim adjustment circuits shown in Figure 3 are optional. The gain and offset errors are trimmed at the factory to within the limits listed in the specifications table. If both errors are trimmed to zero, the over-all accuracy will be equal to the linearity. The 6.8 MΩ and 9 MΩ fixed resistors in Figure 3 should be located close to the converter pins to reduce noise, and the two potentiometers should have a tempco of not more than 100 ppm/°C.

To trim the offset, apply the all one's digital code, which corresponds to 0 volts output for the unipolar range, and to −F.S. for the bipolar ranges (see Figure 2). Adjust the offset potentiometer for the proper value for the output voltage.

After trimming the offset, apply the all zero's digital code to trim the gain. This code corresponds to +F.S. − 1 LSB, and the output should be adjusted to this value with the gain potentiometer.

ANALOG OUTPUT VOLTAGE		DIGITAL BIT INPUTS											
UNIPOLAR COMPLEMENTARY BINARY	BIPOLAR COMPLEMENTARY OFFSET BINARY	MSB 1	2	3	4	5	6	7	8	9	10	11	LSB 12
+F.S. – 1 LSB	+F.S. – 1 LSB	0	0	0	0	0	0	0	0	0	0	0	0
+3/4 F.S.	+1/2 F.S.	0	0	1	1	1	1	1	1	1	1	1	1
+1/2 F.S. + 1 LSB	+ 1 LSB	0	1	1	1	1	1	1	1	1	1	1	0
+1/2 F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1
+1/2 F.S. – 1 LSB	–1 LSB	1	0	0	0	0	0	0	0	0	0	0	0
1/4 F.S.	–1/2 F.S.	1	0	1	1	1	1	1	1	1	1	1	1
+ 1 LSB	–F.S. + 1 LSB	1	1	1	1	1	1	1	1	1	1	1	0
0	–F.S.	1	1	1	1	1	1	1	1	1	1	1	1

Note: For Complementary Two's Complement coding, the bit values are identical to those for Complementary Offset Binary coding in the table, except that the MSB is reversed (MSB bits "1" become "0", and bits "0" become "1").

FIGURE 2. BIT WEIGHT TABLE

STROBE TIMING

A timing diagram for the input register STROBE is shown in Figure 4. The data bits must remain valid for at least 20 ns. The leading edge of the strobe pulse can be simultaneous with the leading edge of the data pulse, or it can be delayed. The data bits must remain valid until the strobe pulse is complete. It is possible for the data bits and strobe to begin and end together in phase.

POWER SUPPLY DECOUPLING

Power supply decoupling capacitors should be used to improve noise rejection. Connect two capacitors to ground at each of the three power supply input pins, as close to the converter as possible. One capacitor should be 1 – 10μF tantalum or electrolytic; the other should be 0.01μF ceramic for high frequency bypassing.

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All DDC hybrids are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5004/5008 except for burn in, which is optional. To specify preburn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) is 2,200,000 hours, Ground Fixed, at 25°C.

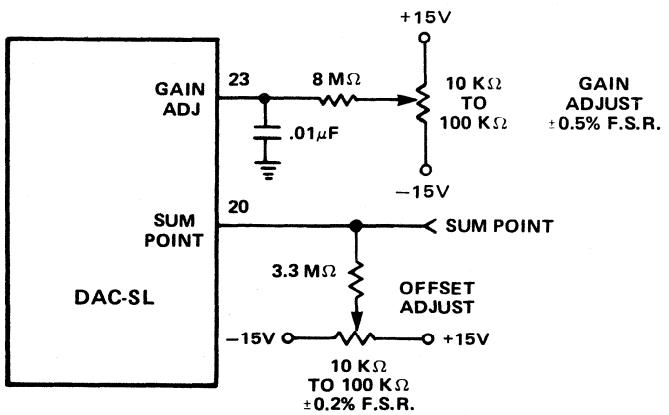


FIGURE 3. TRIM ADJUSTMENT CIRCUITS

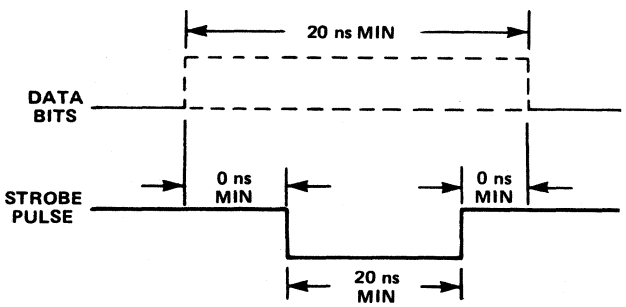
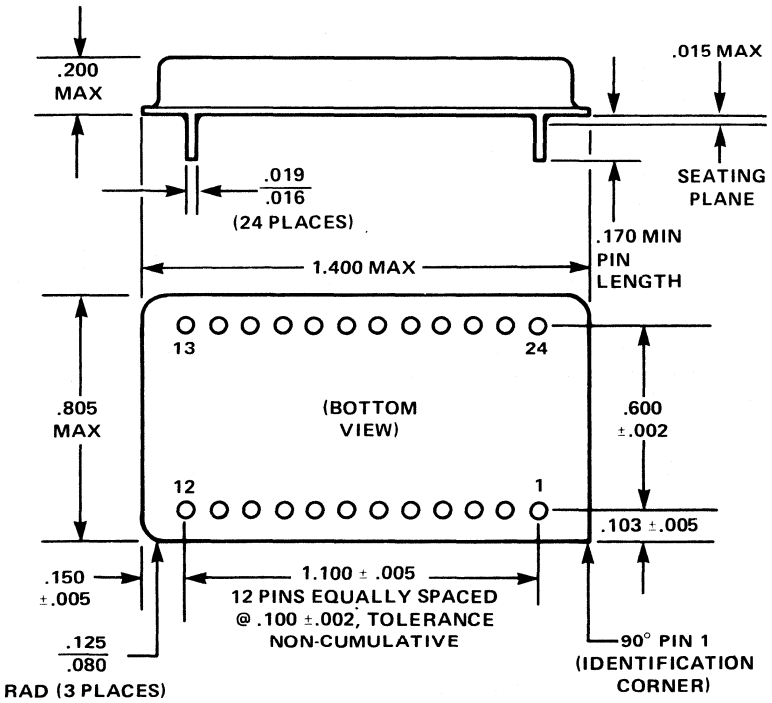


FIGURE 4. STROBE TIMING DIAGRAM

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES
1. Dimensions shown are in inches.
2. Load identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

ORDERING INFORMATION

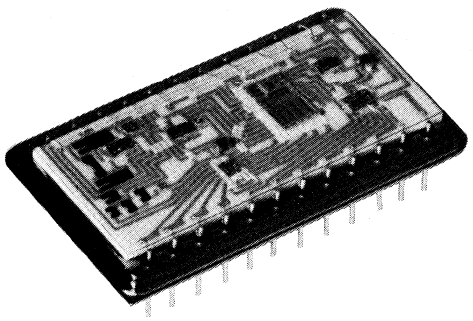
DAC-SL – 12 – 1 – 883B

- 883B: MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883 DDC procedures
  - Blank = Same, except pre burn in test and burn in are omitted.
- 1: Operating Temperature Range (Ambient):
  - –1 = –55°C to +125°C
- 12: Linearity:
  - 12 = 12 bits (±0.0125%)
  - 11 = 11 bits (±0.025%)

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 1 (MSB)	13	+5V DC
2	Bit 2	14	–15V DC
3	Bit 3	15	Voltage Out
4	Bit 4	16	Ref In
5	Bit 5	17	Bipolar Offset
6	Bit 6	18	10V Range
7	Bit 7	19	Strobe
8	Bit 8	20	Sum Point
9	Bit 9	21	Ground
10	Bit 10	22	+15V DC
11	Bit 11	23	Gain Adjust
12	Bit 12 (LSB)	24	Ref Out

12 BIT HYBRID D/A CONVERTER
WIDE OPERATING TEMPERATURE RANGE
100ns Current Settling; 3 μs Voltage Settling



DESCRIPTION

The DDC DAC87 is a 12 bit, wide temperature range (-55°C to +125°C) and high accuracy digital to analog hybrid converter. Its features include form-fit-function replacement for DAC87, linearity error of ±½ LSB, throughput rates up to 6MHz* and guaranteed monotonicity. The voltage output version, DDC DAC87-CBI-V has five pin programmable output ranges, while the current output unit, DDC DAC87-CBI-I, may be used either for direct current drive or with an external op-amp. The DDC DAC87's input is TTL compatible, requiring 1 standard TTL load drive capability and will accept complementary binary and complementary offset binary codes. The unit is packaged in a hermetically sealed 24 pin Double DIP.

APPLICATIONS

Because of its high performance, pin programmable features, and relatively low cost the DDC DAC87 has many applications. These include portable instrumentation, aircraft and shipboard displays, and the D/A in a successive approximation type analog to digital converter. These converters are rugged devices, which can be used in remotely located and hard to access equipment where small size and high MTBF are important.

*Throughput rate for 1 LSB change.

FEATURES

- *GUARANTEED SPECIFICATIONS FROM −55° C TO +125° C*
- *3,000,000 HOUR MTBF*
- *PIN COMPATIBLE WITH DAC87, DAC85*
- *HERMETICALLY SEALED 24 PIN DOUBLE DIP PACKAGE*
- *VOLTAGE AND CURRENT OUTPUT MODELS*
- *MIL-STD-883B SCREENING AVAILABLE*

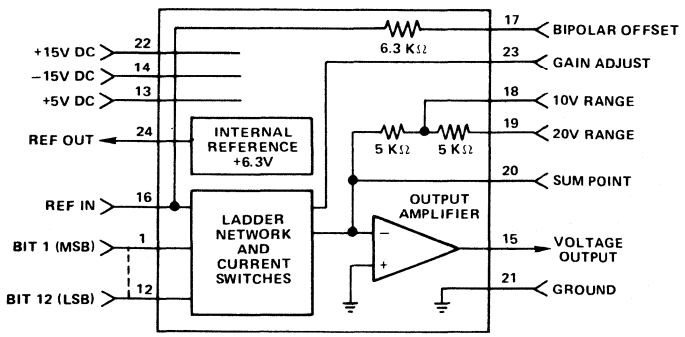


FIGURE 1. BLOCK DIAGRAM FOR VOLTAGE OUTPUT (DDC DAC87-CBI-V)

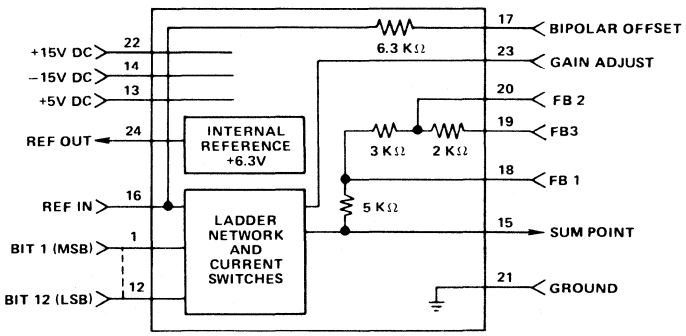


FIGURE 2. BLOCK DIAGRAM FOR CURRENT OUTPUT (DDC DAC87-CBI-I)

SPECIFICATIONS

Typical Values at 25°C and at nominal power supply voltages unless otherwise indicated:

PARAMETER	UNIT	VALUE		
RESOLUTION	bits	12		
ACCURACY		**MIN**	**TYP**	**MAX**
Linearity Error (+25°C)	LSB			±½
—55°C to +125°C	LSB			±1
Differential Linearty Error	LSB			+1 −¾
Gain Error (Trimmable to zero)	%		±0.1	±0.2
Gain Tempco (Using internal feedback resistors)	ppm/°C			±15
Offset Error (Trimmable to zero)	%FSR		±0.05	±0.1
Offset Tempco (Using internal feedback resistors)				
Unipolar Ranges	ppm FSR/°C		±1	±3
Bipolar Ranges	ppm FSR/°C		±5	±15
Monotonicity	bits	12		
DYNAMIC CHARACTERISTICS				
Voltage Output (DDC DAC87-CBI-V)				
Settling Time to ±0.01%FSR				
For Full Scale Change				
With 10k ohm feedback	µs			5
With 5k ohm feedback	µs			3
For 1 LSB Change	µs			1.5
Slew Rate	V/µs		20	
Current Output (DDC DAC87-CBI-I)				
Settling Time to ±0.01%FSR				
Full Scale Change				
With 10 to 100 ohm load	ns			100
With 1k ohm load	ns			500
For 1 LSB Change	ns		50	
DIGITAL INPUT				
Type (TTL Compatible)		12 parallel data bits, positive logic		
Coding		Unipolar ranges: Complementary Binary Bipolar ranges: Complementary Offset Binary and Two's Complement if the MSB Complement is supplied		
Loading		1 std. TTL load		
Maximum Logic Input Voltage Without Damage		Do not exceed voltage of +5 power supply		
ANALOG OUTPUT				
Voltage Output (DDC DAC87-CBI-V)				
Ranges (Typical Values)	V	±2.5 ±5 ±10 0 to +10 0 to +5		
Output Current	mA	±5 min		
Output Impedance		0.05 typ		
Short Circuit Protection		Fully protected		
Current Output (DDC DAC87-CBI-I)		**BIPOLAR** | **UNIPOLAR**		
Ranges (Typical Values)	ma	±1 | 0 to -2		
Output Impedance	kΩ	4.4 | 15		
Compliance	V	±2.5 max | ±2.5 max		
REFERENCE		**MIN**	**TYP**	**MAX**
Internal Reference				
Voltage	V		+6.3	
Current Capability	µA			200
Reference Input				
Voltage/Regulation	V		+6.3 ±10%	
Voltage Without Damage	V			+10
Current Requirements	mA		1.1	
POWER SUPPLIES				
Power Supply Requirements				
Voltages	V	+15 ±0.5	-15 ±0.5	+5 ±0.25
Maximum Voltage Without Damage	V	+18	-18	+7
Current**	mA	20 typ 25 max	20 typ 25 max	10 typ 20 max
Power Supply Sensitivity	%FSR/%P.S.	±0.002	±0.002	±0.002
** Plus load current for +15V and -15V power supplies				
TEMPERATURE RANGES (Ambient)				
Operating	°C	-55 to +125		
Storage	°C	-55 to +150		
PHYSICAL CHARACTERISTICS				
Size (24 Pin Double DIP)	in	0.8 x 1.4 x 0.2 (20 x 36 x 5 mm)		
Weight	oz	0.4 (11.3g)		

INTRODUCTION

Figure 1 and Figure 2 are block diagrams of the voltage output and current output models, respectively, of the DDC DAC87. Note that the two models have different feedback resistors and different pin connections in the output section. In both models the resistor network generates currents which are discrete fractions of the reference voltage. The fractions are determined by the digital inputs which control the current switches. The DDC DAC87 is calibrated with its own internal reference, but an external reference can be used instead. When the internal reference is used, pin 16 must be connected to pin 24.

CODING

The coding for both voltage and current output models is as shown in Figure 3. The full scale voltage (F.S.) and LSB values for all voltage and current ranges are:

RANGE	FULL SCALE (FS)	1 LSB
±2.5V	2.50000V	0.00122V
±5V	5.00000V	0.00244V
±10V	10.00000V	0.00488V
0 to +5V	5.00000V	0.00122V
0 to +10V	10.00000V	0.00244V
±1 mA	1.00000 mA	0.00049 mA
0 to —2 mA	2.00000 mA	0.00049 mA

COMPLEMENTARY

ANALOG OUTPUT VOLTAGE		DIGITAL BIT INPUTS											
UNIPOLAR COMPLEMENTARY BINARY	BIPOLAR OFFSET BINARY	1	2	3	4	5	6	7	8	9	10	11	12
+F.S — 1 LSB	+F.S. — 1 LSB	0	0	0	0	0	0	0	0	0	0	0	0
+3/4 F.S.	+1/2 F.S.	0	0	1	1	1	1	1	1	1	1	1	1
+1/2 F.S. + 1 LSB	+ 1 LSB	0	1	1	1	1	1	1	1	1	1	1	0
+1/2 F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1
+1/2 F.S. — 1 LSB	—1 LSB	1	0	0	0	0	0	0	0	0	0	0	0
1/4 F.S.	—1/2 F.S.	1	0	1	1	1	1	1	1	1	1	1	1
+ 1 LSB	—F.S. + 1 LSB	1	1	1	1	1	1	1	1	1	1	1	0
0	—F.S.	1	1	1	1	1	1	1	1	1	1	1	1

Notes:
1. For current output models (DDC DAC87-CBI-I), the current direction is defined as positive for currents entering the output.
2. For Complementary Two's Complement coding, the bit values are identical to those for Complementary Offset Binary coding in the above table, except that the MSB is reversed (MSB bits "1" become "0" and bits "0" become "1") using an external inverter.

FIGURE 3. BIT WEIGHT TABLE

OFFSET AND GAIN TRIM

The offset and gain errors are trimmed at the factory to within the limits listed in the specifications table. If both errors are trimmed to zero, the over-all accuracy will be equal to the linearity. Figure 4 shows trim adjustment circuits that apply to both the voltage and current output models of the DDC DAC87. The 3.9MΩ and 18MΩ fixed resistors should be located close to the converter pins to reduce noise, and the two potentiometers should have a temperature coefficient of 100 ppm/°C or less.

To trim the offset, apply the all one's digital code, which corresponds to 0 input for a unipolar range and —F.S. for a bipolar range (see Figure 3). Adjust the offset potentiometer for the proper value of analog output.

After trimming the offset, trim the gain by applying the all zero's digital code. This corresponds to +F.S. — 1 LSB, and the output should be adjusted to this value with the gain trim potentiometer.

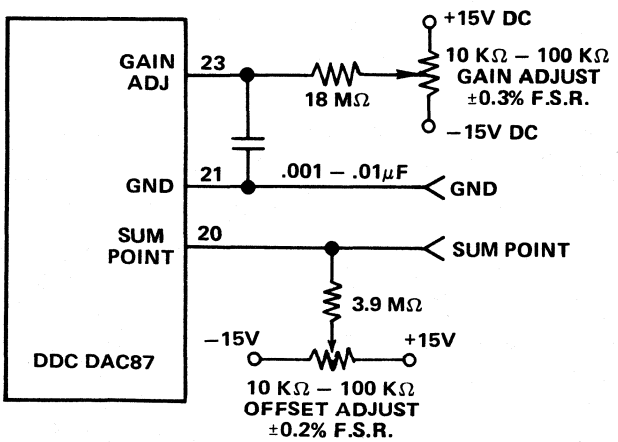


FIGURE 4. OFFSET AND GAIN TRIM CIRCUITS

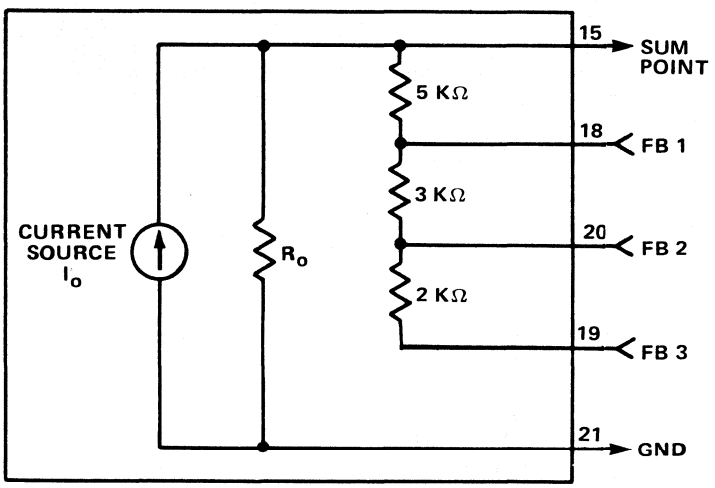


FIGURE 5. EQUIVALENT CIRCUIT FOR (DDC DAC87-CBI-I)

OUTPUT CONNECTIONS FOR (DDC DAC87-CBI-V)

The following table shows pin connections for the five voltage ranges of voltage output model of the DDC DAC87.

Voltage Range	Load Feedback Connection	Bipolar Offset Connection	Other Pin Connections
±2.5V	15 to 18	17 to 20	19 to 20
±5V	15 to 18	17 to 20	—
±10V	15 to 19	17 to 20	19 to 15
0 to +5V	15 to 18	17 to 21	19 to 20
0 to +10V	15 to 18	17 to 21	—

The output load in all cases is connected to pin 15, the voltage output. The feedback connection from pin 15 should be made as close to the load as possible to minimize the effects of line and contact impedance.

OUTPUT CONNECTIONS FOR DDC DAC87-CBI-I

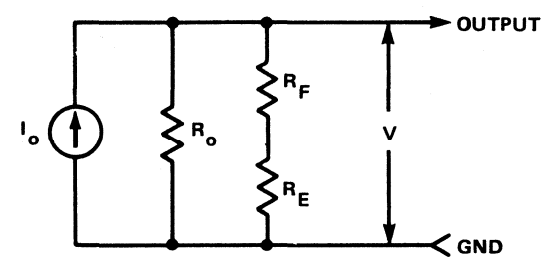
Figure 5 shows the equivalent circuit for the current output model of the DDC DAC87. The converter is represented by a current source with a parallel resistance R_o and a chain of three feedback resistors. The output is unipolar if the Bipolar Offset is connected to ground, and bipolar if it is connected to the Sum Point.

Three configurations for using the DDC DAC87-CBI-I will be discussed. In the first, the converter output current is used to drive a resistive load directly, and the internal feedback resistors are used to scale the output voltage. In the second, the internal resistors are used to provide feedback for an external op-amp. In the third, an external op-amp is used with an external feedback resistor.

1. Driving a Resistive Load. An equivalent diagram for driving a resistive load and using the internal resistors to regulate the load voltage is shown in Figure 6. I_O and R_O have the values given in Figure 5. R_F represents the pin programmed internal feedback resistance and R_E represents additional external resistance in series with R_F. The equations in Figure 6 show the relationship between the voltage V across the load and $R_F + R_E$. Two examples will be discussed, unipolar coding with an output voltage range of 0 to —2V, and bipolar coding with a voltage range of ±1V. To obtain the least temperature drift, R_F should be made as large as possible relative to R_E.

For a 0 to —2V range:

$$R_F + R_E = \frac{(15{,}000)\ (2)}{(15{,}000)\ (.002) - 2} = 1071.4\Omega$$



$$V = \frac{I_o R_o (R_F + R_E)}{R_o + R_F + R_E} \quad \text{OR} \quad R_F + R_E = \frac{R_o V}{R_o I_o - V}$$

R_E = EXTERNAL METAL FILM RESISTOR

FIGURE 6. EQUIVALENT CIRCUIT FOR DRIVING A RESISTIVE LOAD

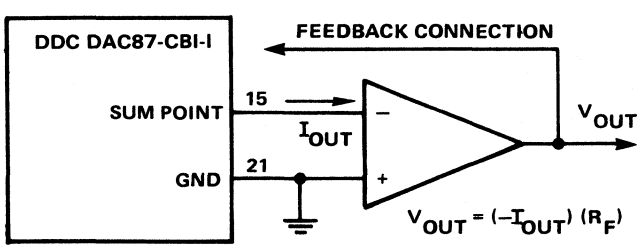


FIGURE 7. CONNECTIONS FOR EXTERNAL OP-AMP USING INTERNAL FEEDBACK RESISTOR

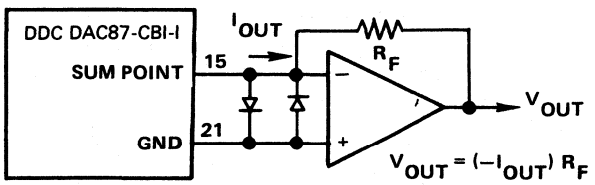


FIGURE 8. CONNECTIONS FOR EXTERNAL OP-AMP USING AN EXTERNAL FEEDBACK RESISTOR

PIN CONNECTION TABLE

FUNCTION		FUNCTION		
PIN	BOTH MODELS	PIN	DDC DAC87-CBI-V	DDC DAC87-CBI-I
1	Bit 1 (MSB)	13	+5 V DC	
2	Bit 2	14	—15 V DC	
3	Bit 3	15	Voltage Out	Sum Point
4	Bit 4	16	Ref In	
5	Bit 5	17	Bipolar Offset	
6	Bit 6	18	10V Range	FB 1
7	Bit 7	19	20V Range	FB 3
8	Bit 8	20	Sum Point	FB 2
9	Bit 9	21	Ground	
10	Bit 10	22	+15V DC	
11	Bit 11	23	Gain Adjust	
12	Bit 12 (LSB)	24	Ref Out	

The three feedback resistors can be programmed for a total resistance of 967.7 Ω by connecting all three of them in parallel. The following pin connections will accomplish this:

17 to 21; 15 to 20; 18 to 19; output from pin 18

The required value of for the external resistance will be

$$R_E = 1071.4 - 967.7 = 103.7\ \Omega$$

For a ±1V range:

$$R_F + R_E = \frac{(4440)\ (1)}{(4440)\ (.001) - 1} = 1290.6\ \Omega$$

A value of $R_F = 1200\ \Omega$ can be obtained by connecting the 2KΩ and 3KΩ resistors in parallel with the following pin connections:

17 to 15; 15 to 18; 18 to 19; output from pin 20

The required value of R_E will be:

$$R_E = 1290.6 - 1200 = 90.6\ \Omega$$

2. External Op-Amp Using Internal Feedback Resistors. Figure 7 shows how to connect an external op-amp to the DDC DAC87-CBI-I when the internal feedback resistors are used. Pin connections for various voltage ranges are as follows:

Voltage Range	Connect Feedback to Pin	Offset Pin Conn.	Other Pin Connection	Feedback Resistance R_F
±2.5V	18	15	19 to 15	2.5KΩ
±5V	18	15	—	5KΩ
±10V	19	15	—	10 KΩ
0 to +5V	18	21	19 to 15	2.5 KΩ
0 to +10V	18	21	—	5 KΩ

3. External Op-Amp With External Feedback Resistor. For output voltage ranges greater than ±10V, an external feedback resistor must be used, as shown in Figure 8. External feeback resistors will generally give poorer gain accuracy over temperature. The internal resistors may be used in series with the external resistors to minimize this effect. When high voltage op-amps are used, diodes should be installed to protect the DDC DAC87 as indicated in Figure 8.

POWER SUPPLY DECOUPLING

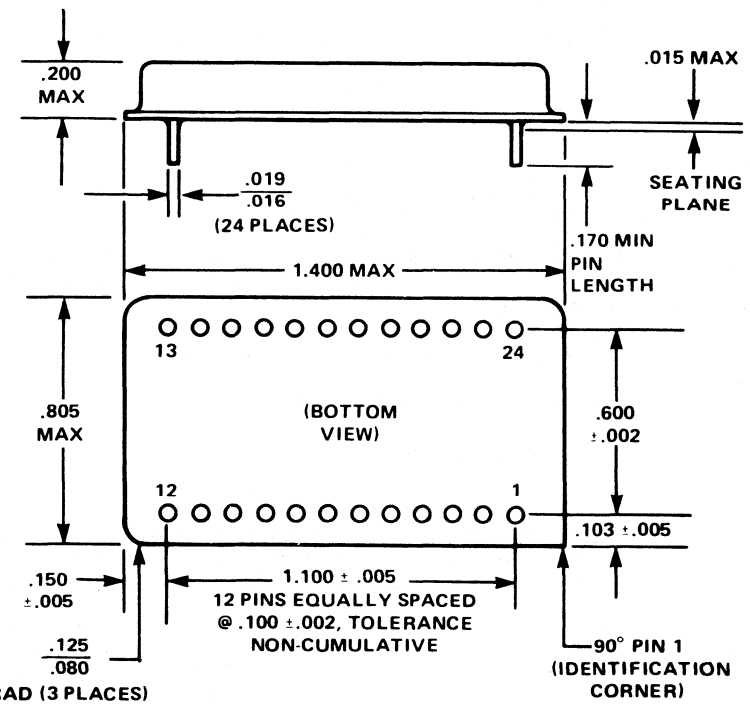
Power supply decoupling capacitors should be used to improve noise rejection. Install two capacitors at each of the three power supply input pins, as close to the module as possible. Tie the other ends of the capacitors to ground, preferably to a ground plane underneath the module. One capacitor at each pin should be a 1 — 10μ F tantalum or electrolytic type; the second capacitor can be 0.01μF ceramic for high frequency bypassing.

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request. The computed MTBF value for DDC DAC87, with MIL-STD-883 processing, (including burn in) is 3,400,000 hours, Ground Fixed, at 25°C.

MECHANICAL OUTLINE

24 Pin Double Dip



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

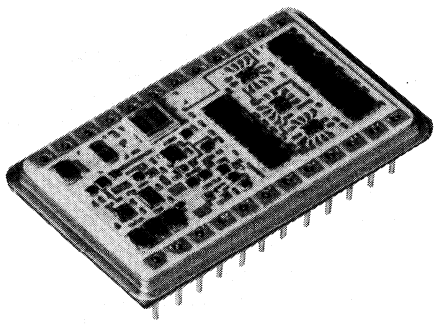
ORDERING INFORMATION

DDC DAC87 -CBI-V -883B

- MIL-STD-883 Processing: Optional
  - 883B = Conforms to MIL-STD-883 DDC procedures.
  - Blank = Same, except pre burn in test and burn in are omitted.
- Output Type:
  - V = Voltage output
  - I = Current output

ILC DATA DEVICE CORPORATION

13 BIT HYBRID D/A CONVERTER
Very Fast Settling Times: 50 ns Current Output, 500 ns Voltage Output



DESCRIPTION

The SDAC and 2615 are very high speed D/A converters with excellent temperature stability. They are designed to have low inherent offset and gain errors. The SDAC contains an output amplifier and can be pin-programmed for three bipolar voltage ranges. The 2615 does not have an output amplifier and provides current output. The SDAC has a separate analog ground for its voltage output so that full accuracy can be obtained even in the presence of common mode voltages. Both devices are calibrated with their own internal references, but may be used in a ratiometric mode with an external reference. They are packaged in a 24 pin DIP with a hermetically sealed metal case.

APPLICATIONS

Because of their small gain and offset errors and low temperature drift, the SDAC and 2615 offer outstanding performance for aircraft and shipboard displays, computer interfaces, sonar systems, and automated processing plants. For applications requiring both high speed and low glitch, the 2615 can be combined with a track-hold deglitcher such as the DGL-13 (see the DDAC data sheet). These converters are high reliability devices, with standard processing based on MIL-STD-883, except for burn-in which is an option. They are rugged devices which can be used in remotely located and hard to access equipment where small size and high MTBF are important.

FEATURES

- *SDAC HAS VOLTAGE OUTPUT: ±2.5V, ±5V, and ±10V*
- *2615 HAS CURRENT OUTPUT: ±2.5 mA*
- *CODING: Complementary Offset Binary*
- *REMOTE GROUND SENSE*

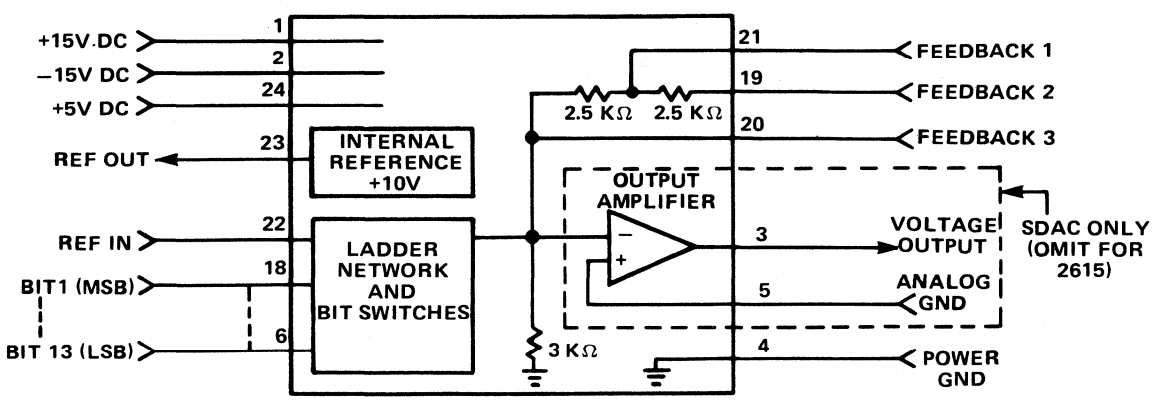


FIGURE 1. SDAC AND 2615 BLOCK DIAGRAM

SDAC AND 2615 SPECIFICATIONS

Typical values at 25°C and at nominal power supply voltages unless indicated otherwise.

PARAMETER	UNITS	SDAC-10 2615-10	SDAC-11 2615-11	SDAC-12 2615-12
RESOLUTION	Bits	13	13	13
ACCURACY (USING INTERNAL REF)				
Linearity Error	% F.S. Range	±0.05 max	±0.025 max	±0.0125 max
Linearity Tempco	ppm/°C	4	2	1
Gain Error	% F.S. Range	±0.1 max	±0.05 max	±0.025 max
Gain Tempco				
V Output	ppm/°C	±15	±15	±15
I Output	ppm/°C	±25	±25	±25
Current Offset, 2615				
Current Offset	μA	2.0 max	1.0 max	0.5 max
Current Offset Tempco	μA/°C	0.04	0.02	0.01
Voltage Offset, SDAC				
Offset, ±10V Scale	mV	10.0 max	5.0 max	2.5 max
Voltage Offset Tempco	μV/°C	200	100	50
Differential Linearity Error	% F.S. Range	±0.1 max	±0.05 max	±0.025 max
Monotonic to	Bits	10	11	12
DYNAMIC CHARACTERISTICS				
Settling Time to Specified Accuracy (for F.S. Input Change)				
Current Output	nsec	50 typ for $R_L \leq 100\Omega$ 100 max for $R_L \leq 330\Omega$		
Voltage Output				
±2.5V Scale	nsec	500 max		
±5V Scale	nsec	1000 max		
±10V Scale	nsec	1600 max		
Output Capacitance for				
Current Output	pF	20 typ		
Slew Rate	V/μs	60 typ; 40 min		
OUTPUT				
Current Output				
Current Range	mA	±2		
Output Impedance	KΩ	3		
Compliance	V	−3 to +6 min		
Voltage Output				
Voltage Ranges	V	±2.5, ±5, or ±10; pin programmable		
Max Current	mA	5 min		
D.C. Impedance	Ω	0.1		
Short Circuit Protection	sec	5 max at 25°C 2 max over temperature range		
DIGITAL INPUTS				
Logic Type		13 bits, TTL compatible Parallel positive logic		
Coding		Complementary offset binary		
Loading		1 standard TTL load		
REFERENCE				
Internal Reference				
Voltage	V	+10 ± 10%		
Current Output	mA	±3 max		
External Reference (Optional)				
Voltage	V	0 to +10		
Input Impedance	KΩ	4.44		
POWER SUPPLIES				
Voltage	V	+15	−15	+5
Regulation for Full Accuracy	%	±2	±2	±5
Max Voltage Without Damage	V	+18	−18	+18
Current (Without External Load)				
SDAC	mA	25 typ 30 max	30 typ 35 max	20 typ 25 max
2615	mA	21 typ 26 max	26 typ 31 max	20 typ 25 max
TEMPERATURE RANGES				
Operating (Case Temperature)				
−3 Option	°C	0 to +70		
−1 Option	°C	−55 to +105		
Storage	°C	−55 to +125		
PHYSICAL				
Size (24 Pin Double DIP)	inch	0.8 x 1.4 x 0.2 (2 x 3.6 x 0.5 cm)		
Weight	oz	0.38 typ (10.8 g)		

TECHNICAL INFORMATION

INTRODUCTION

Figure 1 is a block diagram for both the SDAC and the 2615. On the 2615 there is no connection to pins 3 and 5, and the current output connection is pin 20. These converters generate output voltages (SDAC) or currents (2615) which are digitally controlled, discrete fractions of the reference voltage. The gain and offset are factory trimmed to very tight tolerances so that external trimming is not required. The output is bipolar with complementary offset binary coding.

The converter can be damaged by shorting the voltage output. Pin 3 may be grounded to analog or power ground for 5 sec only at +25°C, and 2 sec only at +85°C case temperature.

SDAC OUTPUT CONNECTIONS

Output connections for all three output voltage ranges of the SDAC are shown in Figure 2. The feedback connection should be made as close to the load as possible to minimize the effects of line and contact impedance. Output drive capability is ±5 mA for all three voltage ranges.

The common mode capability of the SDAC analog ground requires that the resistors R1 and R2 have the values shown. The remote ground at the load must also be within ±1.0V (DC + AC peak voltage) of the analog ground. The common mode noise suppression capability will then be a function of the accuracy of the R1/R2 resistance ratio as shown in the following table. The absolute values of R1 and R2 are not critical. Low power metal film resistors are recommended.

CMRR AS A FUNCTION
R1/R2 RATIO ACCURACY

ACCURACY OF R1/R2 RATIO	MINIMUM CMRR WILL BE
0.1%	60 dB
1.0%	40 dB
10%	20 dB

2615 OUTPUT CONNECTIONS

The current output of the 2615 is taken directly from pin 20. The feedback pins 19 and 21 may be left floating or may be used as feedback for an external amplifier. The load ground should be connected directly to the power ground.

REFERENCE

The SDAC has an internal reference supply and is factory calibrated with this supply. Full specified performance can be obtained with REF IN and REF OUT (pins 22 and 23) connected together.

External references of 0 to +10V can be accommodated with ratiometric accuracy reduced to ±.2% typ for 10V references and 1 LSB additional error for +5V or lower references. Negative references cannot be accommodated. The reference input impedance is 4.44 KΩ.

POWER SUPPLIES

The SDAC has 0.01μf ceramic decoupling capacitors at the ±15V and +5V power supply inputs. The +5V input has an internal regulator and therefore can accept a voltage range of +5 to +15V without damage. It could, therefore, be run from the +15V power supply thus saving the cost of the +5V supply, but increasing internal power dissipation from 1.10 to 1.25 watts max. Accuracy in this configuration is reduced by .005%/volt for variations on pin 24 (+5V input).

CODING

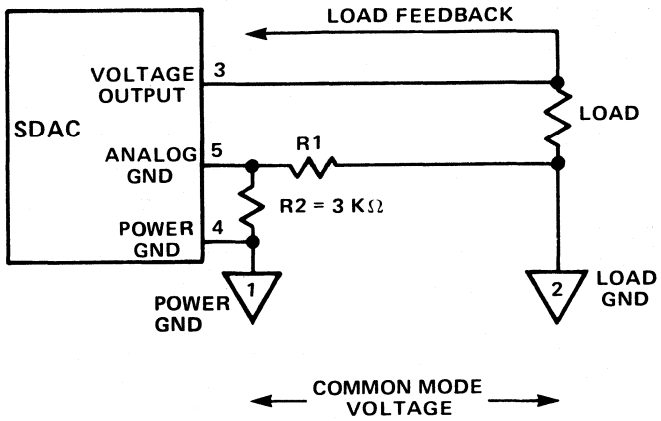
Offset binary coding for the SDAC and 2615 is shown by the bit weight table in Figure 3. The values for full scale voltage (F.S.) and 1 LSB are as follows:

RANGE	FULL SCALE	1 LSB
±2.5V	2.50000V	0.00062V
±5V	5.00000V	0.00122V
±10V	10.00000V	0.00244V
±2 mA	2.00000 mA	0.000488 mA

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All SDAC hybrids are build in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5004/5008 except for burn in, which is optional. To specify preburn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in), Ground Fixed, at 25°C, is 3,100,000 hours for the SDAC and 3,700,000 hours for the 2615.



FEEDBACK CONNECTION AND R1

VOLTAGE RANGE	CONNECT LOAD FBK TO PIN	OTHER PIN CONNECTIONS	R1
±2.5V	21	19 – 20	1.25 KΩ
±5V	21	–	2.5 KΩ
±10V	19	–	5.0 KΩ

FIGURE 2. OUTPUT CONNECTIONS FOR SDAC

COMPLEMENTARY OFFSET BINARY

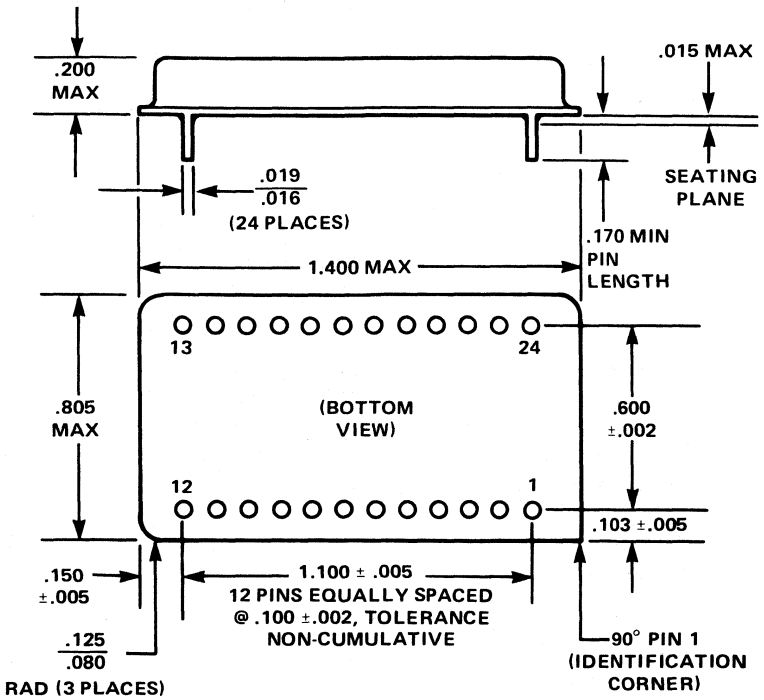
OUTPUT	DIGITAL BIT INPUTS												
	MSB 1	2	3	4	5	6	7	8	9	10	11	12	LSB 13
+ F.S. – 1 LSB	0	0	0	0	0	0	0	0	0	0	0	0	0
+ 1/2 F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1
+ 1 LSB	0	1	1	1	1	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1
–1 LSB	1	0	0	0	0	0	0	0	0	0	0	0	0
–1/2 F.S.	1	0	1	1	1	1	1	1	1	1	1	1	1
–F.S. + 1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	0
–F.S.	1	1	1	1	1	1	1	1	1	1	1	1	1

FIGURE 3. BIT WEIGHT TABLE

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	+15 VDC Input	13	Bit 6
2	–15 VDC Input	14	Bit 5
3	Output (N.C. 2615)	15	Bit 4
4	GND (Tied to Case)	16	Bit 3
5	Ana GND (N.C. 2615)	17	Bit 2
6	Bit 13 (LSB)	18	Bit 1 (MSB)
7	Bit 12	19	Feedback 2
8	Bit 11	20	Feedback 3
9	Bit 10	21	Feedback 1
10	Bit 9	22	Ref. In
11	Bit 8	23	Ref. Out
12	Bit 7	24	+5 VDC Input

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions are shown in inches.
2. Load identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

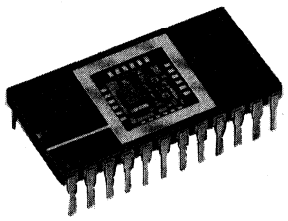
ORDERING INFORMATION

SDAC – 12 – 1 – 883B

- MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883 DDC processing.
  - Blank = Same, except pre burn in test and burn in are omitted.
- Operating Temperature Range (Case):
  - –1 = –55°C to +105°C
  - –3 = 0°C to +70°C
- Linearity Error:
  - 12 = 0.0125% F.S. Range
  - 11 = 0.025% F.S. Range
  - 10 = 0.05% F.S. Range
- Model:
  - SDAC = Voltage output
  - 2615 = Current output

ILC DATA DEVICE CORPORATION

12 BIT MULTIPLYING D/A CONVERTER
Double Buffered; Voltage Output



DESCRIPTION

The DAC-02701 is a double buffered 4 quadrant multiplying DAC with a 10 volt full scale output. It has two-stage transparent input latches for direct microprocessor compatibility, and features 12 bit parallel data transfer. Packaged in a small hermetically sealed 24 pin DDIP, the DAC-02701 offers 12 bit monotonicity over its full −55°C to +125°C operating temperature range. Input registers and multiplying DAC are implemented with low power CMOS technology, offering compatibility with both CMOS and TTL logic families. Data transfer from a 16 bit data bus can be accomplished with one byte. MIL-STD-883B screening is available.

APPLICATIONS

With its small hermetic package, wide operating temperature range, and versatile performance, the DAC-02701 is ideal for the most demanding military and industrial requirements. Typical applications include equipment for computer interface and control, function generation and signal conditioning.

The DAC-02701 two-stage input latches are especially useful in applications that require simultaneous update of multiple DAC channels from a single data bus. These applications include X-Y and sine-cosine coordinate generation.

FEATURES

- *μP COMPATIBLE: DOUBLE BUFFERED INPUT LATCHES*
- *±10 V FULL SCALE VOLTAGE OUTPUT*
- *12 BIT MONOTONIC OVER −55°C TO +125°C TEMPERATURE RANGE*
- *12 BIT PARALLEL DATA TRANSFER*
- *4 QUADRANT MULTIPLICATION*
- *SMALL HERMETIC 24 DDIP PACKAGE*

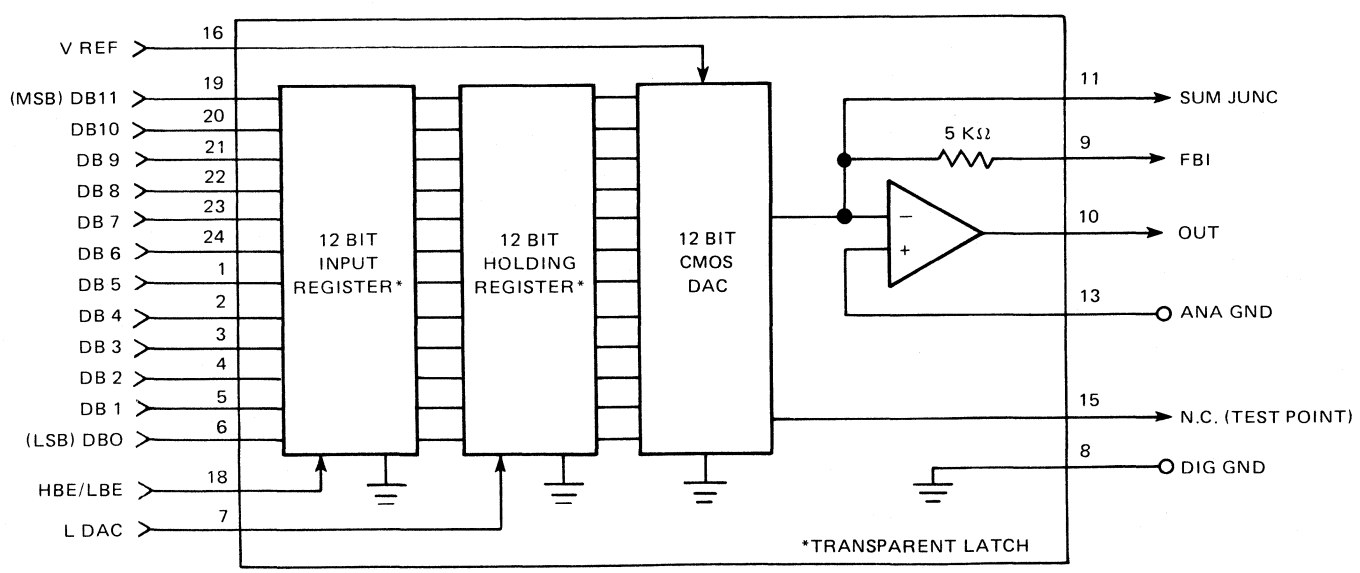


FIGURE 1. DAC-02701 BLOCK DIAGRAM

SPECIFICATIONS – Typical values @ +25°C, V_{REF} = +10V, and ±15 volt power supply voltages unless otherwise noted:

PARAMETER	UNITS	VALUE	
		11 Bit Mono	12 Bit Mono
RESOLUTION	bits	12	12
ACCURACY			
Linearity Error			
Full temp range	%F.S.R.	±0.1 max	±0.05 max
Offset Error			
Full temp range	mV	±10 max	±3 max
Gain Error			
Full temp range	%F.S.R.	±0.2 max	±0.2 max
Monotonicity			
Full temp range	bits	11	12
DYNAMIC CHARACTERISTICS			
Settling Time (1)	μsec	25 max	
Reference Feedthrough (2)	mV p-p	1	
DIGITAL INPUTS			
Logic Compatibility		CMOS and TTL	
Voltage Input			
Logic "1"	V	+2.4 to $+V_{DD}$	
Logic "0"	V	−0.3 to +0.8	
Current Load			
Logic "1"	μA	1 max	
Logic "0"	μA	1 max	
Strobe Pulse Width (3)	nsec	250 min	
Data Setup Time	nsec	250 min	
Data Hold Time	nsec	0 min	
Coding		Complementary Offset Binary	
REFERENCE			
Input Voltage	V	±10	
Input Impedance	KΩ	2.5 min	
ANALOG OUTPUT			
Voltage	V	±10	
Current	mA	±4 max	
Impedance	Ω	0.1 max	
POWER SUPPLIES			
V_{DD}			
Nominal	V	+15 ±0.45	
Current Drain	mA	10 max	
Range	V	+5 to +16 max	
Rejection Ratio	%/%	0.005 max	
V_{EE}			
Nominal	V	-15 ±0.45	
Current Drain	mA	10 max	
Range	V	Same as V_{DD}	
Rejection Ratio	%/%	0.005 max	
TEMPERATURE RANGE			
Operating			
−1 Option	°C	−55 to +125	
−2 Option	°C	−25 to + 85	
Storage	°C	−65 to +150	
PHYSICAL CHARACTERISTICS			
Package		24 pin DDIP	
Size	in	1.22 x 0.6 x 0.15 (31.0 x 15.3 x 3.8 mm)	
Weight	oz	0.09 (2.5g)	

NOTES:
(1) Output settling time to within 0.01% of final value for a 10 volt digital input change
(2) V_{REF} = 20 V p-p at 10 KHz
(3) LDAC and HBE/LBE strobes are level triggered

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a block diagram of the DAC-02701. Functional elements of the unit include a 12 bit input register, a 12 bit holding register, a 12 bit CMOS multiplying DAC, and a current to voltage converter op amp.

Both sets of registers are level triggered and function as transparent latches. This allows the DAC-02701 to be configured for double buffered, single buffered, or direct flow through operation, by proper use of the 2 strobe signals. The input registers are implemented with low power CMOS technology, and are compatible with both CMOS and TTL logic families.

Four (4) quadrant multiplication is accomplished by the 12 bit CMOS DAC. It provides a current output which is the product of its reference input voltage and the digital input stored in the holding register. The external reference may be AC or DC, unipolar or bipolar. Output coding is Complementary Offset Binary. The output op amp is used to convert the DAC current to a voltage.It offers a low impedance source of the 10 volt full scale output. Separate analog and digital grounds are provided to allow flexible use of noise reduction techniques. The analog and digital ground pins must be tied together at one point in the system, preferably close to the DAC-02701.

FOUR QUADRANT MULTIPLICATION

The DAC-02701 output voltage is the product of the applied external reference voltage and the 12 bit digital input word. Four quadrant multiplication refers to the fact that the reference voltage may be either positive or negative, and the digital input word may be either positive or negative. Furthermore, the external reference may be either DC or AC. The DAC-02701 output is therefore the product of both the magnitude and polarity of the two inputs.

INPUT CODING

The DAC-02701 input coding is Complementary Offset Binary. Figure 2 shows various digital input codes and the analog output resulting from each one. It is to be noted that most significant bit (MSB) functions as a polarity control. When the MSB is a logic "0", the output is the same polarity as the external reference. When the MSB is a logic "1", the output is the opposite polarity from the external reference. The eleven LSBs therefore function as a digitally controlled attenuator.

MICROPROCESSOR INTERFACING

Two-stage 12 bit input registers, each independently strobed, make the DAC-02701 easy to interface to a 12 bit or 16 bit microprocessor data bus. Figure 3 illustrates the most general microprocessor interface. The DAC-02701 is mapped into two memory locations; one each for the input register and holding register. Address decoding provides HBE/LBE select for the input register, and LDAC select for the holding register. The microprocessor WRITE signal is then used to generate the HBE/LBE strobe or LDAC strobe, which transfer the data into the appropriate register.

The microprocessor interface shown in Figure 3 is most often used in applications that require simultaneous update of multiple DAC channels from a single data bus. Data is sequentially transferred from the bus to each DAC input register. Then all DACs are updated in parallel by strobing their holding registers simultaneously.

For data bus interfaces with random update requirements, the configuration of Figure 3 may be simplified. These applications require only single buffering of the 12 bit input data. The DAC-02701 holding register can therefore be placed in its transparent mode by permanently tying the LDAC strobe line to a logic "1" level. The DAC-02701 can also be operated with both input register stages in the transparent mode. When HBE/LBE and LDAC strobes are both tied to logic "1", input data will flow through directly to the DAC. The DAC output will then respond directly to input data changes.

TIMING DIAGRAM

Figure 4 is a DAC-02701 timing diagram. It illustrates data and strobe signal timing relationships. The HBE/LBE strobe pulse width must be 250 nanoseconds minimum. Data set-up time, prior to the falling edge of HBE/LBE, is 250 nanoseconds minimum. The LDAC strobe pulse width must be 250 nanoseconds minimum. In order to ensure isolation of the holding register from the data bus, the rising edge of LDAC must follow the falling edge of HBE/LBE by zero (0) nanoseconds minimum.

OFFSET AND GAIN TRIMS

Some applications may require a lower gain error and/or DC offset error than the DAC-02701 exhibits after factory adjustment. Figure 5 illustrates the connections required to trim gain and DC offset errors to zero. Multi-turn trimpots, with temperature coefficients less than 100 ppm/°C are recommended for best results. Metal film fixed resistors, with temperature coefficients less than 100 ppm/°C, are also recommended.

POWER SUPPLIES AND DECOUPLING

Recommended power supply voltages for the DAC-02701 are ±15 volts. It will operate satisfactorily, though, over the range ±5 volts to ±16 volts. If power supplies lower than 15 volts are used, the allowable reference and output voltage swings are less than the specified ±10 volts. This is due to limitations in the output op amp. As an example, if ±5 volt power supplies are used, the reference and output swings will be restricted to typically ±3 volts.

Capacitive decoupling of all power supplies is recommended to minimize noise. Tantalum or electrolytic capacitors of 1 μf or greater will filter out low frequency noise. Ceramic capacitors of 0.01 μf will filter out high frequency noise. For best results, all capacitors should be placed as close as possible to the DAC.

GROUNDING AND LAYOUT PRECAUTIONS

The DAC-02701 provides separate analog and digital grounds to allow flexible use of noise reduction techniques. The ANA GND and DIG GND pins must be tied together at one point in the system, preferably very close to the DAC-02701. The objective of the grounding scheme should be to minimize the AC and DC digital current flow in the return path of the analog signals.

DIGITAL INPUT	ANALOG OUTPUT
0000 0000 0000	$+V_{REF}$
0010 0000 0000	$+V_{REF}$ (3/4)
0100 0000 0000	$+V_{REF}$ (1/2)
0111 1111 1111	$+V_{REF}$ (1/2048)
1000 0000 0000	0
1000 0000 0001	$-V_{REF}$ (1/2048)
1100 0000 0000	$-V_{REF}$ (1/2)
1110 0000 0000	$-V_{REF}$ (3/4)
1111 1111 1111	$-V_{REF}$ (2047/2048)

FIGURE 2. INPUT CODING

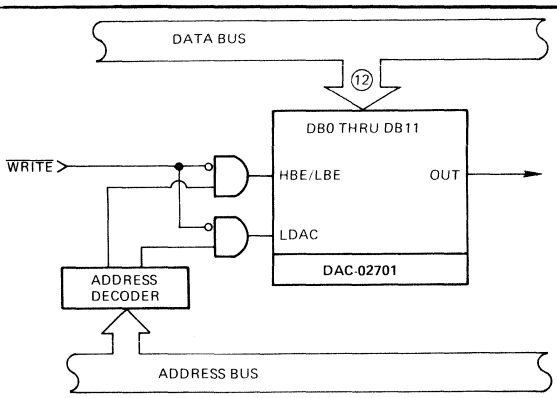


FIGURE 3. MICROPROCESSOR INTERFACE

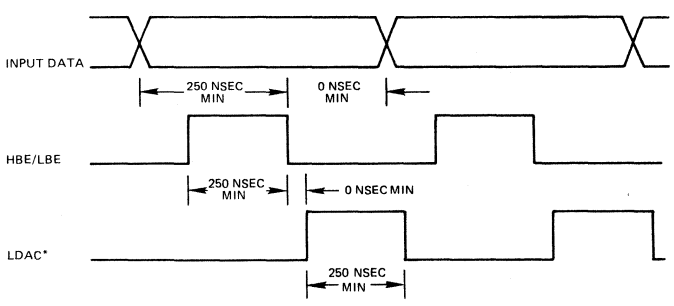


FIGURE 4. TIMING DIAGRAM

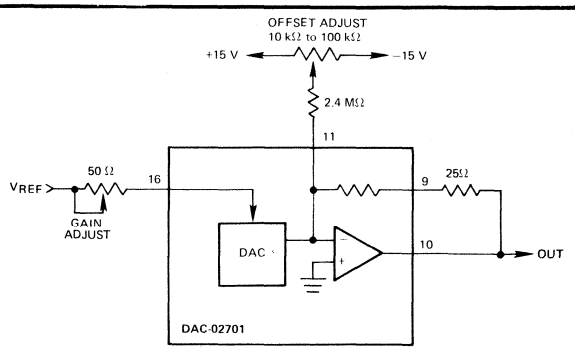


FIGURE 5. OFFSET AND GAIN TRIMS

A grounding configuration which works well is to tie together the ANA GND and DIG GND pins at the DAC-02701 package. A single connection is then made between the analog ground of the DAC-02701 and the analog ground of the load. System power ground should be connected close to the load.

In general, ground noise is minimized by using wide ground conductor paths, which exhibit a lower impedance. To minimize crosstalk and inductive affects, digital input lines and analog output lines should be separated from each other, and made as short as possible.

Unused digital inputs must be connected to either ground or V_{DD}. When digital inputs are routed directly to another printed circuit board, it is recommended that a high value (1Mohm) resistor be connected between each input and ground. This will prevent static charge buildup and resulting damage when the PC board is removed from the circuit.

REALIABILITY

The DAC-02701 is manufactured in accordance with the requirements of MIL-STD-883B. Screening is based upon the requirements of Method 5008, except for burn-in which is optional.

Low power CMOS integrated circuits, and a minimum chip count have resulted in a very low calculated failure rate ~~of~~ the DAC-02701. The predicted MTBF is 6,000,000 hours. in accordance with MIL-HDBK-217C at +25°C in ground fixed applications.

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	DB5	13	ANA GND
2	DB4	14	N.C.
3	DB3	15	N.C. (TEST POINT)
4	DB2	16	V_{REF}
5	DB1	17	+15 V (V_{DD})
6	DB0 (LSB)	18	HBE/LBE
7	LDAC	19	DB11 (MSB)
8	DIG GND	20	DB10
9	FB1	21	DB9
10	OUT	22	DB8
11	SUM JUNC	23	DB7
12	–15 V (V_{EE})	24	DB6

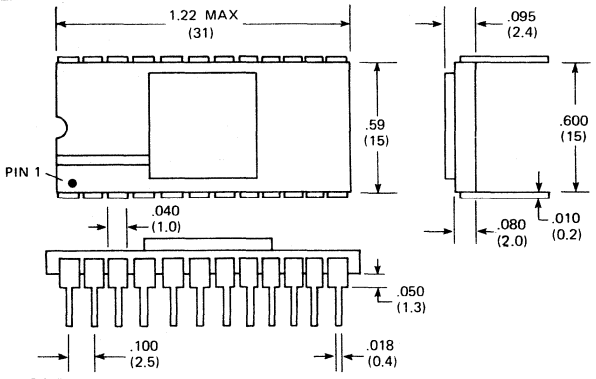
ORDERING INFORMATION

DAC-02701 –1 0 3

- Monotonicity Grade:
  - 3 = 12 bit over temp range
  - 2 = 11 bit over temp range
- Reliability Grade:
  - 1 = Conforms to MIL-STD-883
  - 0 = Same except preburn in test and burn in are omitted
- Operating Temperature Range:
  - 1 = –55°C to +125°C
  - 2 = –25°C to +85°C

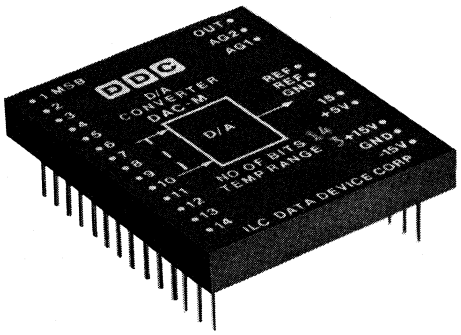
MECHANICAL OUTLINE

24 PIN DDIP



NOTES:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

15 BIT MULTIPLYING D/A CONVERTER
Very Low Feedthrough Capacitance; Remote Grounds



FEATURES

- *VERY HIGH RESOLUTION, COMPLETELY SELF-CONTAINED 4 QUADRANT MULTIPLYING D/A CONVERTER*
- *HAS MANY FEATURES TO SIMPLIFY USE:*
  - *Totally trimmed*
  - *Differential input*
  - *High output CMRR*
  - *Pin selectable one's complement or two's complement coding*
  - *Power supplies are internally decoupled*
- *TOTAL ACCURACY AS LOW AS ±0.0031% F.S. RANGE*
- *DIGITAL SETTLING TIME TO ±2mV IS 5μs MAX*
- *SMALL SIGNAL BANDWIDTH IS 1.0 MHz TYP*

DESCRIPTION

The DAC-M is a high resolution multiplying D/A converter with very low feedthrough capacitance and wide bandwidth. It has many features that simplify its use. The power, reference input, and output grounds are all separated to minimize the effects of system ground noise and to allow for different input and output common mode signals. One's complement or two's complement coding is pin selectable and the 15 bit input is TTL compatible.

APPLICATIONS

The DAC-M is used in x–y displays and plotters, character and stroke generators, graphic display systems, programmed pulse generators, meter drive circuits, and electronic linotype systems. The modules are totally encapsulated, rugged and able to withstand severe environmental requirements such as the specifications for shock, vibration, and temperature in MIL-STD-202E. They are suitable for both military and demanding industrial environments.

SPECIFICATIONS
At 25° ambient temperature and rated supplies unless indicated otherwise.

PARAMETER	UNITS	VALUE DAC-M-11	DAC-M-12	DAC-M-13	DAC-M-14
RESOLUTION (Including Sign)	Bits	15	15	15	15
ACCURACY					
Total Accuracy (Max, Includes Linearity, Offset, and Gain Errors)					
DC to 400 Hz	Bits	11	12	13	14
	% F.S. Range	±0.0244	±0.0122	±0.0061	±0.0031
Above 400 Hz		Increases linearly up to 0.1% typ at 10 kHz			
Total Accuracy Tempco (Max)	% F.S.R./°C	±0.002	±0.001	±0.0005	±0.0005
Linearity Tempco (Typ)	% F.S.R./°C	±0.0001	±0.0001	±0.0001	±0.0001
Gain Tempco (Typ)	% F.S.R./°C	±0.0010	±0.0005	±0.0003	±0.0002
Offset Tempco (Typ)	μV/°C	25	25	25	25
DYNAMIC CHARACTERISTICS					
Analog Dynamics, Ref to Output					
Settling Time to ±2 mV of Final Value	μs	10 max for a ±20V step			
Slew Rate	V/μs	10 typ; 5 min			
Small Signal Bandwidth (f_t)	MHz	1 typ; 0.2 min			
Frequency for Full Output (FFO)	kHz	40 min			
Steady State Ramp Delay	μs	0 typ; ±0.2 max			
Phase Shift, Ref to Output	degrees	±0.3 max at 400 Hz			
Feedthrough Capacitance	pF	5 typ; 15 max for RC high pass circuit with R assumed to be 2 KΩ			
Digital Dynamics					
Settling Time to ±2 mV of Final Value	μs	5 max for F.S. digital change			
Slew Rate	V/μs	10 typ; 5 min			
REFERENCE INPUT					
Ref Signal Voltage Range	V	±10 max			
Input Range, Ref Signal + Ref Common Mode	V	±16 with respect to power GND			
Absolute Max Without Damage	V	±20 with respect to power GND			
Input Impedance					
Single Ended	KΩ	40 ± 1%			
Differential	KΩ	80 ± 1%			
Frequency Range					
For Full Accuracy	Hz	0 to 400			
Total Range	Hz	0 to 10,000			
CMRR, Ref to Output	dB	80 typ, 70 min			

PARAMETER	UNITS	VALUE		
DIGITAL INPUT				
Logic Type		TTL compatible		
		15 parallel bits, positive true		
Coding (Pin Selectable)		One's complement or two's complement		
Loading, Each Bit		1 normal TTL load		
OUTPUT				
Output Signal Voltage Range	V	±10		
Output Range, Signal + Output Common Mode	V	±11 max with respect to power ground		
Max Output Common Mode Without Damage	V	±10		
Current	mA	±10 min		
DC Impedance	Ω	0.1 max		
Output CMRR	dB	70 min, ratio of output signal to output common mode		
Noise (DC to 10 kHz)	mV rms	1 max		
Short Circuit Protection		Fully protected		
POWER REQUIREMENTS				
Voltages	V	+15 ± 1%	−15 ± 1%	+5 ± 2%
Max Voltage Without Damage	V	+18	−18	+7
Current	mA	80 max	80 max	80 max
Output Rejection Ratio for Linear Output Range	dB	80 typ	80 typ	80 typ
TEMPERATURE RANGES				
Operating, Case Temperature				
−1 Option	°C	−55 to +85		
−3 Option	°C	0 to +70		
Storage	°C	−55 to +125		
PHYSICAL CHARACTERISTICS				
Size	inch	3.125 x 2.625 x 0.42 (7.94 x 6.67 x 1.07 cm)		
Weight	oz	2.9 typ (82.3 g)		

SECTION C

S/H AND T/H AMPLIFIERS

C. SAMPLE/HOLD AND TRACK/HOLD AMPLIFIERS

SUMMARY TABLE

Name	Form Factor	Acquistion Time (F.S. Change)	Linearity Error (max)	Aperture Uncertainty (Jitter)	Small Signal Bandwidth	Features	Page
TH-8530 T/H	24 pin DDIP hybrid	10 ns typ	±0.2% F.S.R.	35 ps max	100 MHz typ	100 MHz T/H amplifier exceeds speed of any S/H. Drive capability for capacitive loads.	105
SH-8518 S/H	24 pin DDIP hybrid	30 ns typ	±0.1% F.S.R.	35 ps max	100 MHz typ	Ultra-fast.	108
ADH-050 and ADH-051 T/H	24 pin DDIP hybrid	100 ns typ 500 ns typ	±0.0125% F.S.R. ±0.0125 ps max	500 ps max 1000 ps max	15 MHz typ 3.5 MHz typ	Very fast. 12 bit linearity.	111
DGL-13 T/H Deglitcher	24 pin DDIP hybrid	1800 ns max Programmed by feedback resistor.	±0.01% F.S.R.	1.0 ns typ	12 MHz typ	Designed for deglitching. Preprogrammed hold time initiated by external strobe.	114
THA05203	24 pin DDIP hybrid	150 ns typ	±0.01% F.S.R.	100 ps max	16 MHz typ*	High speed, high accuracy. HTC-0300A and TP4860 pin compatible	118

*3dB small signal

BACKGROUND INFORMATION

INTRODUCTION

Sample/hold and track/hold amplifiers are used when the voltage level of a signal must be held or stored for a short period of time. A signal which varies rapidly may have to be held constant to allow time for an analog to digital or synchro to digital conversion to take place, or it may have to be stored while multiplexed signal channels are converted sequentially.

DDC's sample/hold and track/hold amplifiers are distinguished for their speed and low jitter. The new TH-8530 track/hold is in fact faster than any other track/hold or even sample/hold amplifier currently available. The DGL-13 track/hold falls into a different category. Designed for deglitching D/A converters, it has exceptionally low glitch and a preprogrammed hold time initated by an external strobe.

The main components of a S/H or T/H amplifier are shown in the simplified diagram of Figure 1. When the switch is closed the output signal follows the analog input, and when the switch is opened the output voltage is ideally fixed at the level of the input because it is stored on the holding capacitor. The difference between a S/H and T/H amplifier is that a sample/hold can only sample the input signal briefly, whereas a track/hold can track the input continuously. In a S/H the gate is AC coupled to the switch, and the switch can remain closed for only a brief time. In a T/H the gate is DC coupled to the switch, and the switch remains closed as long as the gate signal stays in the track mode.

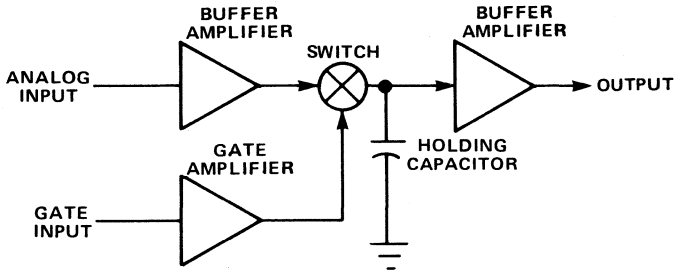


FIGURE 1. SIMPLIFIED DIAGRAM OF TRACK/HOLD OR SAMPLE/HOLD AMPLIFIER

The relationships between the output, input, and gate signals of a S/H or T/H amplifier are complex. In these devices there are delays between the gate signal changes and the opening or closing of the switch. Time is required for the output to settle, the output can have offsets and input signals can feed through to the output even when the switch is open. These effects are illustrated in Figure 2, and are discussed in the following sections.

TERMINOLOGY AND SIGNAL RELATIONSHIPS

The definitions which follow describe the key terms used to characterize S/H and T/H amplifiers. The terminology is depicted graphically in Figure 2.

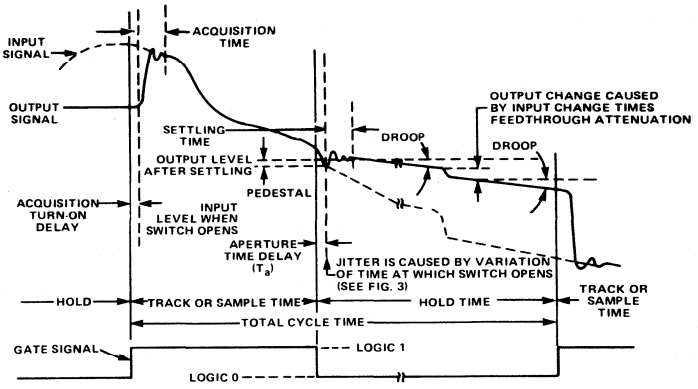


FIGURE 2. RELATIONSHIP OF OUTPUT, INPUT, AND GATE SIGNALS
(Assuming Gate Logic 0 = Hold)

A logic gate signal initiates the track or sample period. After this signal has been applied, the holding capacitor requires an interval of time called the Acquisition Time to charge to the point where it can track the input signal. The acquisition time depends on the magnitude of the voltage change required. It includes the Acquisition Turn-On Delay which is the time interval between application of the logic signal and the switch closure, plus in some cases output buffer activation time. The minimum track or sample period must be at least as long as the Acquisition Time.

When a signal is applied to the gate to initiate the hold period, there is a short delay, the Aperture Time Delay (T_a), before the switch opens to isolate the holding capacitor from the analog input. The delay itself can be compensated for, but the Aperture Time Delay Uncertainty (Jitter) associated with the delay can lead to errors, as shown in Figure 3.

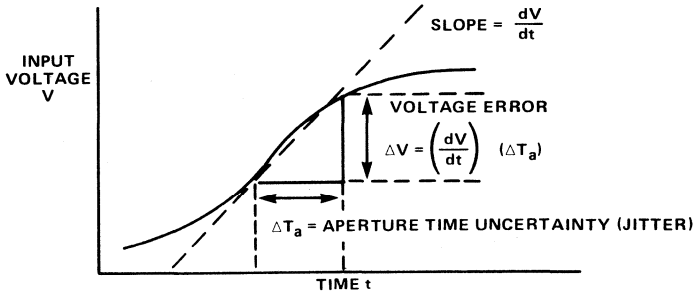


FIGURE 3. APERTURE TIME UNCERTAINTY ERROR (JITTER)

The time needed for the S/H amplifier output to settle out to the holding capacitor voltage after the gate changes from the sample mode to the hold made is the Settling Time, which includes the aperture time delay. Settling time is defined as the time required for an amplifier to settle to its final value ± a specified error band. If the output voltage is used at a shorter time interval after switching to the hold mode, errors will be introduced.

After the switch is opened and the output has settled, the output voltage generally increases or decreases linearly with time. This Droop is caused mainly by the bias current of the output buffer amplifier and by leakage through the switch. The bias current and leakage can be positive or negative. Droop can also be caused by leakage from the holding capacitor. The droop rate will determine how long a hold time can be tolerated to maintain the required accuracy.

When the switch opens after the sample period, any unbalanced charge in the switch is transferred to the holding capacitor, creating a small positive or negative step error, the Pedestal, in the output voltage during the hold period. The SH-8518 has the provision for fine trimming the pedestal error.

There will be a DC Offset or difference in DC voltage level between the input and output voltages of the S/H or T/H because of offset errors in the input and output amplifiers. Such a DC offset is present during both the track and the hold modes.

While the switch is open and the signal is being held, a step change in the input signal will still feed through the open switch capacitance to the output. The small output signal change which results is equal to the input voltage divided by the Feedthrough Attenuation of the open switch circuit.

SAMPLING RATE LIMITATIONS

The sampling rate is the rate at which an entire sample and hold cycle is completed.

$$\text{Sampling rate} = \frac{1}{\text{total cycle time}} = \frac{1}{\text{track (or sample) time + hold time}}$$

The maximum sampling rate is therefore determined by the minimum sample time plus minimum hold time. The minimum sample time is the acquisition time, while the minimum hold time will include the settling time plus whatever additional time is required for information processing.

A sample/hold amplifier has a minimum sampling rate as well as a maximum one. The minimum rate is determined by the maximum sample time plus the maximum hold time. The sample time has a maximum value (which should be specified) because the gate is AC coupled.

The hold time may also have a maximum value, because of droop. The output error will exceed the specified accuracy if the hold time is greater than the maximum error divided by the droop rate.

Droop may eventually cause the output voltage to exceed the limits of the specified output voltage range. The time to acquire a new signal may then exceed the specified acquisition time because of saturation effects.

ERROR CAUSED BY APERTURE TIME UNCERTAINTY

The uncertainty in the moment of time at which the signal is acquired and held (the aperture time jitter) causes an error whose magnitude depends on the rate at which the input is changing (Figure 3). The following discussion relates the maximum percent error in the output V caused by this effect with the aperture time uncertainty ΔT_a and the analog signal frequency f.

The error ΔV in the voltage is:

$$\Delta V = \left(\frac{dV}{dt}\right) \Delta T_a$$

For a sinusoidal signal, $V = V_o \sin (2\pi ft)$

$$\Delta V = 2\pi f V_o \cos (2\pi ft)\, \Delta T_a$$

Since the maximum value of the cosine function is 1, the maximum percent error is:

$$\text{maximum \% error} = 100\left(\frac{\Delta V}{V_o}\right) = 200\pi (f)(\Delta T_a) = 628\ (f)\ (\Delta T_a)$$

As an example, if the aperture time uncertainty is 500ps, then at a frequency of 0.5 MHz:

$$\text{maximum \% error} = (628)\ (0.5 \times 10^6)\ (500 \times 10^{-12}) = .16\%$$

This % error is the percentage of the maximum input signal amplitude, not the percentage of allowable full scale. Note also that if the input rate dV/dt is constrained only by slew rate limiting, then the maximum % error should be calculated directly as

$$\text{maximum \% error} = \frac{100}{V_o}\left(\frac{dV}{dt}\right)_{\text{max slew}} \Delta T_a$$

The error caused by aperture time uncertainty may be obtained from the nomograph in Figure 4 if the input signal is sinusoidal and the output is not slew rate limited. Any sloping straight line drawn on the nomograph from top to bottom relates the corresponding aperture uncertainty, percent error, and input frequency. As an example, suppose the maximum allowed error caused by aperture time is specified to be 0.1%, and the aperture time is 500 ps. A straight line drawn through these values on the nomograph intersects the frequency scale at about 300 KHz. This would be the highest input frequency consistent with a maximum error of 0.1%.

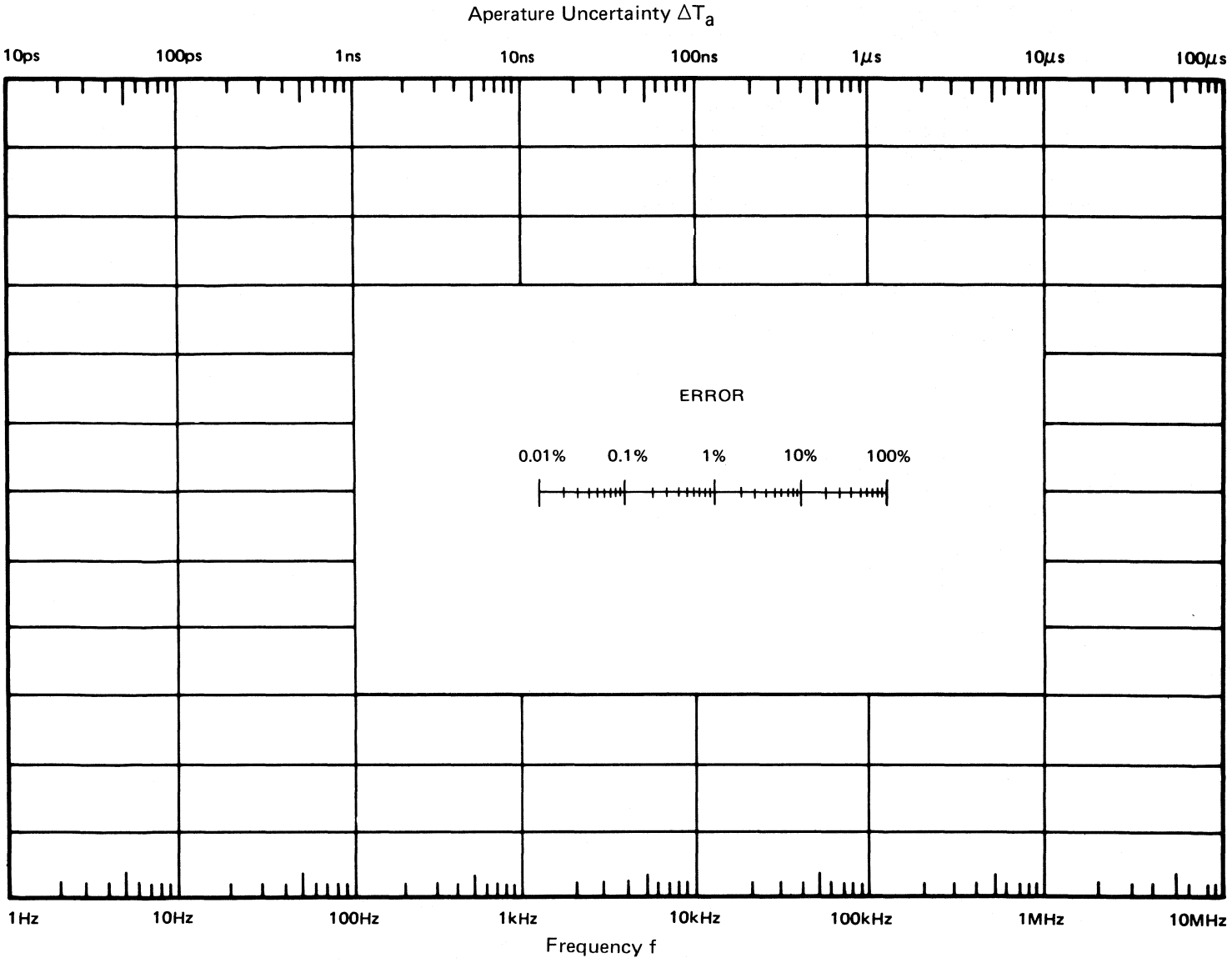


FIGURE 4. NOMOGRAPH FOR ERROR CAUSED BY APERTURE TIME UNCERTAINTY (JITTER)

The nomograph can also be used to show that voltage acquisition errors in the A/D converters can be greatly reduced if a track/hold amplifier precedes the converter. Assume an A/D converter with a conversion time of 2.2μs and an input with a maximum frequency of 20 KHz. In this situation the 2.2μs can be treated as an aperture time uncertainty. Connecting this with the 20 KHz frequency on the nomograph gives a maximum error of 28%. This error can easily be reduced by several orders of magnitude by a T/H or S/H whose aperture time uncertainty is much less than 2.2μs.

MATCHING A T/H OR S/H TO AN A/D CONVERTER

When a S/H or T/H amplifier is used at the input of an A/D converter, the performance of the system will depend on the combined specifications of both units, as well as on their compatibility.

Since the signal should be sampled at a frequency at least twice that of the maximum signal frequency, the maximum signal frequency is equal to one half of the maximum sampling rate of the system. As discussed in the section on Sampling Rate Limitations, the sampling rate of the system depends on the total cycle time. The cycle time is at least as long as the acquisition time + settling time + A/D conversion time, so

$$(f_{SIG})_{MAX} = \frac{1/2}{t_{Acquisition} + t_{Settling} + t_{A/D\ Conversion}}$$

The feedthrough attenuation of the S/H or T/H at f_{SIG} should represent less than 1/4 LSB of the A/D converter. For instance, suppose the converter has 8 bit resolution (1 LSB = 0.4%) and

an 18 MHz clock rate. Then f_{SIG} is 9 MHz max, and at this frequency the S/H should have a maximum feedthrough attenuation of 0.1% (60 dB).

The acquisition time of the S/H or T/H is specified both for the magnitude of the input voltage change and for the percentage to which the final value will be accurate. The acquisition time should be specified both for a sufficiently large input voltage and for settling to within at least 1/2 LSB of the A/D converter.

Aperture time uncertainty (jitter) creates a sample to sample ambiguity in the output voltage when the S/H is processing high frequency signals. As shown in the previous section, the jitter time ΔT_a is related to the maximum percent error at a signal frequency f_{SIG} by:

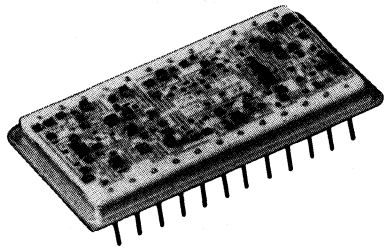
$$\text{maximum \% error} = 628\,(f_{SIG})\,(\Delta T_a).$$

The maximum % error should be less than 1/2 LSB of the A/D converter, so the maximum uncertainty in the aperture time of the S/H or T/H should be:

$$(\Delta T_a)_{max} = \frac{\text{1/2 LSB (expressed as a \%)}}{628\,(f_{SIG})}$$

TH-8530

HYBRID VIDEO TRACK/HOLD
10 ns Acquisition Time; 50 MHz Sampling Rate



FEATURES

- *20 pS APERTURE TIME UNCERTAINTY (JITTER)*
- *1 mV/µs DROOP*
- *9 ns SETTLING TIME TO ±0.1%*
- *±0.2% MAX LINEARITY ERROR (RATED LOAD)*
- *INPUT BUFFER AMPLIFIER*
- *POWER SUPPLIES INTERNALLY DECOUPLED*

DESCRIPTION

The TH-8530 is the world's fastest track and hold amplifier. Its 50 MHz sampling rate actually makes it faster than any existing sample and hold. The TH-8530 is also the smallest T/H or S/H available in its speed range. The 24 pin double DIP module contains all necessary components including the holding capacitor, an FET amplifier to buffer the holding capacitor, an input buffer amplifier, and an ECL compatible gate input. It is a high reliability device, manufactured and processed to conform to MIL-STD-883, DDC procedures.

APPLICATIONS

The TH-8530 is ideal for video processing applications, particularly pulse processing and pulse stretching systems where the pulse duration is very short, such as radar systems or transient analyzers. With a maximum sampling rate of 50 MHz, the TH-8530 is excellent for parallel (or "flash") type A/D converter systems. Other areas where this fast track and hold can be used are communications and television systems.

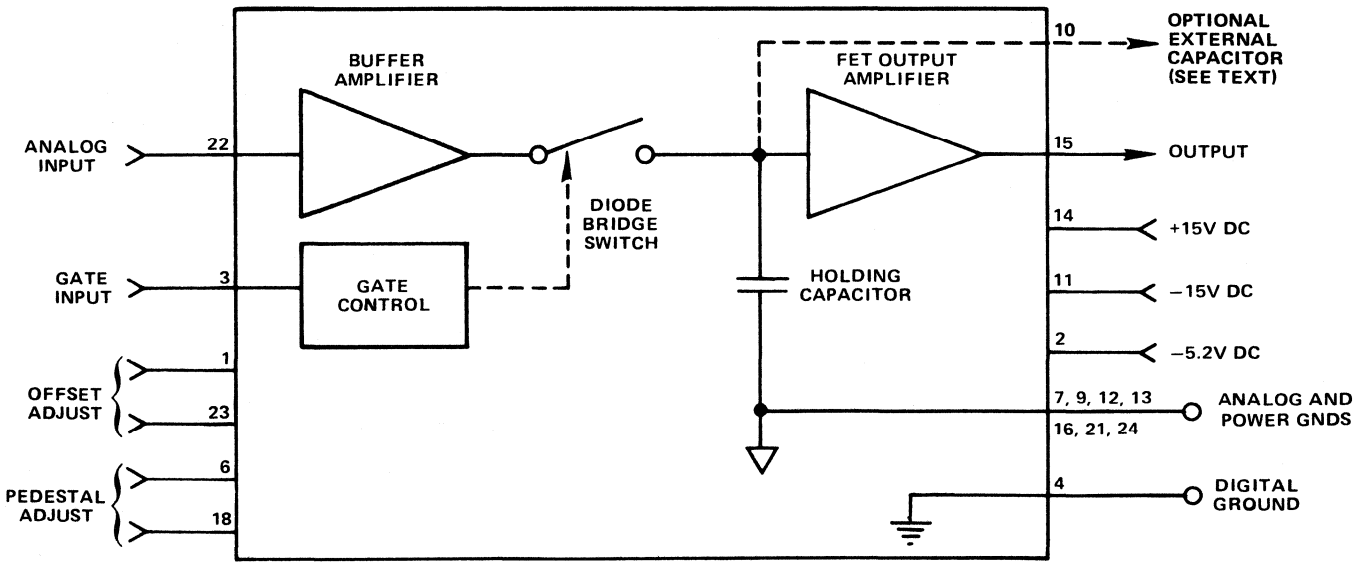


FIGURE 1. TH-8530 BLOCK DIAGRAM

SPECIFICATIONS
At 25°C case temperature and rated supplies unless otherwise indicated.

PARAMETER	UNITS	VALUE
ACCURACY		
Gain		
No load		+0.97 typ
With 200 Ω Rated Load		+0.95 typ; +0.92 min
Gain Tempco	ppm/°C	25 typ; 50 max
Linearity Error		
No Load	% of F.S.	0.1 max
At Rated Load	% of F.S.	0.2 max
Linearity Tempco	ppm/°C	5 typ; 15 max
DC Offset (Trimmable to Zero)	mV	25 typ; 100 max
DC Offset Tempco	µV/°C	40 typ; 100 max
Pedestal (Trimmable to Zero)	mV	25 typ; 100 max
Pedestal Tempco	µV/°C	60 typ; 150 max
DYNAMICS		
Small-Signal Bandwidth (f_t)	MHz	100 typ. 80 min
Slew Rate	V/µsec	400 min
Update Change	V	2 max
Max Sampling Rate (1)	MHz	50 typ; 33 min
Min Cycle Time	ns	15 typ; 25 max
Acquisition Turn-On Delay	ns	3.5 typ; 7 max
Acquisition Time to 0.1% of Final Value		
2V Input Change	ns	10 typ; 15 max
0.2V Input Change	ns	5 typ; 8 max
Aperture Time Delay	ns	3.5 typ; 5 max
Aperture Time Uncertainty (Jitter)	ps	20 typ; 35 max
Feedthrough Attenuation in Hold Mode	dB	60 min through 10 MHz
Settling Time to 0.1% of Final Value (2)	ns	9 typ; 15 max
Droop Rate at 25°C (Case)	mV/µs	1 typ; 10 max
Droop Rate Vs. Temp		Doubles every 10°C
Glitch (From Track to Hold)		
Amplitude	mV	20
Duration	ns	15 (to less than 2 mV)
ANALOG INPUT		
Range For Rated Accuracy	V	±1 max
Absolute Max Without Damage	V	±2.5
Input Impedance	KΩ	100 typ; 20 min
Capacitance	pF	5 typ; 8 max
Bias Current	mA	±0.1 typ; ±0.5 max
GATE INPUT		
Type		ECL compatible (external pulldown req'd)
Logic Levels	V	−0.8 = Logic 1 = Hold −1.6 = Logic 0 = Track
OUTPUT		
Voltage Range	V	±1 max
Steady State Current	mA	±5 max
Transient Current	mA	±50 max
Output Impedance	Ω	4 typ; 10 max
POWER REQUIREMENTS		
Supply Voltages	V	+15 ± 5% / −15 ± 5% / −5.2 ± 5%
Absolute Max Voltage	V	+18 / −18 / −7
Current	mA	55 typ / 55 typ / 45 typ 65 max / 65 max / 55 max
Power Dissipation	W	1.9 average
TEMPERATURE RANGE (CASE)		
Operating		
−1 Option	°C	−55 to +85
−3 Option	°C	0 to +70
Storage	°C	−55 to +125
PHYSICAL		
Type		24 pin DDIP
Size	inch	1.4 x 0.8 x 0.2 (3.6 x 2.0 x .51 cm)
Weight	oz	.42 typ (11.9 g)

NOTES:
1. Sampling rate for 0.1% dynamic error.
2. Settling time into Hold mode.

TECHNICAL INFORMATION

INTRODUCTION

The TH-8530 track and hold amplifier (Figure 1) consists basically of a voltage holding capacitor connected to the input signal through a switch. The input signal and output voltages are both buffered by amplifiers. The switch is controlled by an ECL logic gate signal which determines whether the holding capacitor voltage and output voltage will track the input signal (switch closed, logic 0) or will be held constant, retaining the value of the input at the moment the switch opens (switch open, logic 1).

The TH-8530 is available in several optional electrical configurations. Provision for the use of an external holding capacitor has been made available on Pin 10 (See Pin Connection Table). Because the external capacitor is connected in parallel with the internal capacitor, this option reduces the effects of droop and extends holding time. Acquisition time, however, is increased by the presence of additional capacitance created by this circuitry. This option must be designated when ordering the TH-8530. Include "-10" to the part number for external holding configuration (See Ordering Information).

Unipolar voltage outputs may be ordered, which provide internal offsets of the specified ±1V input range. Option "P" produces 0 to +2V and option "N" produces 0 to -2V at the output (Pin 15). A bipolar output range is available as option "B" (See Ordering Information.)

GROUND CONNECTIONS

To minimize coupling of a gate signal into an output signal, connect the gate signal ground to pin 4 only. Do not connect other grounds to pin 4. Analog input/output and supply voltage grounds can be connected to any of the analog ground pins. The analog grounds are connected together internally and tied to the case. It is best to also connect these grounds together externally to minimize impedances. The analog and digital grounds are separated internally to avoid crosstalk between them and must be tied together externally.

TRIM ADJUSTMENTS

The offset and pedestal are trimmed at the factory to within the limits listed in the specifications table. Further adjustments may be made using the trim adjustments shown in Figure 2. Connect the output (Pin 15) to an oscilloscope and ground the analog input (Pin 22). Apply a 50 nsec negative ECL pulse at a 1 MHz rate to the gate input. Vary the pedestal adjust potentiometer to minimize the pedestal and the offset potentiometer to trim the offset as shown in Figure 3.

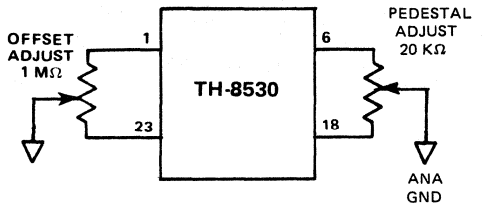


FIGURE 2. TRIM ADJUSTMENT CIRCUITS

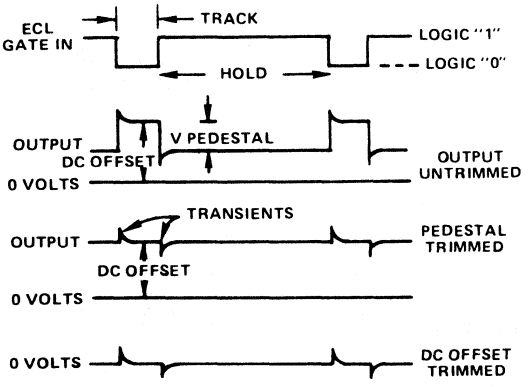
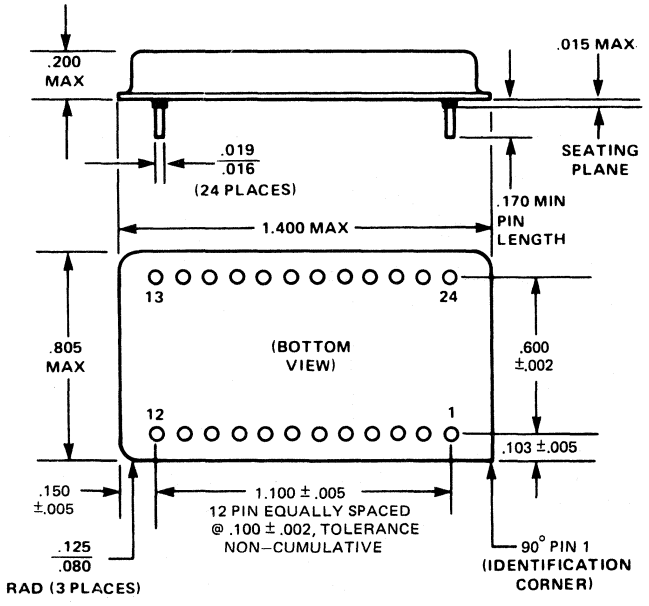


FIGURE 3. SCOPE TRACES DURING OUTPUT TRIM ADJUSTMENTS

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions are shown in inches.
2. Load identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Case tied to analog ground.

RELIABILITY

The use of MSI and thin film resistor chips, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All TH-8530 products are manufactured to meet military standards for high reliability. DDC hybrids are built in conjunction with the requirements of MIL-STD-883 Test Methods and Procedures for Microelectronics. The screening procedures are based on Method 5008.

PIN CONNECTION TABLE

PIN	FUNCTION
1	Offset Adjust
2	–5.2 VDC
3	Gate Input
4	Digital Ground
5	NC
6	Pedestal Adjust
7	Analog Ground
8	NC
9	Analog Ground
10	NC (See Note)
11	–15 VDC
12	Analog Ground
13	Analog Ground
14	+15 VDC
15	Output
16	Analog Ground
17	NC
18	Pedestal Adjust
19	NC
20	NC
21	Analog Ground
22	Analog Input
23	Offset Adjust
24	Analog Ground

Note: Pin 10 for external capacitor on special order only.

ORDERING INFORMATION

TH-8530 – 1 – B – 10 – 883B

883B = MIL-STD-883 Processing:
- 883B = Conforms to MIL-STD-883 DDC procedures.
- Blank = Same, except pre-burn in test and burn in are omitted.

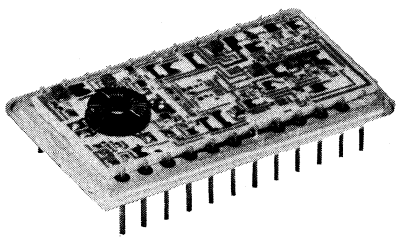
10 = Pin 10 connected to the holding capacitor.
Blank = No connection.

Output Voltage Range (all with ± 1V input):
- B = –1V to + 1V
- N = 0 to – 2V
- P = 0 to + 2V

Temperature Range (Case):
- –1 = –55° C to +85° C
- –3 = 0° C to +70° C

ILC DATA DEVICE CORPORATION

HYBRID VIDEO/PULSE SAMPLE/HOLD
30 ns Acquisition Time; 20 MHz Sampling Rate



FEATURES

- *20 pS APETURE TIME UNCERTAINTY (JITTER)*
- *0.2 mV/μs DROOP*
- *20 ns SETTLING TIME TO 0.1%*
- *0.05% LINEARITY ERROR*
- *INPUT BUFFER AMPLIFIER*

DESCRIPTION

The SH-8518 video/pulse sample and hold amplifier is the smallest video sample and hold module available, complete in a 24-pin double DIP hermetically sealed metal package. The module includes all necessary components, including the holding capacitor, FET amplifiers to buffer the input and output signals, and a TTL compatible gate control. It is a highly reliability device manufactured and processed to meet the requirements of MIL-STD-883.

APPLICATIONS

The SH-8518 is well suited for a variety of video processing applications in communications, radar, and television systems. It can be used very effectively in pulse processing and pulse stretching applications, as in radar systems or transient analyzers. With a maximum sampling rate of 20MHz, the SH-8518 is ideal for multiplexed A/D converter systems, and for use with high speed A/D converters such as DDC's 8-bit hybrid ADH-8512.

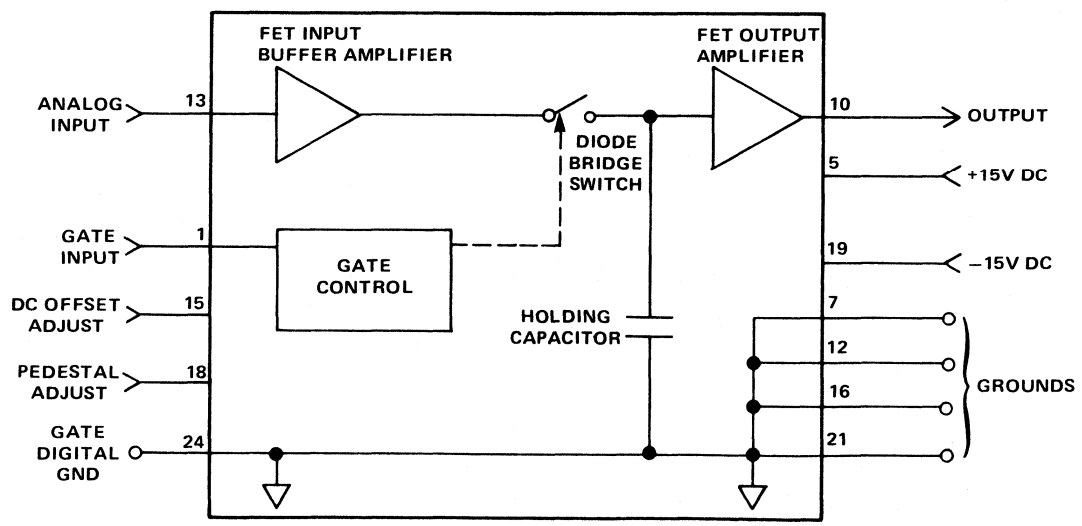


FIGURE 1. SH-8518, BLOCK DIAGRAM

SH-8518 SPECIFICATIONS

At 25° C case temperature and rated supplies

PARAMETER	UNIT	VALUE
ACCURACY		
Gain		+0.975 no load: +0.96 typ with 500-ohm rated road
Gain Tempco	PPM/°C	25 typ; 50 max
Linearity Error:		
For ±2.5V Input	% of F.S.	< 0.05 typ; 0.1 max
For ±3.5V Input	% of F.S.	0.2 max with ±5V max sample-to-sample change
Linearity Tempco	PPM/°C	5 typ; 15 max
DC Offset (trimmable to zero)	mV	20 typ; 100 max
DC Offset Tempco	µV/°C	40 typ; 100 max
Pedestal (trimmable to zero)	mV	100 typ; 300 max
Pedestal Tempco	µV/°C	50 typ; 100 max
DYNAMICS		
Small-Signal Bandwidth (f_t)	MHz	100 typ; 80 min
Slew Rate	V/µs	600 typ; 400 min
Update Change	V	±5 max
Max Sampling Rate	MHz	15 min; 20 typ
Min Cycle Time	ns	66.7 max; 50 typ
Duty Cycle (Ratio of Sample Time to Cycle Time)	%	< 80
Max Sample Time	ns	100
Acquisition Turn-On Delay	ns	8 typ; 10 max
Acquisition Time (T_A) to 0.1% of Final Value (Includes Delay):		
±5V Input Change	ns	30 typ; 35 max
±1V Input Change	ns	25 typ; 30 max
Aperture Time Delay (T_a)	ns	5 typ; 8 max
Aperture Time Delay Uncertainty (Jitter) (ΔT_a)	ps	20 typ; 35 max
Feedthrough Attenuation in Hold Mode	db	66 typ; 60 min, DC through 10 MHz
Settling Time (To within ±0.1% of Final Value):		
For +5V Input Change	ns	30 max
For ±1V Input Change	ns	20 max
Droop Rate at 25°C (Case)	mV/µs	0.2 typ; 5 max
Droop Rate Temperature Dependence		Doubles every 10°C

PARAMETER	UNIT	VALUE
ANALOG INPUT		
Signal Voltage Range	V	± 2.5 max for full linearity; ± 3.5 max for reduced linearity (see linearity specification)
Impedance		$10^{10}\ \Omega$ min plus 5 pf max
GATE INPUT		
Type		TTL Compatible
Load		2 standard TTL unit loads max
Logic Levels		Logic 1 = sample mode Logic 0 = Hold mode
OUTPUT		
Max Voltage	V	±3.5 min
Max Current	mA	±5 min
Impedance	Ω	10 max
Short Circuit Protection to Ground		Up to max allowable operating case temperature
POWER REQUIREMENTS		
Supply Voltages	VDC	+15±5% / −15 ±5%
Absolute Max Voltage	VDC	+18 / −18
Current Max	mA	55 typ; (1) 70 max / 50 typ; 60 max
Power Dissipation	W	1.6 average
TEMPERATURE RANGE (CASE)		
Operating:		
−1 Option	°C	-55 to +85
−3 Option	°C	0 to +70
Storage	°C	-55 to +125
Thermal Resistance	°C/W	θCA = 30
PHYSICAL		
Type		24-pin double DIP
Size	inch	1.4 x 0.8 x 0.28 (3.6 x 2.0 x 0.71 cm)
Weight	oz	0.42 (11.9g) typ

NOTES: (1) 55 mA for 10% T/H duty cycle.
125 mA for 50% T/H duty cycle.

TECHNICAL INFORMATION

1. INTRODUCTION

The SH-8518 Sample and Hold (S/H) amplifier (Figure 1) consists basically of a voltage holding capacitor connected to the input signal through a switch. The input signal and output voltage from the holding capacitor are both buffered by FET amplifiers. The switch is controlled by a TTL logic gate signal which determines whether the capacitor and therefore output voltage follows the input signal (switch closed, logic 1) or remains constant, retaining a particular value of the input voltage (switch open, logic 0).

In a S/H amplifier such as the SH-8518 the gate is AC coupled to the switch, so that very short gate pulses are used and the input signal is sampled only briefly. This usually allows shorter acquisition times and greater sampling rates than with a track and hold amplifier in which the gate is DC coupled to the switch. Because of the AC coupling, the SH-8518 sample time must be less than 100ns. For applications requiring longer sample times, consider DDC's track and hold amplifiers, which have no limitation on the tracking time.

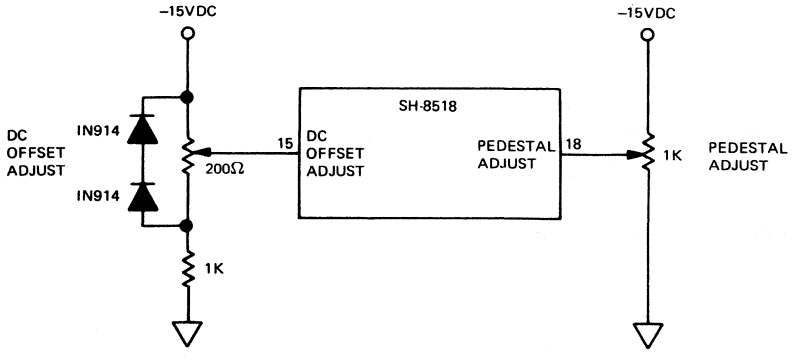


FIGURE 2. TRIM ADJUSTMENT CIRCUITS

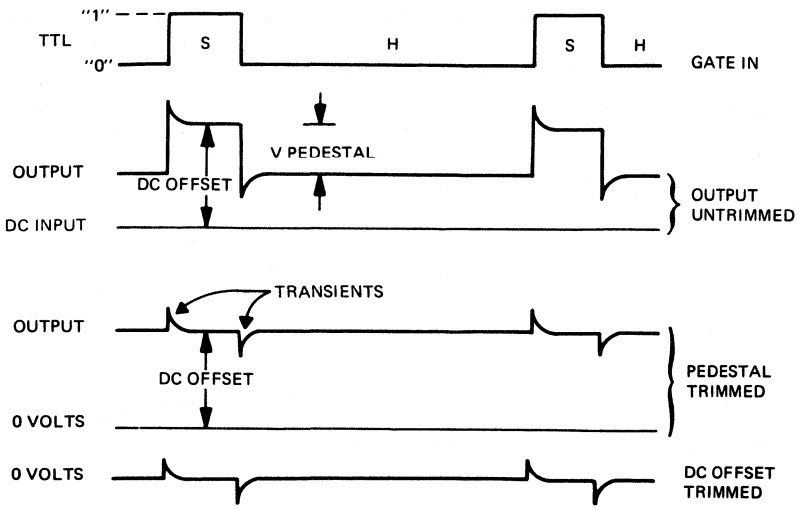
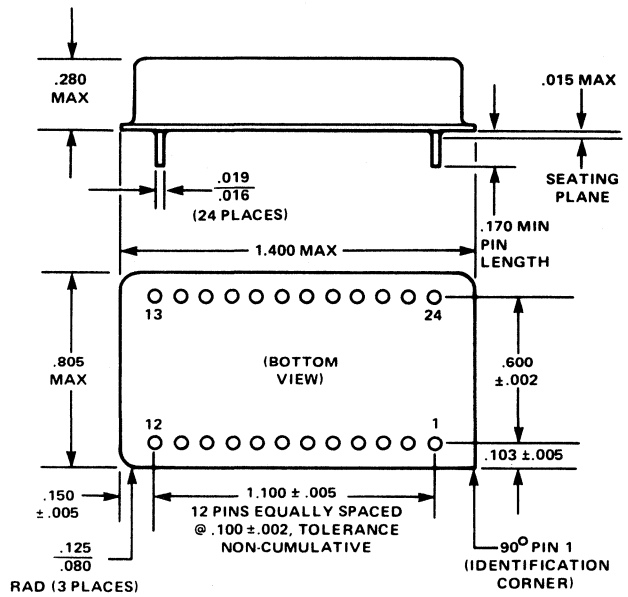


FIGURE 3. SCOPE TRACES DURING OUTPUT TRIM ADJUSTMENTS

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions are shown in inches.
2. Load identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

ORDERING INFORMATION

SH-8518-1 – 883B

- MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883 DDC procedures
  - Blank = Same, except pre-burn in test and burn in are omitted.
- Operating Temperature Range (case):
  - –1 = 55°C to +85°C
  - –3 = 0°C to +70°C

The terminology, signal relationships, and major design considerations for sample/holds such as the SH-8518 are discussed in the Background Information at the front of the S/H and T/H section of this catalog.

2. GROUND CONNECTIONS

To minimize inadvertent coupling of a gate signal onto an output signal, connect the gate signal between pins 1 and 24 only. Do not connect any other grounds to pin 24. Analog input, output, and supply voltage grounds can be connected to ground pins 7, 12, 16 and 21 as convenient. These four pins should be connected together externally to minimize impedances. All grounds are tied together internally and connected to the case.

3. TRIM ADJUSTMENTS

The DC Offset and Pedestal are trimmed at the factory to within the limits listed in the specifications table. Further adjustments may be made after installation using the trim adjustment circuit shown in Figure 2. Connect the Output (pin 10) to an oscilloscope and ground the Analog Input (pin 13). Apply approximately 30ns positive TTL pulse at a rate of about 1MHz to the Gate Input (pin 1). Vary the Pedestal Adjust potentiometer to minimize the pedestal and the DC Offset potentiometer to trim the offset as depicted in Figure 3.

4. RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

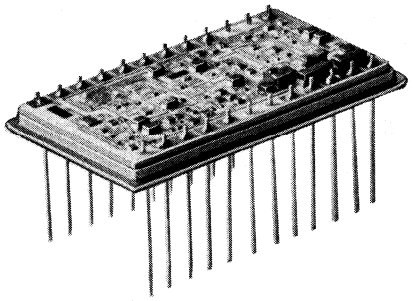
All SH-8518 hybrids are built in accordance with requirements of MIL-STD-883 and screening is based on the requirements of Method 5008 (DDC procedures) except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) is 327,000 hours, Ground Fixed, at 25°C.

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Gate Input	13	Analog Input
2	N.C.	14	N.C.
3	N.C.	15	DC Offset Adjust
4	N.C.	16	Ground
5	+15VDC	17	N.C.
6	N.C.	18	Pedestal Adjust
7	Ground	19	-15VDC
8	N.C.	20	N.C.
9	N.C.	21	Ground
10	Output	22	N.C.
11	N.C.	23	N.C.
12	Ground	24	Gate Digital Ground

All grounds are tied to the case.

ADH-050 AND ADH-051



HYBRID VIDEO TRACK/HOLD
100 ns Acquisition Time;
± 0.0125% Max Linearity Error

DESCRIPTION

The industry's first hybrid video track and hold module, the ADH-050 features small size, fast acquisition time (100 ns, typ.) and low aperture time uncertainty (500 ps, max.). Standard processing with no added cost conforms to MIL-STD-883 except for burn-in which is an option.

The Model ADH-051 has a larger hold capacitor than the ADH-050. The larger capacitor reduces the hold drift rate by a factor of five, with a corresponding increase in acquisition time and decrease in bandwidth.

Included as standard in all units is a pin programmable input buffer amplifier which may be used differentially, single ended, or as a follower with $10^7\Omega$ input impedance. Linearity is better than .0125%, making the ADH-050 suitable for use in 12 bit systems. No adjustment, trimming, or periodic calibrations are required.

APPLICATIONS

The Model ADH-050 is designed for track/hold requirements for video digitizing. It is ideal for avionics and other high reliability applications. Other uses include high-speed data processing systems and A/D converters.

FEATURES

- *500 pS APERTURE TIME UNCERTAINTY (JITTER)*
- *0.1 mV/μs Ddroop*
- *70 ns TYP SETTLING TIME TO ±2 mV*
- *PIN PROGRAMMABLE INPUT BUFFER AMPLIFIER*
- *POWER SUPPLIES INTERNALLY DECOUPLED*

SPECIFICATIONS

At 25° and nominal supply voltages unless otherwise noted.

PARAMETER	UNITS	VALUE	
ACCURACY (AC, in to out, referred to 10V full scale range)			
Gain (pin programmable)		−1; ±1/2; ±2	
Gain Error	%	0.1 max	
Gain Tempco	ppm/°C	2 typ; 5 max	
Linearity Error	%	±0.0125 max	
Linearity Tempco	ppm/°C	2 typ; 5 max	
Track/Hold Amplifier			
Offset	mV	5 typ; 20 max	
Offset Tempco	μV/°C	20 typ; 50 max	
Pedestal	mV	20 typ. 30 max	
Pedestal Tempco	μV/°C	10 typ; 25 max	
Buffer Amplifier			
Offset, Referred to Buffer Input	mV	1 typ; 3 max	
Offset Tempco	μV/°C	20 typ; 50 max	
Note: See Tempco Values for case temp. −55°C to 110°C			
DYNAMIC CHARACTERISTICS		ADH-050	ADH-051
Small Signal Bandwidth			
Track/Hold Stage	MHz	15 typ	3.5 typ
Buffer Stage (Follower)	MHz	5 typ	5 typ
Slew Rate			
Track/Hold	V/μs	200 typ	80 typ
Buffer Amplifier	V/μs	60 typ	60 typ
Aperture			
Time Delay	ns	5 max	5 max
Delay Uncertainty (Jitter)	ps	500 max	1000 max
Acquisition Time			
±5V T/H Amplifier Input	ns	100 typ	500 typ
	ns	120 max	600 max
±1V T/H Amplifier Input	ns	90 typ	450 typ
	ns	100 max	500 max
Settling Time (To Within +2 mV of Final Value)			
T/H Amplifier in Track Mode	ns	100 max, 70 typ	
Buffer Amplifier	ns	500 max	
Feedthrough Attenuation (Hold Model)	dB	80 typ	80 typ
	dB	60 max	66 max
Droop Rate at 25°C Case Temp.	mV/μs	0.1 max	0.02 max
Droop Rate Temperature Dependence		Doubles every 10°C	
Note: For lower droop rates, consult factory			

PARAMETER	UNITS	VALUE
ANALOG INPUT		
Input Capacitance w/without Buffer	pF	15 max
Absolute Max Voltage, w/without Buffer	V	±15
Without Buffer Amplifier		
Input Voltage Range	V	±5
Input Impedance	Ω	300
Buffer Amplifier Characteristics		
Impedance as Follower	Ω	10^7 min
Bias Current	na	100 typ; 250 max
Output Voltage Range	V	±5 max
Buffer as Differential Amplifier		
Input Voltage Range	V	±2.5 min
Common Mode Range	V	±10 max
Input Impedance (Differential)	Ω	1000 typ
Buffer as Single Ended Amplifier		
Input Voltage Range	V	±2.5 max
Impedance	Ω	1500 typ
Note: A gain of 1/2 is also pin-programmable – see text		
LOGIC INPUT		
Track Mode Current (-0.8V, Logic 1)	mA	2.2 typ
Hold Mode Current (-1.8V, Logic 0)	mA	1.7 typ
OUTPUT		
Voltage Swing	V	±6 min
Current Range	mA	±10 min
Impedance	Ω	0.1 max
Short Circuit Protection		(up to one minute)
POWER REQUIREMENTS		
Supply Voltages	V	+15 ± 5% / −15 ± 5% / −5.2 ± 5%
Absolute Max Without Damage	V	+18 / −18 / −7
Current	mA	75 max / 55 max / 55 max
THERMAL CHARACTERISTICS		
Operating Temperature (Case)	°C	−55 to +110
Storage Temperature	°C	−55 to +125
Thermal Resistance, Case to Air	°C/Watt	θ_{CA} = 20 typ
PHYSICAL CHARACTERISTICS		
Size (24 Pin Double DIP)	inch	1.4 x 0.8 x 0.28 (3.6 x 2.0 x 0.71 cm)
Weight	oz	0.42 typ (11.9 g)

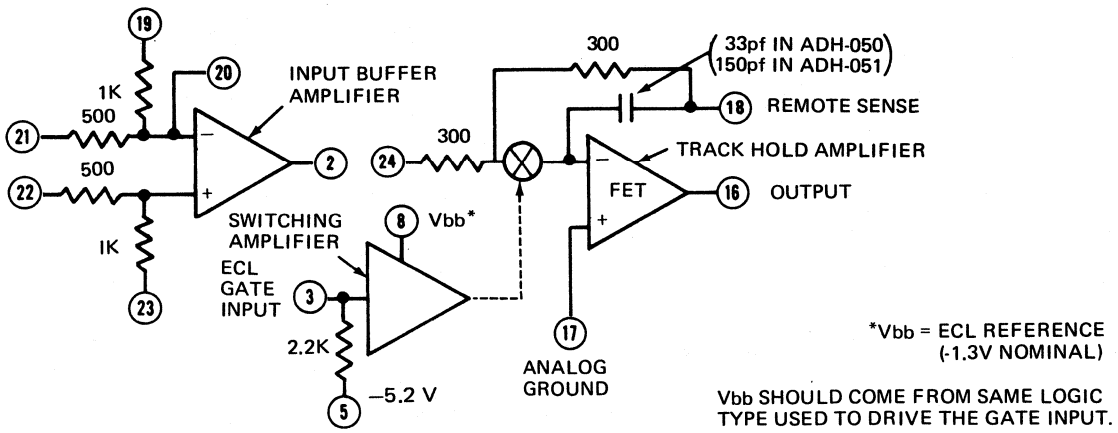


FIGURE 1. ADH-050/051 BLOCK DIAGRAM

TECHNICAL INFORMATION

1. INTRODUCTION

The ADH-050 consists of two parts (Figure 1); a track and hold amplifier with an ECL logic gate input and a gain of -1, and an input buffer amplifier. Depending on the external pin connections, the buffer amplifier may be either by-passed or connected in various ways, as described below.

With the ECL gate at -0.8V (logic 1), the output will track the input with no time limitation. The output is D.C. coupled and there is no duty cycle restriction. On application of -1.8V to the gate (logic 0), the output switches to a "hold" condition, the voltage being held constant by a holding capacitor. Slow leakage from this capacitor causes the output to drift, or droop, in a systematic way as indicated in the specifications.

In a track/hold amplifier such as the ADH-050, the switch is DC coupled to the gate and there is no limitation on the tracking time. In a sample/hold amplifier, the switch is AC coupled, and the input signal is sampled briefly. This usually allows shorter acquisition times and greater sampling rates. Consider the sample/hold amplifiers in the DDC product line for such applications.

The terminology, signal relationships, and major design considerations for track/holds such as the ADH-050 and ADH-051 are discussed in the Background Information at the front of the S/H and T/H section of this catalog.

2. INPUT BUFFER AMPLIFIER

The input buffer amplifier may be connected in a variety of ways. The follower configuration shown in Figure 2 provides an input impedance greater than 10^7 ohm and is useful for multiplexing. Differential and single ended inputs with a gain of 2 may be obtained as in Figures 3 and 4. The gain may be reduced to 1/2 in the circuits of Figures 3 and 4 by interchanging pins 19 and 21, and pins 22 and 23. With a gain of 1/2, the allowable input voltage is ±10V.

Caution: use of external resistors to adjust the gain may greatly increase temperature effects. The internal resistances of the buffer amplifier have been precisely adjusted to provide a gain tempco of less than 3 ppm.

In the differential amplifier configuration shown in Figure 3, any common mode voltage e_{cm} must be less than ±10V.

The bandwidth of the buffer amplifier can be reduced by connecting a capacitor between pins 20 and 19. This may be useful in reducing the input analog signal noise level.

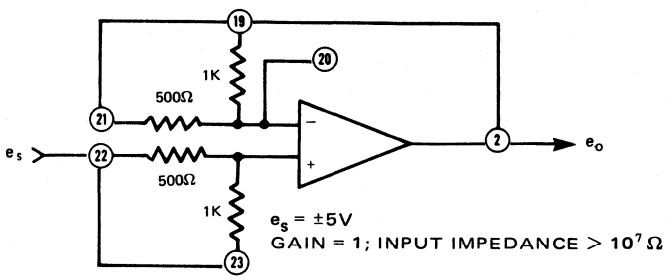


FIGURE 2. BUFFER AMPLIFIER CONNECTED AS FOLLOWER

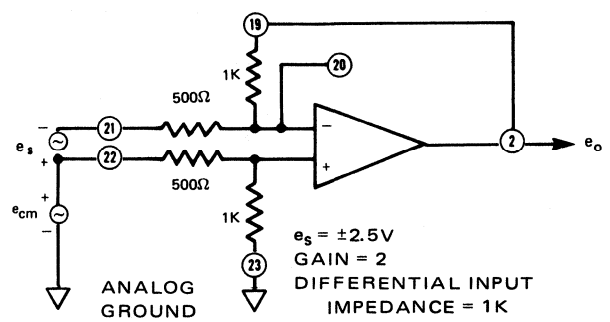


FIGURE 3. BUFFER AMPLIFIER CONNECTED AS DIFFERENTIAL AMPLIFIER

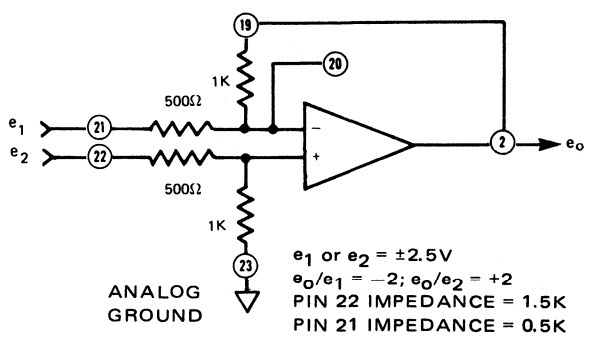
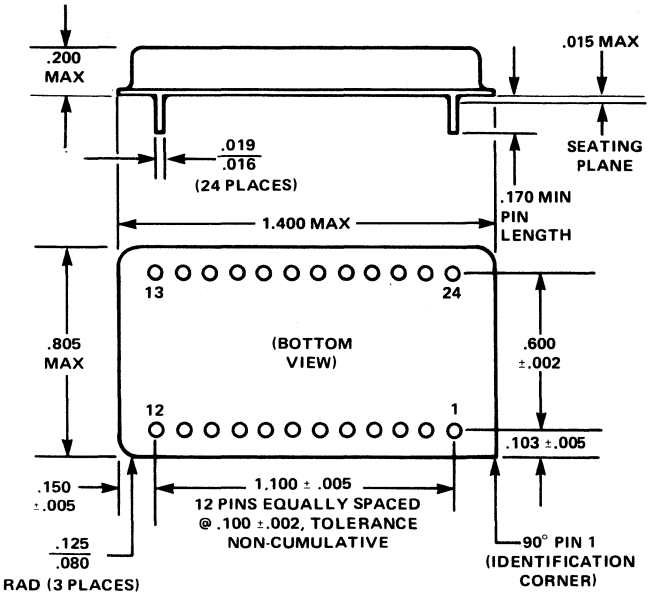


FIGURE 4. BUFFER AMPLIFIER CONNECTED AS SINGLE ENDED AMPLIFIER

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

PIN CONNECTION TABLE

PIN NO.	FUNCTION
1	N.C.
2	Buffer Out
3	T/H Gate In
4	Power Ground
5	-5.2V In
6	N.C.
7	N.C.
8	Vbb In
9	-15V In
10	Power Ground
11	Power Ground
12	+15V In
13	Power Ground
14	N.C.
15	N.C.
16	T/H Output
17	Analog GND
18	T/H Remote Sense (FDBK)
19	Buffer FDBK
20	Buffer S Pt.
21	Buffer (-) In
22	Buffer (+) In No. 1
23	Buffer (+) In No. 2
24	T/H In

Case is connected to Power Ground. Analog Ground is separate from Power Ground.

ORDERING INFORMATION

ADH-050 – 883B

- 883B: MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883 DDC procedures
  - Blank = Same, except pre burn in test and burn in are omitted
- 050: Hold Capacitor Size:
  - 050 = Standard droop rate
  - 051 = 1/5 standard droop rate

When the buffer amplifier is bypassed, the small signal bandwidth and slew rate are somewhat greater, as indicated in the specifications.

3. LOGIC GATE

The ECL gate signal must be high (-0.8V) for the track mode and low (-1.8V) for the hold mode. To ensure positive operation, the -1.3V Vbb voltage supplied to pin 8 on the ADH-050 should come from the gate logic. An ECL gate such as the 10115 includes an appropriate Vbb output generator. When using TTL logic, a TTL to ECL translator such as the 10124 may be used, or a circuit such as shown in Figure 5.

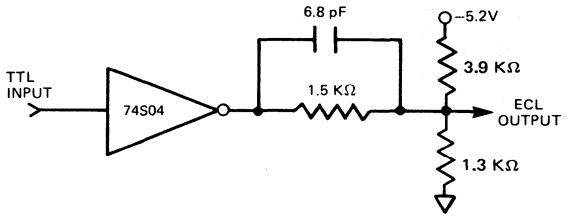


FIGURE 5. CIRCUIT TO PROVIDE ECL GATE FROM TTL LOGIC

4. POWER SUPPLIES

For protection during testing and evaluation, all power supplies should be regulated to ±0.1% and should have current limiting. Set the current limiting for each supply to the maximum value listed in the specifications.

5. OUTPUT AND REMOTE SENSE

A remote sense (pin 18) is available to bypass resistance in the output connections, as shown in Figure 6. Pin 18 must be connected to the output from pin 16 at some point to provide necessary feedback.

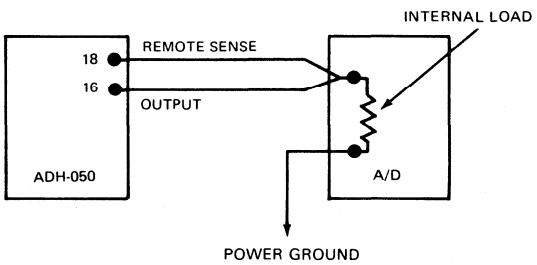


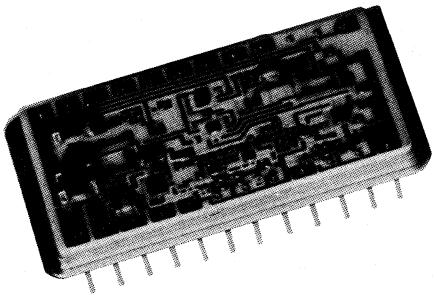
FIGURE 6. OUTPUT CONNECTIONS

6. RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All ADH-050 and ADH-051 hybrids are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5008 except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) is 900,000 hours, Ground Fixed, at 25° C.

13 BIT T/H WITH CONTROLLED HOLD TIME
Deglitcher T/H For CRT's



FEATURES

- *ULTRA LOW GLITCH*
- *10 MHz UPDATE RATE*
- *–60 db FEEDTHROUGH*
- *0.005% TYP LINEARITY ERROR*

DESCRIPTION

The DGL-13 is a track-hold amplifier especially designed for deglitching applications. It will hold a voltage level constant during a glitch interval and then resume tracking. The hold time (50 ns minimum) is determined by an internal timing circuit and may be increased by adding an external capacitor. In normal operation the DGL-13 is strobed just before a glitch is expected to occur, and the internal switch opens 5 ns later to initiate the hold mode. The hold-pulse that opens the switch is available as an output pulse which may be used to initiate an input data change. While tracking, the DGL-13 operates as an op-amp in an inverting mode with an output swing capability of up to ±10V.

APPLICATIONS

The DGL-13 track/hold can be used to deglitch DACs in applications such as cockpit CRT displays and transient sensitive servo systems. It can function as a gated op-amp in digitally controlled frequency synthesizers. The DGL-13 can operate well in the most stringent of industrial and military ground and avionics applications. The processing of DDC hybrids is based on MIL-STD-883 and they are suitable for remotely located and hard to access equipment where high MTBF and small size are critical.

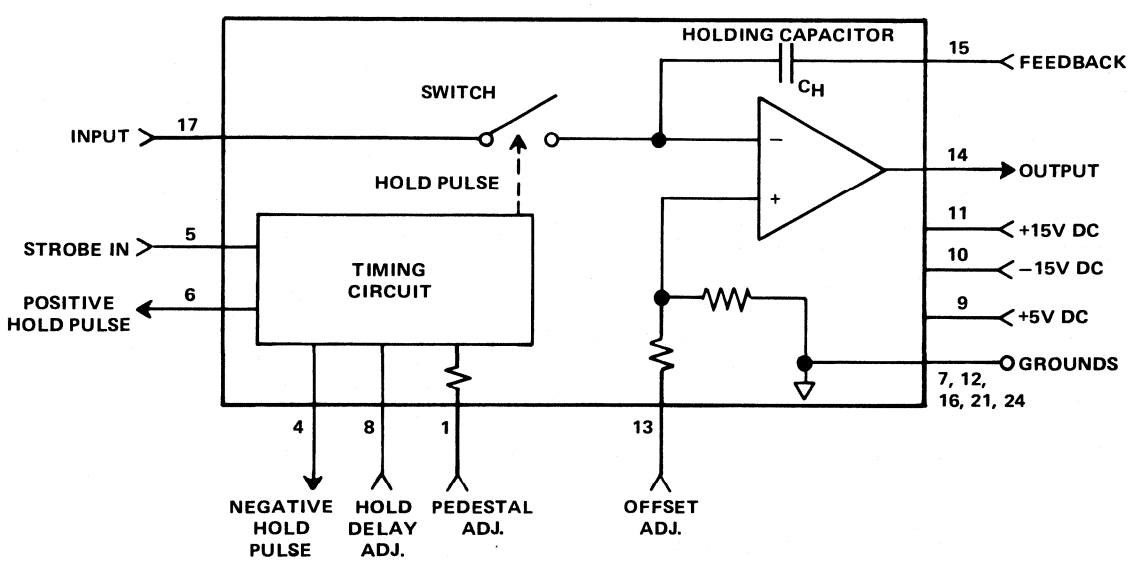


FIGURE 1. DGL-13 BLOCK DIAGRAM

SPECIFICATIONS

At 25° case temperature and at rated power supplies unless otherwise noted.

PARAMETER	UNITS	VALUE
ACCURACY		
Linearity Error	% FSR	0.01 max
Linearity Tempco	ppm FSR/°C	1.0 max
DC Offset	mV	35 max (Trimmable to zero)
DC Offset Tempco	μV/°C	40 max
Pedestal	mV	±10 (Trimmable to zero)
Pedestal Tempco	μV/°C	50 max
DYNAMIC CHARACTERISTICS		
Small Signal Bandwidth (f_t)	MHZ	12 typ; 8 min
Large Signal Voltage Gain		
At 25°C (Case)	V/V	25,000 typ; 15,000 min
Full Temperature Range	V/V	10,000 min
Internal Hold Capacitance (C_H)	pF	10 ± 10%
Slew Rate	V/μs	20 typ; 15 min
Max Sampling Rate	MHz	10
Min Cycle Time	ns	50
Min Hold Time	ns	50 (may be increased by external capacitor)
Acquisition Turn-On Delay	ns	5 typ; 10 max
Acquisition Time		Equal to settling time – see text
Aperature Time Delay	ns	5 typ; 10 max
Aperature Time Uncertainty (Jitter)	ns	1.0 typ
Feedthrough Attenuation in Hold Mode	dB	60 typ
Settling Time		Depends on feedback resistor – see text
Droop Rate	mV/μs	1.0 typ; 10 max
Droop Rate Tempco		Double every 10°C
ANALOG INPUT		
Offset Voltage	mV	50 max
Offset Voltage Average Drift	μV/°C	40
Bias Current at 25°	μA	1 typ; 5 max
Max Input Voltage Without Damage	V	±15

PARAMETER	UNITS	VALUE
LOGIC INPUT/OUTPUT		
Logic Type		TTL compatible
Strobe Input		Positive pulse, 10 ns min Loading is 3 std TTL loads
Positive Hold Pulse Output		Delayed 5 ns nominal with respect to strobe input, pulse length equal to hold time Drive capability is 5 std TTL loads
Negative Hold Pulse Output		Same as positive pulse, except inverted
OUTPUT		
Output Voltage Swing ($R_L \geq 2K\Omega$)	V	12 typ; 10 min
Output Current Range	mA	±5
Max Peak Output Current Without Damage	mA	50
Full Power Bandwidth for ±10V Output	kHz	330 typ; 250 min
Short Circuit Protection to GND	sec	5 at 25°C case temperature 2 at 85°C case temperature
POWER REQUIREMENTS		
Supply Voltages	V	+15 ±2% | −15 ±2% | +5 ±1%
Absolute Max Voltage	V	+18 | −18 | +5.5
Current	mA	4 typ + load | 5 typ + load | 35 typ
Power Dissipation	W	0.85 typ + load
TEMPERATURE RANGE (CASE)		
Operating		
−1 Option	°C	−55 to +85
−3 Option	°C	0 to +70
Storage	°C	−55 to +125
PHYSICAL CHARACTERISTICS		
Size (24 Pin DDIP)	inch	0.8 x 1.4 x 0.2 (2 x 3.6 x 0.5 cm)
Weight	oz	0.38 typ (10.8 g)

TECHNICAL INFORMATION

INTRODUCTION

As shown in the block diagram, Figure 1, the main components of the DGL-13 are an amplifier connected in an inverting mode, a holding capacitor, and a switch controlled by a timing circuit. If the timing circuit is not strobed, the switch remains closed and the output will track the input. When a strobe pulse is applied, its leading edge triggers a one-shot in the timing circuit which, 5 ns later, generates a hold pulse. The leading edge of the hold pulse in turn opens the switch to initiate the hold mode. The output voltage then remains at the voltage stored on the holding capacitor. The hold mode time, which is determined by the timing circuit, is 50 ns typical. The hold time may be increased by adding an external capacitor between pins 4 and 8 (see Figure 4).

The hold pulse is also available as an output strobe at pin 6 to indicate when the switch begins to open. The hold mode output may be used to initiate an input data change.

The five ground pins, 5, 12, 16, 21, and 24, should be connected together externally with a ground plane.

The DGL-13 was designed as a component for the DDAC, a 10 MHz, 13 bit hybrid D/A converter. The DDAC Technical Information section shows how the DGL-13 can be used in a high speed deglitching application.

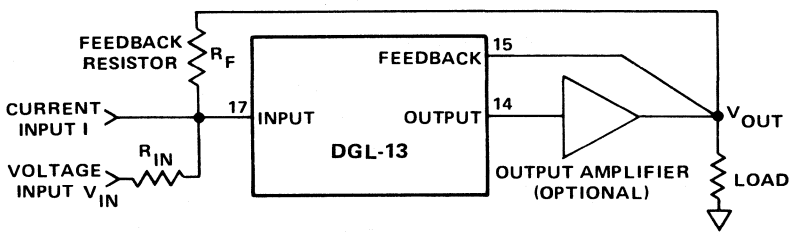


FIGURE 2. SIGNAL INPUT/OUTPUT CONNECTIONS

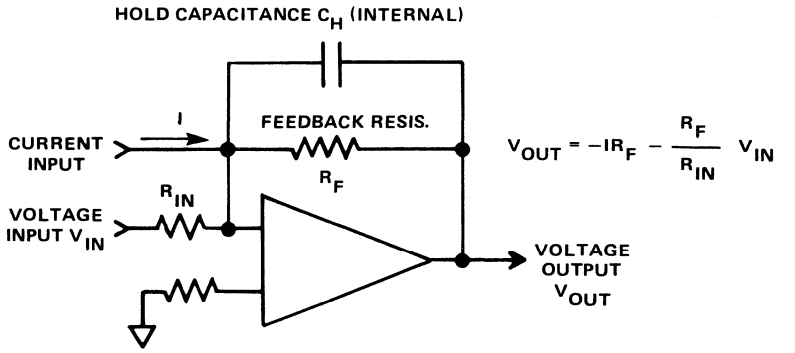


FIGURE 3. EQUIVALENT CIRCUIT IN TRACK MODE

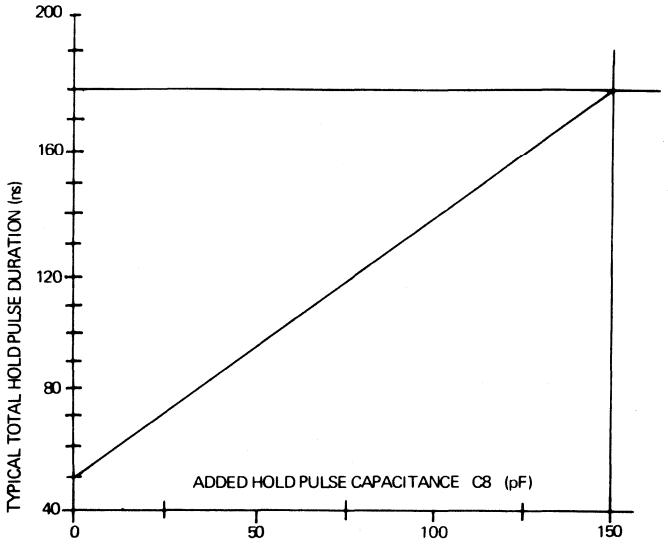


FIGURE 4. HOLD PULSE DURATION VS ADDED CAPACITANCE

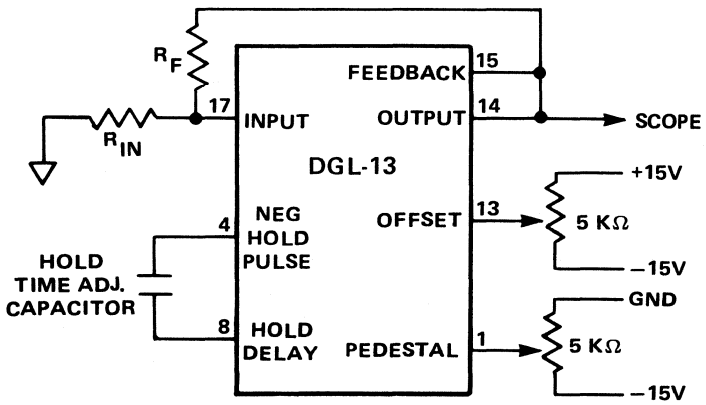


FIGURE 5. ADJUSTMENTS FOR HOLD TIME AND TRIM

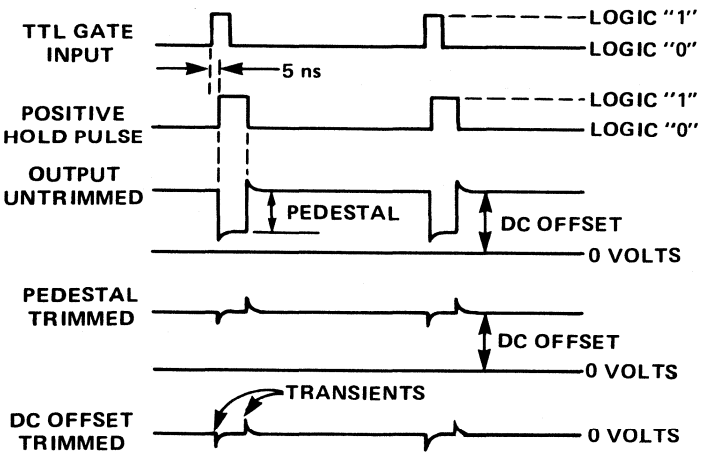


FIGURE 6. SCOPE TRACES DURING OUTPUT TRIM ADJUSTMENTS

INPUT/OUTPUT CONNECTIONS AND SETTLING TIME

Figure 2 shows proper signal input and output connections. The feedback pin 15 and the external feedback resistor R_F should be connected to the output as close to the load as possible to minimize the effects of line resistance. In the tracking mode, the equivalent circuit is that of an inverting amplifier, as shown in Figure 3. The feedback resistor is used to adjust the output scaling. If it is relatively large, it may reduce the bandwidth below the intrinsic bandwidth of the amplifier.

The analog output pin may be grounded for 5 sec at +25°C and 2 sec at +85°C case temperature. It must not be connected to any of the three supplies or damage to the converter will occur.

The DGL-13 output can provide ±5 mA and a voltage range of ±10V. An optional external current booster amplifier may be added, as shown in Figure 2. DDC's coax cable driver, the HCD-13, will provide up to 500 mA at ±10V for this application, as discussed in the DDAC data sheet.

When switched into the track mode, the DGL-13 output tends to overshoot slightly before settling out. With large voltage changes, the output transition is limited by the 20V/μs slew rate of the amplifier. For 10V changes, the output will settle to within ±0.01% of final value in 1800 ns. The settling time for small signal changes (not limited by slew) is limited by the bandwidth of the internal amplifier, the internal capacitance, and the external resistors. The settling time can be calculated from the following chart and formula:

Number of Time Constants	Output Settles to Within
2.3	10%
4.6	1%
6.9	0.1%
9.2	0.01%

Time Constant (in ns)

$$= \frac{(R_F + R_{IN}) \times 10^3}{2\pi f_t R_{IN}} + C_H R_F$$

where:

f_t = small signal bandwidth in MHz
R_F, R_{IN} = feedback and input resistors in KΩ
C_H = internal hold capacitance in pF.

The acquisition time of the DGL-13 will always be identical to its output settling time. This is because the DGL-13 can be used only in an inverting mode with a feedback capacitor.

TIMING

The minimum hold pulse duration is 50 ns typical, but this interval may be increased to 180 ns or more. The relationship between hold pulse duration and any additional capacitance added between pins 4 and 8 is shown in Figure 4.

The maximum cycling rate of the DGL-13 depends on the settling time after switching to the tracking mode, on the delay, and on the hold time in the hold mode. For instance, assume a time constant of 90 ns and that settling is required to ±10%. The table in the previous section shows that ±10% settling requires 2.3 time constants so the settling time is 2.3 x 90 = 207 ns. If the hold time has not been increased beyond 50 ns, the total time is:

207 ns,	for Settling
50 ns	for Hold Time
5 ns	for Delay
262 ns	Total Interval

The maximum cycling rate will then be 1/262 ns = 3.82 MHz. A slower rate is acceptable, but a faster rate will not allow sufficient time for settling.

TRIM ADJUSTMENTS

The DC offset and pedestal are trimmed at the factory to within the limits listed in the specifications table. Further adjustments may be made after installation using the trim adjustment circuit shown in Figure 5. Connect the output (pin 14) to an oscilloscope and ground the input (pin 17) through an input resistor R_{IN}. The trim settings will depend on the values of R_{IN} and R_F. Apply an approximately 30 ns positive TTL pulse at a rate of about 1 MHz to the strobe input (pin 5). Vary the pedestal adjust potentiometer to minimize the pedestal and the DC offset potentiometer to trim the offset as depicted in Figure 6.

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All DGL-13 hybrids are built in accordance with requirements of MIL-STD-883 and screening is based on the requirements of Method 5008 except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number.

ORDERING INFORMATION

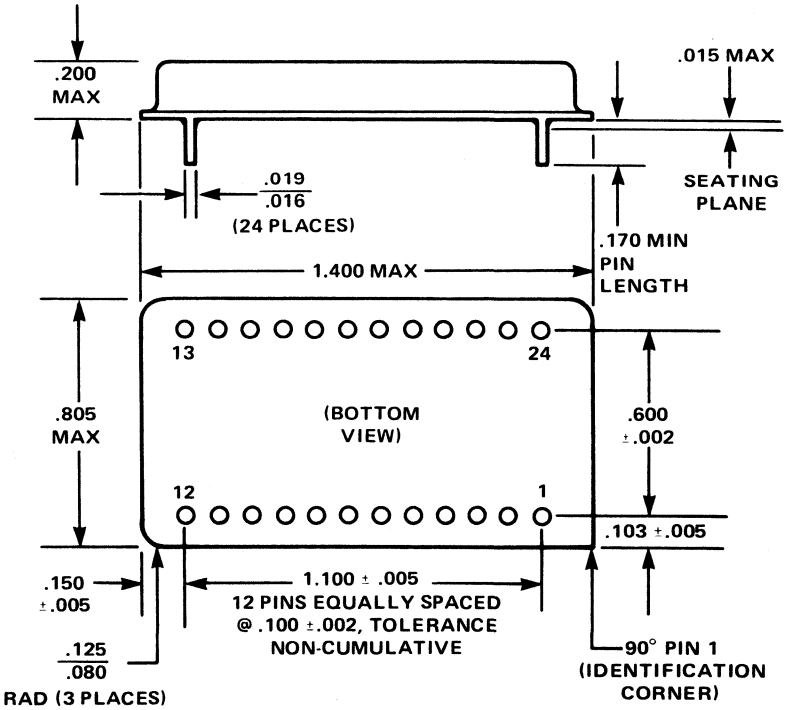
DGL – 13 – 1 – 883B

- 883B: MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883 DDC procedures
  - Blank = Same, except pre-burn in test and burn in are omitted.
- 1: Operating Temperature Range (Case):
  - –1 = –55°C to +85°C
  - –3 = 0°C to +70°C

PIN CONNECTION TABLE

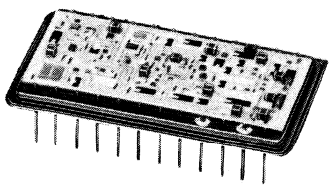
PIN	FUNCTION
1	Pedestal Adjust
2	N.C.
3	N.C.
4	Negative hold pulse
5	Strobe input
6	Positive hold pulse
7	Ground (To Case)
8	Delay adjust
9	+5VDC
10	–15VDC
11	+15VDC
12	Ground (To Case)
13	Offset adjust
14	Analog output
15	Feedback
16	Ground (To Case)
17	Analog input
18	N.C.
19	N.C.
20	N.C.
21	Ground (To Case)
22	N.C.
23	N.C.
24	Ground (To Case)

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions are shown in inches.
2. Load identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

DDC
ILC DATA DEVICE CORPORATION



HIGH SPEED TRACK/HOLD HYBRID
150 nsec Acquisition Time
±0.005% Linearity Error

DESCRIPTION

The THA-05203 is a high speed, high accuracy track/hold amplifier packaged in a hermetic 24 pin DDIP. With its 150 nanosecond acquisition time to 0.01% for a 10 volt step, 0.005% linearity error, 60 picosecond aperture jitter and 74 dB feedthrough attenuation, the THA-05203 is ideal for use in digitizers with data throughput rates up to 5 MHz. Other performance features include −55°C to +125°C operating temperature range, ±10 volt input range, droop rate of 0.5 μV/μsec and small signal bandwidth of 16 MHz. The THA-05203 track/hold is pin for pin compatible with HTC-0300A and TP4860 type units, and offers comparable or superior performance for all parameters.

With its high performance, wide operating temperature range, and small hermetic package, the THA-05203 is ideal for the most demanding military and commercial data acquisition requirements. Typical applications include sonar and radar digitizing, medical and nuclear instrumentation and high speed waveform analyzers.

FEATURES

- *150 NSEC ACQUISITION TIME 10V STEP TO ±0.01% F.S.*
- *60 NSEC SAMPLE TO HOLD SETTLING TIME*
- *50 PSEC APERTURE JITTER*
- *74 dB FEEDTHROUGH ATTENUATION*
- *−55°C to +125°C OPERATING TEMPERATURE RANGE*
- *TTL COMPATIBLE*
- *HTC-0300A AND TP4860 PIN COMPATIBLE*

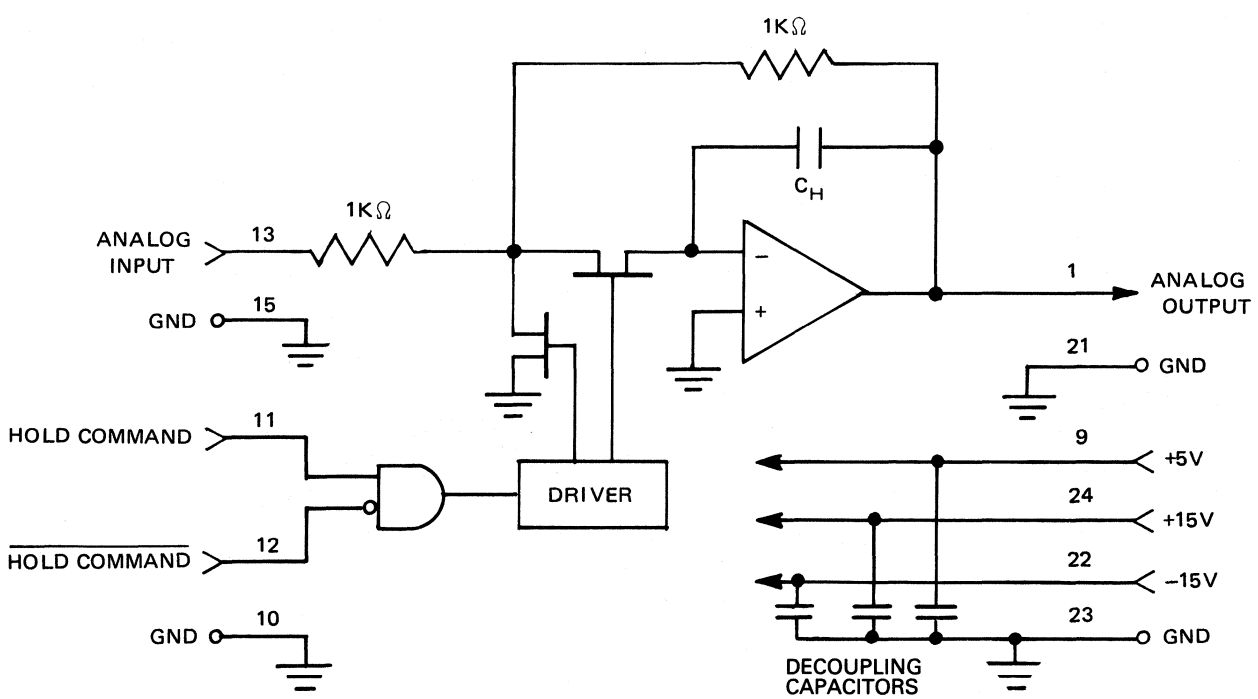


FIGURE 1. THA-05203 BLOCK DIAGRAM

SPECIFICATIONS

(At +25°C and nominal supply voltages unless otherwise noted)

PARAMETER	UNITS	VALUE	
ACCURACY			
Gain	V/V	−1.00±0.1% max	
Gain Tempco	ppm/°C	0.5 typ	5 max
Offset	mV	0.5 typ	5 max
Offset Tempco	ppm FSR/°C	3 typ	15 max
Linearity	% FS	0.005 typ	0.01 max
Pedestal (Hold Mode)	mV	2.5 typ	20 max
Pedestal Tempco	ppm FSR/°C	4 typ	
DYNAMIC CHARACTERISTICS			
Acquisition Time			
To 1% FS for 10V Step	nsec	90 typ	
To 0.1% FS for 10V Step	nsec	100 typ	170 max
To 0.01% FS for 10V Step	nsec	150 typ	200 max
Settling Time (Sample to Hold)			
To 0.1% FS	nsec	40 typ	
To 0.01% FS	nsec	60 typ	100 max
Aperture Jitter (RMS)	psec	50 typ	100 max
Aperture Delay	nsec	6 typ	
Feedthrough Attenuation			
DC to 2.5 MHz, 20V input	dB	74 typ	
Droop Rate			
+25°C	mV/usec	0.0005 typ	0.005 max
+70°C	mV/usec	0.015 typ	
+125°C	mV/usec	1 typ	
Bandwidth (3dB Small Signal)	MHz	16 typ	8 min
Slew Rate	V/usec	300 typ	150 min
Transient (Sample to Hold)	mV p-p	180 typ	
ANALOG INPUT			
Voltage Range	V	±11.5 typ	±10.25 min
Impedance	KΩ	1 typ	
DIGITAL INPUTS			
Logic Levels			
Logic "1"	V	+2.0 min	+5.0 max
Logic "0"	V	0 min	+0.8 max
Logic Loading	TTL	1 load typ	
ANALOG OUTPUT			
Voltage Range	V	±10.25 min	
Current[1]	mA	±50 max	
Impedance	Ω	0.1 typ	
Noise[2]	mV rms	0.1 typ	
Capacitive Load	pF	250 max	
POWER REQUIREMENTS			
Current Drain			
+15V Supply	mA	19 typ	25 max
−15V Supply	mA	21 typ	25 max
+5V Supply	mA	17 typ	25 max
Power Dissipation	mW	685 typ	875 max
Voltage Tolerance			
±15V	%	5 typ	
+5V	%	5 typ	
Power Supply Rejection Ratio	mV/V	±0.5 typ	
TEMPERATURE RANGE (Case)			
Operating			
−1 Option	°C	−55 to +125	
−3 Option	°C	0 to +70	
Storage	°C	−55 to +125	
PHYSICAL CHARACTERISTICS			
Package		24 pin DDIP	
Size	in (mm)	1.4x0.8x0.2 (36x20.3x5.1)	
Weight	oz (g)	0.4 (11.3)	

Notes:
(1) Output is short circuit protected to ground with a current limit of ±65 mA.
(2) Noise is specified in track mode with a 5 MHz bandwidth.

TECHNICAL DESCRIPTION

GENERAL

As shown in the block diagram of Figure 1, the THA-05203 consists of a unity gain inverting op amp with series and shunt switches at its summing point. Placing the track/hold in the track mode causes the series switch to close and the shunt switch to open. In the track mode, the analog output is an inverted version of the analog input. Placing the track/hold in the hold mode causes the series switch to open and the shunt switch to close. In the hold mode, the analog output is held constant by the hold capacitor at the value just prior to the series switch opening.

INPUT/OUTPUT CHARACTERISTICS

As shown in the diagram of Figure 2, the track interval is initiated when the HOLD COMMAND is brought LOW. The output slews as the hold capacitor is charged to a new value. Acquisition time is defined as the time required for the output to settle to within a given error band of its final value, after the HOLD COMMAND goes LOW. Acquisition time for any interval depends on the magnitude of the voltage change since the last interval. The minimum track time must be at least as long as the acquisition time for the largest possible input change. Figure 3 shows THA-05203 error versus acquisition time for a 10 volt input step.

The hold interval is initiated when the HOLD COMMAND is brought HIGH. As shown in Figure 2, there is a short delay, the Aperture Delay, before the series switch opens to isolate the hold capacitor from the analog input. The uncertainty in this delay, called Aperture Jitter, causes an error in the output when the input slews fast. Figure 4 shows aperture jitter error versus input slew rate, assuming 100 picosecond aperture jitter.

After the HOLD COMMAND goes HIGH, a transient appears on the output due to charge transfer across the series switch. A Settling Time (Sample to Hold) interval elapses before the output reaches a given error band of its final value. The track/hold output has not achieved rated performance until after this settling time interval has elapsed.

The charge transferred across the series switch onto the hold capacitor when the HOLD COMMAND goes HIGH causes a step error at the output. This Pedestal error is constant for every hold interval and does not vary with input voltage.

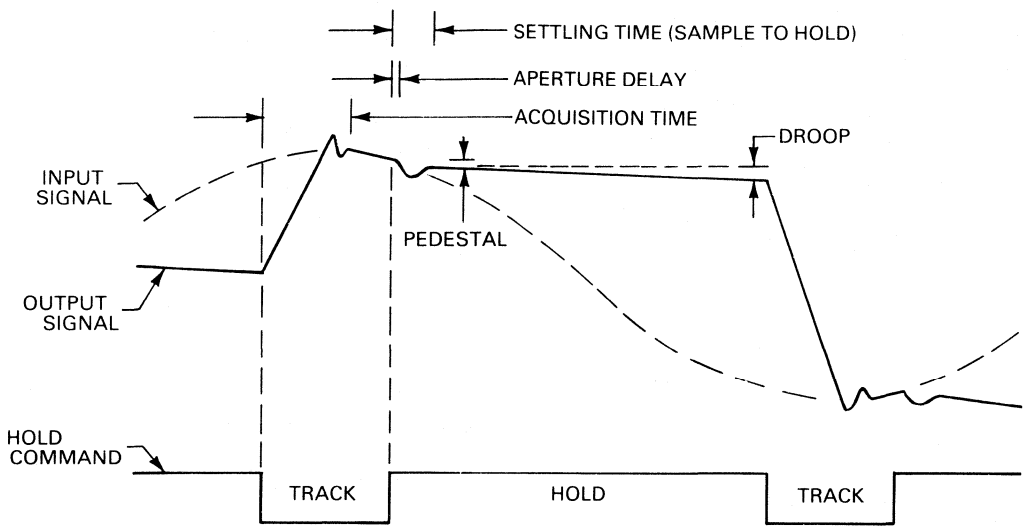


FIGURE 2. INPUT/OUTPUT CHARACTERISTICS

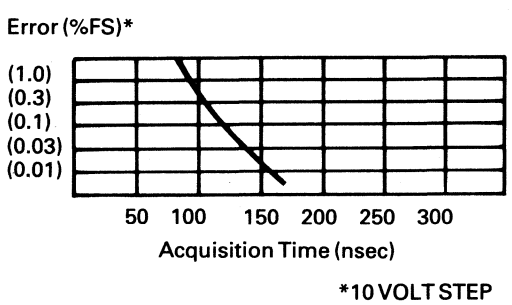


FIGURE 3. ERROR vs. ACQUISITION TIME

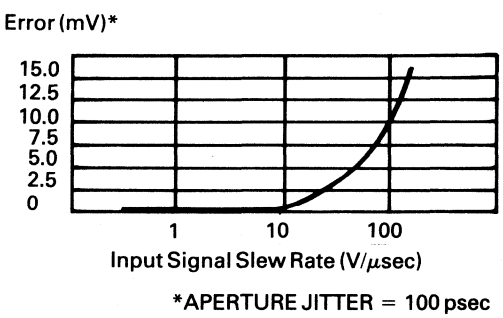


FIGURE 4. APERTURE ERROR vs. SLEW RATE

During the hold interval, the output voltage will increase or decrease linearly with time. This Droop error is caused by charging of the hold capacitor by op amp bias current or series switch leakage current.

Another source of error, during the hold interval, is Feedthrough. Even though the series switch is open, fast slewing input signals can cause the output to change by voltage division across the open switch capacitance. The output error that results will be equal to the input voltage divided by the feedthrough attenuation.

APERTURE ERROR

A track/hold is used with an A/D converter to keep the ADC input constant during the conversion interval. This is because converter input must vary no more than ½ LSB during the conversion time to maintain its accuracy.

The highest allowable frequency, while maintaining less than ½ LSB variation at the A/D converter input, can be calculated with and without the use of a track/hold. The dramatic increase in allowable input frequency when a track/hold is used illustrates why most applications use a track/hold and ADC combination.

The following example assumes a 10 volt sinusoidal input to a 12 bit 2μsec A/D converter, and calculates the frequency at which a ½ LSB change occurs during the aperture interval. With no track/hold, the aperture interval is equal to the ADC conversion time. With a track/hold, the aperture interval is equal to the aperture jitter time.

$$V_{in} = 10 \sin 2\pi ft$$

$$\frac{dV_{in}}{dt} = 20\pi f \cos 2\pi ft$$

$$\left.\frac{dV_{in}}{dt}\right|_{max} = 62.8 f_{max}$$

$$f_{max} = \frac{2.5 \times 10^{-3} \text{ volt}}{(62.8)(\text{Tap})}$$

For no track/hold: Tap = 2×10^{-6} sec

f_{max} = 20 KHz

For track/hold: Tap = 50×10^{-12} sec

f_{max} = 800 KHz

OUTPUT LOADING

Attention must be paid to the resistive and capacitive loading of the THA-05203 to maintain desired performance. Capacitive loads above 50pf will affect track/hold acquisition and settling time. Capacitive loads above 250pf are to be avoided, since the potential for oscillations will result. The recommended resistive load is 500 ohms or higher. Resistive loads as low as 250 ohms may be used, but at this load the potential exists for current limiting non-linearities.

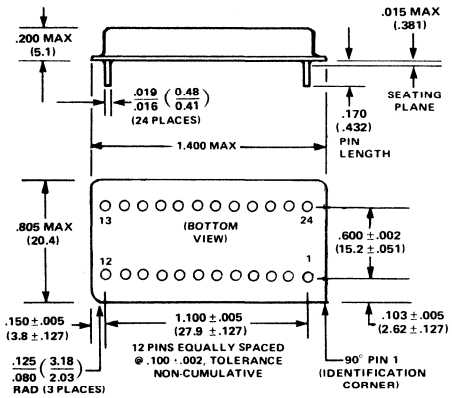
GROUNDING

Attention must be paid to proper high frequency grounding techniques in order to get the most performance from the THA-05203. It is highly desirable to use a large area ground plane under the track/hold. This will maintain a low impedance return path at all frequencies of interest. Each of the 4 ground pins on the track/hold package must be connected to ground as close to the package as possible, in order to avoid voltage differences between the ground pins.

POWER SUPPLY DECOUPLING

The THA-05203 provides internal ceramic decoupling capacitors on the +5 volt and ±15 volt power supply lines. In most applications it is desirable to add external 1μF tantalum capacitors. These decoupling capacitors should be mounted as close as possible to the hybrid package to avoid high frequency power supply line drops.

MECHANICAL OUTLINE
24 PIN DOUBLE DIP



NOTES:
1. Dimensions shown are in inches (millimeters)
2. Lead identificattion numbers are for reference only
3. Lead spacing dimensions apply at seating plane
4. Pin material meets solderability requirements MIL-STD-202E, Method 208C

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Analog Output	24	+15V Supply
2	N/C	23	Ground
3	N/C	22	−15V Supply
4	N/C	21	Ground
5	N/C	20	N/C
6	N/C	19	N/C
7	N/C	18	N/C
8	N/C	17	N/C
9	+5V Supply	16	N/C
10	Ground	15	Ground
11	Hold Command	14	N/C
12	$\overline{\text{Hold Command}}$	13	Analog Input

ORDERING INFORMATION

THA-05203−100

- Reliability Grade:
  - 1=Conforms to MIL-STD-883
  - 0=Same except preburn in test and burn in are omitted
- Operating Temperature Range:
  - 1=−55°C to +125°C
  - 3=0°C to +70°C

SECTION D

US NAVY STANDARD ELECTRONIC MODULES

HYBRID AND DISCRETE SEM PRODUCTS
JAN Qualified Modules for Navy SEM Program

FEATURES

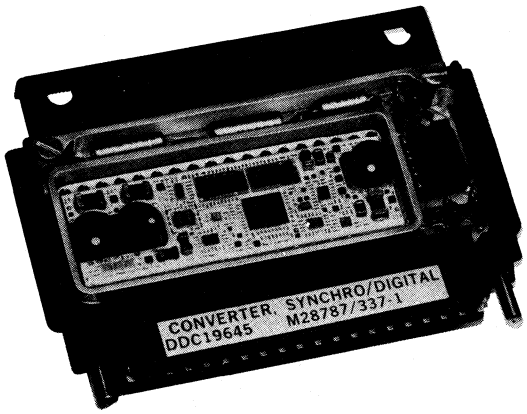
- *FACILITY CERTIFICATION BY N.W.S.C. CRANE, INDIANA*
- *MODULE QUALIFICATION— JAN AND QUALIFIED SPECIAL*
- *SPECIAL (CUSTOM) DESIGNS*
- *CAPABILITIES: S/D, D/S, A/D. D/A, DATA BUS, CUSTOM FILTERS, CUSTOM HYBRIDS*

DESCRIPTION

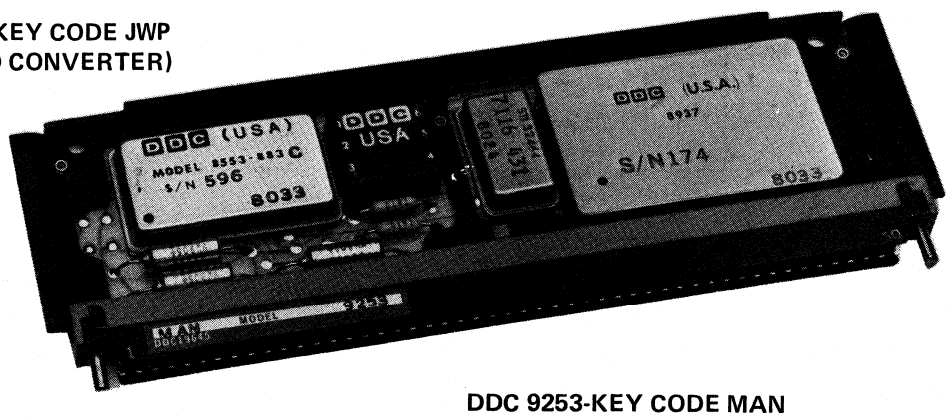
The product assurance program, facilities, and manufacturing procedures of ILC Data Device Corporation have been certified by the U.S. Navy for the production of JAN qualified modules for the Standard Electronic Module (SEM) program. Various standard DDC synchro and other data conversion products and a number of custom designed products have been adapted to SEM configuration with an assigned Key Code, as shown in the table. For these units to which an M28787 slash number has been assigned, DDC either has been JAN certified and is a QPL supplier, or is in the process of obtaining JAN certification. Consult the DDC factory for the most recent JAN certification status. Units listed in the table without M28787 numbers are some of the "special SEMs" which DDC has qualified.

DDC's proven expertise in meeting SEM program requirements, its extensive experience in the design and manufacture of data conversion products, and its sophisticated hybrid capability are available for the creation of new SEM designs. The SEM modules shown in the table are able to implement complex functions such as single and dual speed synchro-to-digital tracking converters, multiplexed synchro-to-digital converters, and digital-to-synchro converters.

The Naval Avionics Center (NAC) in Indianapolis, Indiana has prepared applications data manuals for synchro SEM modules with assigned SEM part numbers. These manuals are available to SEM users (call 317-353-3808).



DDC 9200-KEY CODE JWP
(14 BIT S/D CONVERTER)



DDC 9253-KEY CODE MAN
(MIL-STD-1553 R.T.U.)

Module Size	DDC P/N	Key Code	Function	SEM Part No. M2878/XXX	Closest DDC Standard Product
1A	9205	HUH	Two-Speed Error Crossover Switch/Detector	/225	
1A	9250	SHX	Error Detector	/189	
1A	9241	SHV	Octant/Quadrant Detector	/188	
1A	9210	SHY	MSB Function Generator	/186	
1A	9220	SHU	LSB Function Generator	/187	
1C	9202	STT	Scott-T and Reference Transformer—Input/Output	/185	H-Series
1C	9201	SES	Dual Power Amplifier	/184	and
1C	9401	KMA	Quadrant Selector and Successive Approximation Logic	NAVALEX 0104-925	HMSDC-Series
1B	9470	KMB	Synchro Input Processor—Transformer	NAVALEX 0104-926	
1B	9450	KMC	Reference Input Processor—Transformer	NAVALEX 0104-927	
1C	9271	JMB	60 Hz Input Processor—Transformer	Special	
1B	9251	JMC	60 Hz Reference Input Processor—Transformer	Special	
1A	9286	KMD	Solid State Control Transformer	Special	HXCT-14-1
1A ①	9281	KME	Solid State Control Transformer	Special	HSCT-14-H-1
1A	9288	KMF	400 Hz Error Processor	Special	HDP-4-1
1A	9289	KMG	60 Hz Error Processor	Special	HDP-6-1
1A ①	9299	KMH	400 Hz 10 bit S/D Converter	Special	HSDC-10-4H-1
1A ①	9203	KMJ	60 Hz 10 bit S/D Converter	Special	HXDC-10-6H-1
1A	9208	KMK	10 bit S/D Converter	Special	HXDC-10-4-1
1A ①	9280	KMP	Solid State Control Transformer	Special	HSCT-14-L-1
1A ①	9225	PMK	4 Channel MUX Synchro/Sine-Cos	Special	SC8711-1
1B	9204	KMR	400 Hz 14 bit R/D Converter	Special	HRCT-14-L-1-a/+ HDP-6-1
1A	9291	KMQ	400 Hz 14 bit Solid State Cosine Control Transformer	Special	HCCT-14-1
1A	9293	KMM	14 bit D/R Converter	Special	HRDC-14-1
1B	9290	HLC	60-400 Hz Scott-T and Reference Transformer	Special	Custom Product
1A	9207	HLD	10 bit S/D Converter	Special	HXDC-10-6-1
1C	9300	QQQ	12 bit A/D Converter	/232	Custom Product
1A	9900	UFU	12 bit 3 μsec A/D with Buffer (±5V Input)	Special	ADH-8516-1
1A	SEM090 00600	DRG	12 bit, 3 μsec A/D with Buffer (±10V Input)	Special	ADH-8516-1
2A ②	9253	MAN	MIL-STD-1553 BUS Adapter (R.T.U.)	Special	BUS-8553-1 +BUS-8937-1
2A	9297	CA4	Geometric A/D Converter	Special	Custom Product
1A	9200	JWP	60-400 Hz 14 bit S/D Converter with Tri-state Data	/337	Monobrid S/D
1A	SEM180 04301	NKP	60-400 Hz 14 bit R/D Converter with Tri-state Data	Special	Monobrid R/D
2A	SEM880 0601	BYK	Selectable Bandpass Filter	Special	Custom Product
2A	SEM880 0602	BYP	Selectable Bandpass Filter	Special	Custom Product
2A	SEM880 0600	BYQ	Selectable Bandpass Filter	Special	Custom Product
1A	SEM090 01603	DE7	Sonar filter	Special	Custom Product
	SEM18005-601	JAP	400 Hz 14 bit S/D converter with Tri-State Data	Special	Custom Product
	BUS 67001	UKT	MIL-STD-1553B Interface Unit	Special	Custom Product
	BUS 67002	UKU	MIL-STD-1553B Protocol and Subsystem Interface	Special	Custom Product
	BUS 67003	UKS	MIL-STD-1553 Bus Controller	Special	Custom Product

① Includes Solid State Scott-T

② Configuration is Format B (ISEM)

③ All units with MIL-M-28787 part number are presently JAN qualified or in the process of being qualified.

ORDERING INFORMATION

9205-HUH-M28787/225

- 9205 — DDC PART NUMBER
- HUH — KEY CODE
- M28787/225 — MIL PART NO. (WHERE APPLICABLE)

NOTE: FOR MODULES OTHER THAN "SPECIAL" REFER TO MIL-STD-1634 AND M28787 FOR DETAILED INFORMATION.

SECTION E

SYNCHRO AND RESOLVER TO DIGITAL CONVERTERS

SUMMARY TABLE

1. SINGLE SPEED TRACKING CONVERTERS

Name	Form Factor	Resolution	Accuracy	Features	Page
FDC-632	Encap. Module 3.1 x 2.6 x 0.4"	12 bits	±15.8 min	Complete flux valve converter with internal transformer isolation.	131
HSDC-8915	36 pin DDIP hybrid	14 bits	±4 min ±0.9 LSB	Complete 14 bit S/D converter in one hybrid package. Functional as control transformer.	133
			±2.6 min	High accuracy option "a"	
SDC-502	Encap. Module 3.1 x 2.6 x 0.8"	16 bits	±1 min	Synthesized reference, which improves quadrature rejection. Adjustment free and transformer isolated.	141
			±40 sec	High accuracy option "a"	
SDC-510/ 511	Encap. module 3.1 x 2.6 x 0.8"	3½ decades BCD	±6 min ±0.9 LSB	0.1° resolution; 0° to 359.9° unipolar or 0° to ±179.9° bipolar	145
SDC-522 or SDC-524	Encap. Module 3.1 x 2.6 x 0.8"	12 bits	±6 min ±0.9 LSB	Industry standard	147
		14 bits	±4 min ±0.9 LSB		
SDC-620	Encap. Module 3.1 x 2.6 x 0.8"	10 bits	±21 min	Low cost	150
SDC-630 or SDC-632 or SDC-634	Encap. Module 3.1 x 2.6 x 0.4"	10 bits	±21 min	Low profile, internal transformer for 400 Hz or 60 Hz	152
		12 bits	±8.5 min		
		14 bits	±4 min ±0.9 LSB	±2.6' high accuracy optional	
SDC-14510	36 pin DDIP hybrid	14 bits	±8.5 min	Small internal transformer isolated (7 rps) S/D tracking converter with 14 bit resolution and 7.5 TTL load drive capability.	156
			±5.3 min	High accuracy option	
SDC-14520	36 pin DDIP hybrid	16 bits	±5.3 min ±2.6 min. ±1.3 min	High resolution (16 bits), 1.25 rps tracking S/D converter with three accuracy options.	162
SDC-14700	Encap. Module 3.1 x 2.6 x 0.8"	5 decade	±0.05°	Synchro or resolver to BCD converter, pin programmable for all standard synchro and resolvers. Offset adjust for system zeroing. Broadband (47 Hz to 1200 Hz).	169
			±0.03°	High accuracy option.	
SDC-19000 SERIES	Encap. Module 3.1 x 2.6 x 0.4"	10 bits 12 bits 14 bits	±21 min ±8.5 min ±5.3 min.	Low cost synchro or resolver to digital converter. Available in three broadband frequency ranges. Fast tracking rates. Velocity output is standard. 12 bit units contain Major Carry and Direction output for mulit-turn and incremental applications.	173
			±2.6 min	High accuracy option	

SUMMARY TABLE

1. SINGLE SPEED TRACKING CONVERTERS (Continued)

Name	Form Factor	Features	Page
SDC-19100 SERIES	2.1 x 2.1 x 0.2"	Low cost, wide band 10, 12, 14 and 16 bit S/D and R/D hybrid converters, with a single LSI component. Accuracy is ±21, ±8.5, ±5.3, and ±2.6 minutes for the 10, 12, 14 and 16 bit units. Standard outputs include 3-state parallel data, Direction Count and DC Analog Velocity.	179

2. MULTISPEED CONVERTERS

Name	Form Factor	Features	Page
HSDC-360	Three 36 pin DDIP modules plus discrete components	A two-speed S/D or R/D tracking converter composed of two hybrid control transformers, a hybrid data processor, plus discrete components. Resolution is 16 bits and accuracy is ±0.41 minutes for a 36:1 speed ratio.	187
SDC-361/2	Single module 3.1 x 2.6 x 0.8"	2 speed S/D or R/D converter with internal isolation transformers. Resolution is 16 bits and accuracy is ±20 sec.	192

3. MULTIPLEXED CONVERTERS

Name	Form Feature	Features	Page
HMSDC-8700 or MSDC-700	36 pin DDIP hybrid Encap. Module 3.1 x 2.6 x 0.4"	Two hybrid or discrete modules consisting of one input processor module (containing four input channels) and one central converter module. More than one input processor may be used to multiplex additional channels. Binary output with an accuracy of ±5.3 minutes and a resolution of 14 bits.	196
DDC-6509	Rolm 1602 P.C. Card	Multi-channel S/D and R/D converter board, with highly accurate DDC Model HSDC-8915 Monobrid Series Converters. Configured for compatibility with AN/UYK Nova computer. Provides 8 channels of conversion and capability to handle 8 seperate reference inputs.	203

ADDENDUM*

RDC-1919X Series	2 x 2 x 0.2" hybrid	10-16 bit, resolution resolver (sine and cosine) to digital converter with ±21 to ±1.3 minute accuracy. Features velocity output with 1% linearity, which eliminates the need for electromechanical tachometers in most applications. Operates with full accuracy and linearity at 0°C to +70°C.	—

*This product was introduced after the catalog printing deadline. Consult factory for data sheets.

BACKGROUND INFORMATION

INTRODUCTION

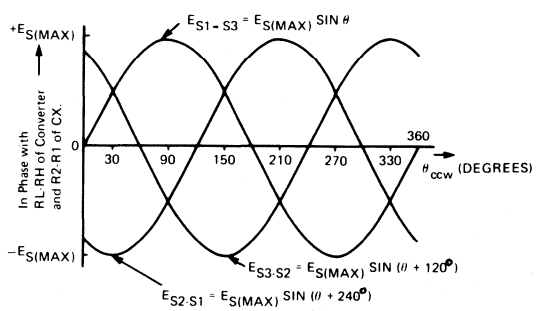
DDC's synchro-to-digital and resolver-to-digital converters employ the latest in component and circuit technology and represent a significant improvement in performance and reliability over former units.

From a systems engineer's standpoint, outstanding performance features have been incorporated into these units. They are designed for printed circuit board mounting by hand soldering or flow soldering techniques. Each unit is fully trimmed and tested before leaving the factory. DDC builds hundreds of synchro converters each month, making shipments from stock a common occurrence.

THEORY OF OPERATION

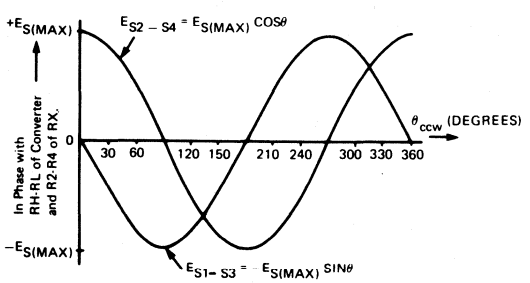
Theory of operation is explained for DDC's discrete and hybrid tracking synchro-to-digital converters. The same principles apply to the resolver-to-digital converters except that the angular analog data input is in 4-wire resolver form rather than 3-wire synchro. Synchro or resolver angle data is proportional to the ratio of line-to-line amplitudes across the terminals. These line-to-line amplitudes vary as the shaft angle is changed. The angle information is converted from synchro format, (see Figure 1A), i.e., Sin θ cos ωt, sin $(\theta + 120^\circ)$ cos ωt, sin $(\theta + 240^\circ)$ cos ωt, to resolver format, (see Figure 1B), i.e., sin θ cos ωt and cos θ cos ωt, by the Scott "T" Transformer,

(A)



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ)

(B)



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 1. SYNCHRO AND RESOLVER SIGNALS

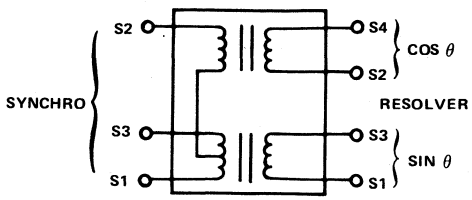
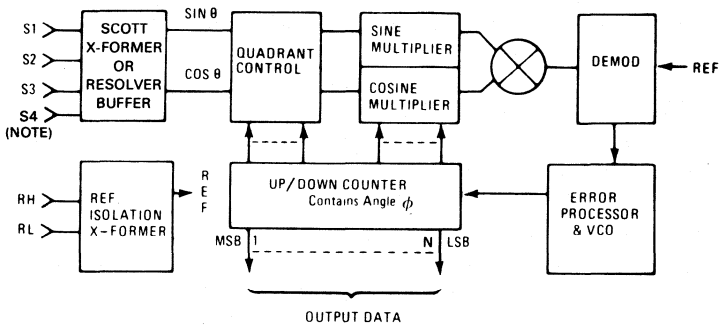


FIGURE 2. SCOTT "T" TRANSFORMER



Note: Use S1, S2, S3 and S4 for resolver inputs, or S1, S2 and S3 only for synchro inputs.

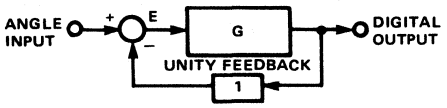
FIGURE 3. BLOCK DIAGRAM SYNCHRO-DIGITAL CONVERTER

shown in Figure 2. In a synchro transmitter, RH-RL corresponds to R1-R2, and in a resolver RH-RL corresponds to R2-R4. Note that all converters use resolver format internally. The carrier, cos ωt, is of minor importance to this discussion and will be dropped from the notations hereafter. As shown in the block diagram of Figure 3, the converter performs the following trigonometric computation:

$$\text{Sin}\,(\theta - \phi) = (\text{Sin}\,\theta \cos\phi - \cos\theta \sin\phi).$$

In this expression, θ represents the input data angle and ϕ represents the angle contained in the up-down binary counter. The error function, sin $(\theta - \phi)$, is processed and controls the up-down counter in such a manner that at null, $\theta = \phi$. The converter includes a dual integration, making it a Type II servo loop and hysteresis function to eliminate the one or two bits of "hunting" otherwise present in a Type II servo loop. Prior to the counter being updated due to an input data change, a "converter busy" signal is generated. When it returns to normal, the data may be frozen by activating the "inhibit" control line and transferring the data simultaneously. It is important to realize that one advantage of a tracking converter is that the output data is always fresh and always available. There are no errors due to velocity lags or minor varitions in synchro carrier amplitudes or power supply voltage.

The loop dynamics of DDC's tracking S/D converters are described by the unity feedback configuration shown in Figure 4. The closed-loop transient response is nominally critically damped, and the parameters A and B for each S/D converter can be requested from the applications engineering group at DDC if they are not listed in the product section of this catalog.



$$G = \frac{A^2\left(\frac{S}{B} + 1\right)}{S^2\left(\frac{S}{10B} + 1\right)}$$

FIGURE 4. S/D CONVERTER LOOP DYNAMICS

APPLICATIONS

For all of DDC's synchro converters, the input synchro signals are connected to S1, S2 and S3. Input resolver signals are connected to S1, S2, S3, and S4. The conventions are shown in Figure 5. These signals are applied to an input Scott "T" transformer or a resolver isolation transformer. Application of DC voltages, or AC voltages other than those intended, may damage this transformer. The same is true with regard to the reference signal applied to RH and RL. Also, careful attention must be given to making the proper electrical connections. Reversal or misapplication of power supplies can result in damage to the converter.

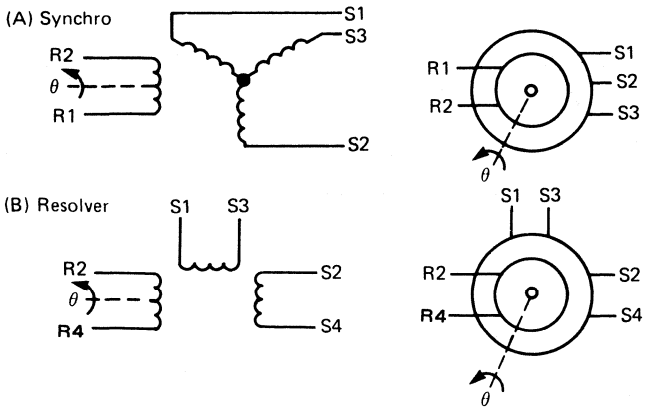


FIGURE 5. SYNCHRO AND RESOLVER CONVENTIONS

MULTIPLEXED S/D CONVERTER SYSTEMS

Multiplexed S/D converter systems differ from tracking type converters for two reasons: they have multiple inputs rather than one, and they use a successive approximation conversion technique rather than a Type II tracking loop. The heart of the system is the central converter, which consists of one or more modules. Added to this are input circuits for each channel which transform the synchro information to resolver format. The reference carrier is monitored and when a peak is detected the sin and cos (resolver) levels of all channels are sampled and held as DC information. One channel is now selected and the central converter is started. A successive approximation technique is used by the central converter to determine the status of each digital bit, one at a time, starting with the most significant bit (MSB) and ending with the least significant bit (LSB).

The central converter uses a solid state control transformer whose inputs are θ (the analog input angle) and ϕ (the digital angle in the output register). The output from the solid state CT is sin $(\theta - \phi)$, the same form as an electromechanical CT. The converter operates on this signal to reduce it to a minimum, thus making θ equal to ϕ. Since only n trials are needed to resolve 2^n different levels, relatively fast S/D conversions can be made in this fashion.

MULTISPEED S/D CONVERSION

The operation of a two speed S/D is essentially the same as a single speed tracking S/D, except there are two solid state CTs generating two error voltages. These two CTs are driven from a single up/down counter. One CT is referred to as the coarse CT and the other is called the fine CT. Digital information from the counter to the fine CT is multiplied by the speed ratio between the two (for example, 36X). A cross-over switch selects which CT error signal is fed to the error processor. Assuming an off-null condition, the cross-over switch feeds the coarse CT error to the error processor. The converter seeks a null in the same manner described for a single speed S/D. As a null is approached, the coarse CT error voltage drops below a preset limit and the cross-over switch automatically switches over to the fine CT error voltage to feed into the error processor. Since the counter angle θ is multiplied by the speed ratio, the gradient of the fine CT error voltage is multiplied by the same amount. The tracking loop is now able to seek an even finer null, using the fine error voltage, and will switch back to the coarse error voltage only if the preset theshold is exceeded. In order to eliminate false nulls 180 degrees away from the true null, a digital offset and a "stickoff" voltage are introduced in the coarse channel.

ACCURACY TESTS

Because of the high accuracy of DDC's S/D converters, only laboratory-grade synchro or resolver substitution boxes or standards should be used. If synchro standards are not available, arrangements may be made to witness the final source inspection at the DDC factory.

Bit	Deg/Bit	Min/Bit
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14 LSB	0.0220	1.32

FIGURE 6. BIT WEIGHT TABLE

Figure 7 shows how to arrange test equipment for measuring the accuracy of S/D converters. A separate lamp driver or suitable readout is required for each of the output data lines. The synchro standard is set to any desired test angle, and the lamps which are on are added according to their bit weights (see Figure 6) and compared with the test angle.

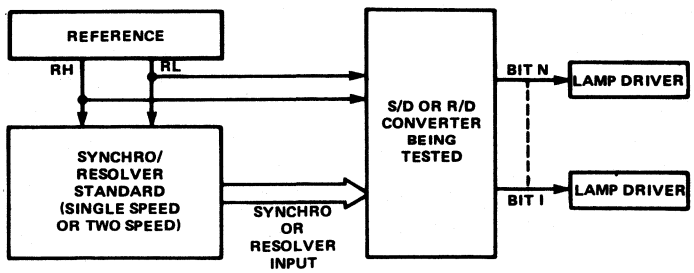


FIGURE 7. ACCURACY TEST CIRCUIT

PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc. Appropriate handling procedures should be used in order to prevent damage to CMOS circuits.

It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a pin connection by ripping out the plated through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.

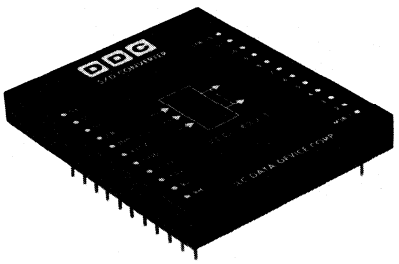
APPLICATION NOTES

The following application notes are available, upon request:

- CONSIDER BASIC PARAMETERS WHEN CHOOSING S/D CONVERTERS
- CHOOSING THE RIGHT ENCODER SIMPLIFIES MOTION CONTROL
- SYNCHRO & MICROPROCESSOR COMBINE FOR VERSATILE MULTI-TURN POSITION SENSING
- MEASURING THE POSITION OF MECHANICAL SHAFTS
- RESOLVER-BASED POSITION ENCODERS SATISFY DEMAND OF ROBOTICS

FDC-632

FLUX VALVE TO DIGITAL CONVERTER



FEATURES

- *12 BIT RESOLUTION*
- *ACCURACY TO ± 15.8 ARC MINUTES*
- *INTERNAL TRANSFORMER ISOLATION*
- *TTL COMPATIBLE LOGIC*
- *MEETS MIL-STD-202E REQUIREMENTS*

DESCRIPTION AND APPLICATIONS

The FDC-632 is a flux valve to digital converter, with 12 bit resolution and accuracy to ±15.8 arc minutes. Incorporating many dynamic characteristics designed into our standard SDC-632 Synchro to Digital Tracking Converter, this flux valve unit is packaged in a 3.1 X 2.6 X 0.4 inch encapsulated module. Conversion of the flux valve output signals of 50 to 200 mV @ 800 Hz requires an external reference frequency doubler circuit. The doubler circuit doubles the frequency of the 26V @ 400 Hz reference input and faciliates demodulation of the signal input within the converter, (see Figure 1).

The FDC-632 applies a unique control transformer algorithm that provides inherently higher accuracy and jitter free output. Utilizing a type II servo loop, the FDC-632 has no velocity lag up to the specified tracking rate (see Figure 2). Each unit is fully trimmed and requires no adjustments or calibrations in the field.

Flux valves are most commonly used in magnetic bearing devices aboard ships and aircraft, where accuracy within one-half degree is required.

SPECIFICATIONS

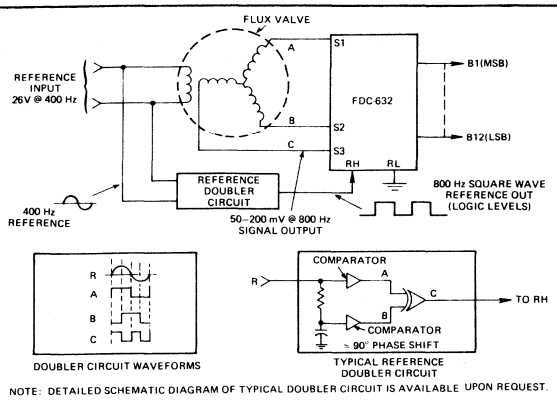
Apply over temperature range, power supply range, reference frequency and amplitude range, ± 10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	12 Bits
ACCURACY (WORST CASE)	± 15.8 Minutes
SIGNAL AND REFERENCE INPUT	
Flux Valve Synchro Input*	
Signal Frequency	800 Hz ± 10%
Signal Input Impedance	1 kΩ (min) (L-L Balanced, Resistive)
Signal Input Voltage Range	50 to 200 mV (L-L Input Level)
Reference Input*	
Reference Input Frequency	800 Hz
Reference Input Impedance	8 kΩ (Resistive)
Reference Input Voltage Range	1 to 5 V rms
*Transformer Isolated	
Note: The 800 Hz square wave reference input is derived from 400 Hz Flux Valve excitation through a user supplied doubler circuit (see figure 1.).	
DIGITAL INPUT/OUTPUT	
Logic type	TTL
Inhibit Input (INH) Loading	Logic "O" inhibits 0.2 Std. TTL loads plus 18 kΩ min pull-up resistor to + 5 V supply
Outputs	
Type	Low power Schottky (can drive remote loads)
12 Parallel Data Bits	Natural binary angle; positive logic
Converter Busy (CB)	0.5 to 1.5 μsec positive pulse. Data changes on leading edge
Drive Capability	2 Std. TTL loads (5 Std. load capability available on special order; consult factory)

PARAMETER	VALUE
DYNAMIC CHARACTERISTICS	
Input Rate for Full Accuracy	0 to 10 rps (min); 15 rps (typ)
Acceleration for 1 LSB Lag	295°/sec² (typ)
Settling Time	
For Normal Tracking (Up to Specified Input Rate)	No lag error
For 179° Step Change	
Settling to 1 LSB	300 msec (typ)
Settling to Final Value	360 msec (typ)
Velocity Constant (Type II Servo Loop)	$K_V = \infty$
Acceleration Constant	K_a = 3,600 sec² (nom)

POWER SUPPLIES	+15 V Supply	−15 V Supply	+5 V Logic Supply
Normal Voltage	+11 to −16.5 V	−11 to −16.5 V	+4.5 to +5.5 V
Voltage Range	+18 V	−18 V	+7 V
Max Voltage Without Damage	4 mA (typ)	18 mA (typ)	80 mA (typ)
Current	6 mA (max)	30 mA (max)	120 mA (max)

TEMPERATURE RANGES	
Operating	
−1 Option	−55°C to +105°C
−3 Option	0°C to +70°C
Storage	−55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size (Encapsulated Module)	3.125 X 2.625 X 0.43 inch (79.37 X 66.67 X 10.92 mm)
Weight	4 oz (113 g)



NOTE: DETAILED SCHEMATIC DIAGRAM OF TYPICAL DOUBLER CIRCUIT IS AVAILABLE UPON REQUEST.

FIGURE 1. CONNECTION DIAGRAM

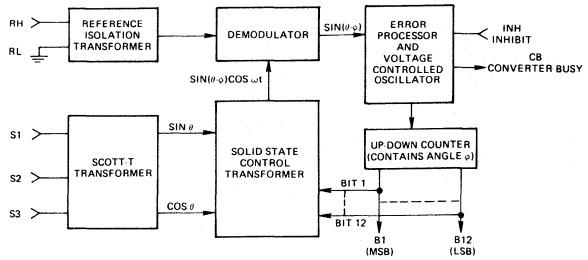


FIGURE 2. BLOCK DIAGRAM

TECHNICAL INFORMATION

TIMING

Figure 3, below, shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy pulse (CB). The CB is a positive pulse 0.5 to 1.5 μsec long. Data changes on the leading edge of the CB pulse, and data can be transferred 0.5 μsec after the leading edge.

The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the inhibit is applied. The converter will ignore an inhibit applied during the "busy" interval until that interval is over. Timing is as follows: (a) apply the inhibit, (b) wait 0.5 μs, (c) transfer the data, and (d) release the inhibit. Extra CB pulses will not occur if the input angle changes while the counter is locked by the INH.

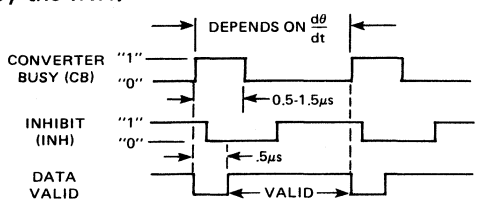


FIGURE 3. TIMING DIAGRAM

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltages are not the ± 15 VDC nominal values, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage. The + 15 V supply voltage will determine the positive maximum velocity, and the −15 V supply voltage will determine the negative maximum velocity.

So long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. Figure 4 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.

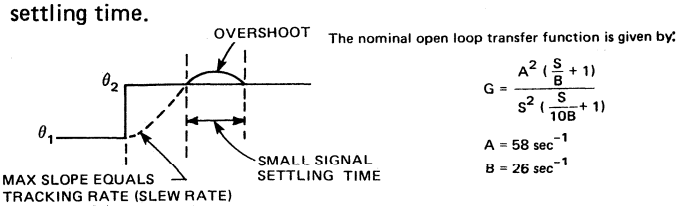
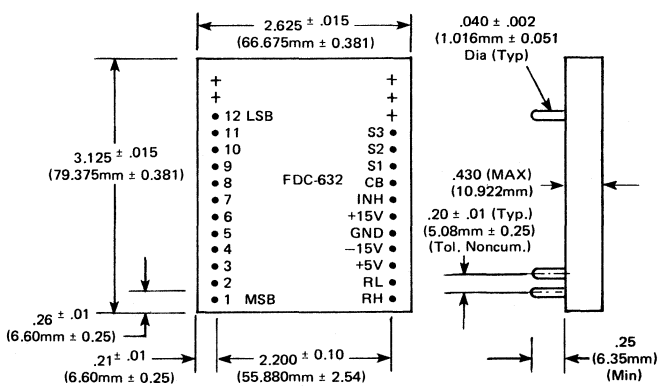


FIGURE 4. RESPONSE TO A STEP INPUT

TRANSFORMER INPUT

To prevent damage to the input transformers, the maximum steady state voltage should not exceed the specified input voltage by more than 30%. The maximum common mode voltage (DC plus recurrent AC peak) should not exceed 500 V.

MECHANICAL OUTLINE



Notes:
1. Pin material is electrosoldered brass per MIL-F-14072, M222
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.

ORDERING INFORMATION

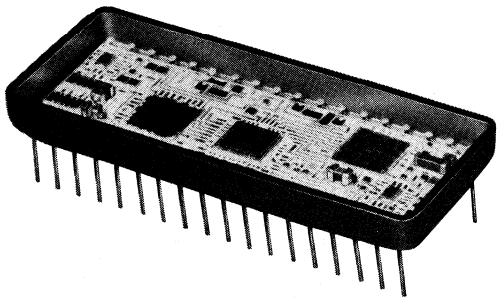
FDC – 632– 1

Temperature Range:
1 = −55°C to +105°C
3 = 0°C to +70°C

Input Type:
FDC = Flux Valve

HSDC-8915 MONOBRID® SERIES*

14 BIT MONOLITHIC HYBRID S/D AND R/D TRACKING CONVERTERS



DESCRIPTION

The HSDC-8915 Monobrid® Series is the first complete 14-bit synchro-to-digital or resolver-to-digital converter contained in a single hybrid module. Most of its circuitry has been incorporated into a custom designed monolithic chip, thereby greatly reducing parts count inside the hybrid. The Monobrid combination of monolithic and hybrid technologies allows a more sophisticated design with better performance and additional features to fit inside a standard 36 pin DDIP hybrid package. Power consumption is reduced, reliability is increased, and costs are lower.

New features found in the HSDC-8915 Series are 3-state output in two bytes, and a transparent latch which allows the converter to keep tracking even while an Inhibit is being applied. Innovative features found in other recent DDC hybrid converters are also included, such as a ±2.6 minute high accuracy option, analog velocity signal, error voltage outputs, solid state signal and reference isolation, broadband input, and accommodation to non-standard line-to-line voltage levels.

The HSDC-8915 Series is available in two accuracy grades: ±4 minutes ±0.9 LSB and ±2.6 minutes. The accuracy is not affected by carrier amplitude variation because the conversion is ratiometric. Phase sensitive detection in the error loop rejects quadrature and noise. Adjustments and calibration are never required.

The HSDC-8915 Series accepts broadband inputs: 360 to 1000 Hz or 47 to 1000 Hz. Two kinds of input signal isolation are available: internal differential solid state input with high common mode rejection, and transformer isolation with external transformers. Output angle is natural binary code, parallel positive logic, and TTL/CMOS compatible. Synchronization to a computer is complete via a Converter Busy output and an Inhibit input.

Only one main power supply is required. Its +15V DC nominal level can range from +11 to +16.5 volts with no degradation in performance. The HSDC-8915 is also connected to the external logic power supply. Internal logic is CMOS, and all logic inputs and outputs are buffered to the external logic level. TTL or any external CMOS logic level between +4.5V and the +15V supply level can be accommodated.

APPLICATIONS

With three-state output and an Inhibit that does not stop the tracking process, HSDC-8915 Series converters are especially suited for bus multiplexing and interfacing with microprocessors. These converters are ideal for remotely located and hard to access equipment where low power requirements, small size, and high MTBF are critical. All units are processed to MIL-STD-883. They are well suited to the most stringent and severe industrial or military and avionics applications. In conjunction with other devices, they are easily adapted for closed loop control.

Designed for printed circuit board mounting by standard techniques, the HSDC-8915 Series can be readily incorporated into other equipment by the OEM user. Because of their low cost, they are competitive with discrete S/D converters in many applications.

FEATURES

- *10 RPS TRACKING*
- *LOW POWER:*
  150 mW, Typical
- *ACCURACY:*
  ±4 minutes ±0.9 LSB standard
  ±2.6 minutes high accuracy option
- *3-STATE LATCHED OUTPUTS FOR MICROPROCESSOR DATA BUS*
- *USABLE AS CONTROL TRANSFORMER (CT)*
- *INHIBIT DOES NOT INTERRUPT TRACKING*
- *LOGIC:*
  TTL and CMOS compatible 14 bit parallel binary angle
  Converter Busy and Inhibit
  Enable lines for 3-state output

*Patented

Note: Monobrid® is a registered trademark of ILC Data Device Corporation.

HSDC 8915 MONOBRID SERIES SPECIFICATIONS

Over reference amplitude, temperature, and power supply ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY	
Normal Accuracy	±5.3 minutes ±0.9 LSB
High Accuracy Option "a"	±2.6 minutes max (total error)
REFERENCE INPUT	
Carrier Frequency Ranges	
Nominal 400 Hz Units	360 – 1000 Hz
Nominal 60 Hz Units	47 – 1000 Hz
Reference Input Characteristics	
Voltage Range	4 – 130V rms
Input Impedance	250 KΩ min, single ended 500 KΩ min, differential
Common Mode Range	DC common mode plus recurrent AC peak = 210V max
SYNCHRO/RESOLVER SIGNAL INPUTS	
SOLID STATE BUFFER INPUT MODULES	
Minimum Input Impedance (Balanced)	

	Z_{IN} Line to Line	Z_{IN} Each Line to GND
Synchro		
90V L-L (8918, 8919)	130 KΩ	85 KΩ
11.8V L-L (8917)	17.5 KΩ	11.5 KΩ

	Z_{IN} Single Ended	Z_{IN} Differential	Z_{IN} Each Line to GND
Resolver			
90V L-L (8922)	175 KΩ	350 KΩ	175 KΩ
26V L-L (8921)	50 KΩ	100 KΩ	50 KΩ
11.8V L-L (8920)	23 KΩ	46 KΩ	23 KΩ

Common Mode Ranges		
For 90V L-L Input	182V Max	DC common mode plus recurrent AC peak
For 26V L-L Input	60V Max	
For 11.8V L-L Input	60V Max	

VOLTAGE FOLLOWER BUFFER INPUT MODULES	
(For External Transformers)	
Input Signal Type	Sin and cos resolver signals referenced to converter internal reference V (not to external GND)
Sin/Cos Voltage Range	1V nominal, 1.15V max
Max Voltage Without Damage	15V rms continuous; 100V peak transient
Input Impedance	Z_{IN} > 10 MΩ (transient protected voltage follower)
TRANSFORMER CHARACTERISTICS	
(See Ordering Information for List of Transformers. Reference Transformers are Optional for Both Solid State and Voltage Follower Input Options.)	
400 Hz TRANSFORMERS	
Reference Transformer	
Carrier Frequency Range	360 – 1000 Hz
Voltage Range	18 – 130V
Input Impedance	40 KΩ min
Breakdown Voltage to GND	1200V peak
Signal Transformer	
Carrier Frequency Range	360 – 1000 Hz
Breakdown Voltage to GND	700V peak
Minimum Input Impedances (Balanced)	

	Synchro Z_{IN} (Z_{SO})	Resolver Z_{IN}
90V L-L (Option 4H)	180 KΩ	100 KΩ
26V L-L (Option 4M)	–	30 KΩ
11.8V L-L (Option 4L)	20 KΩ	30 KΩ

60 Hz TRANSFORMERS	
Reference Transformer	
Carrier Frequency Range	47 – 440 Hz
Input Voltage Range	80 – 138V rms; 115V rms nominal
Input Impedance	600 KΩ min, resistive
Input Common Mode Voltage	500V rms, transformer isolated
Output Description	+R (in phase with RH-RL) and -R (in phase with RL-RH) derived from op-amps. Short circuit proof.
Output Voltage	3.0V nominal riding on ground reference V. Output voltage level tracks input level.
Power Required	4 mA typ, 7 mA max from + 15V supply.

PARAMETER	VALUE
Signal Transformer	
Carrier Frequency Range	47 – 440 Hz
Input Voltage Range	10 – 100V rms L-L; 90V rms L-L nominal
Input Impedance	148 KΩ min L-L balanced resistive
Input Common Mode Voltage	±500V rms, transformer isolated
Output Description	Resolver output, – sine (–S) and + cosine (+C) derived from op-amps. Short circuit proof.
Output Voltage	1.0V rms nominal riding on ground reference V. Output voltage level tracks input level.
Power Required	4 mA typ, 7 mA max from +15V supply
DIGITAL INPUT/OUTPUT	
Logic Type	TTL/CMOS compatible, depending on logic supply voltage
Outputs	
14 Parallel Data Bits	Natural binary angle; positive logic
Converter Busy (CB)	0.5 –2.0 μs positive pulse; leading edge initiates counter update
Drive Capability	1 Standard TTL load. 1.6 mA at 0.4 V_{max} (logic "0"). 10 Standard TTL loads, 0.4 mA at 2.8 V (logic "1"). 10 μA_{max} (high impedance).
Input:	Z_{IN} ≥ 25 KΩ pull up resistor to V_L
Inhibit Input (INH)	INH – Logic 0 inhibits
Enable, Bits 1 to 6 (EN 1-6)	(EN 1-6) and (EN 7-14) – Logic 0 enables
Enable, Bits 7 to 14 (EN 7-14)	Logic 1 high impedance
$\overline{S}$ (Control Transformer)	Logic 0 for use as CT
Logic Type	CMOS Compatible – Logic "0" ≤ 0.3V_L "1" ≥ 0.7V_L
Accuracy	±4 minutes
Loading	CMOS
ANALOG OUTPUTS	
Filtered DC Error Voltage (E)	–1 VDC per +LSB of error (±3 LSB range)
DC Velocity Voltage ($\dot{\theta}$)	+1 VDC per +2.1 rps at 400 Hz +1 VDC per +0.54 rps at 60 Hz
AC Error Voltage Near Null (e)	16 mV rms for +1 LSB of error (nominal input voltage
Loading	1.0 mA)
DYNAMIC CHARACTERISTICS	
Input Rate	
At 400 Hz	0 to ±10 rps min
At 60 Hz	0 to ±2.5 rps min
Velocity Constant	$K_V = \infty$ (No limitation with Type II servo loop)
Acceleration Constant	
At 400 Hz	K_a = 65,000 sec^{-2} nominal
At 60 Hz	K_a = 1000 sec^{-2} nominal
Settling Time	
For 179° Step Change	
At 400 Hz	150 ms typ to 1 LSB 200 ms max to final value
At 60 Hz	350 ms typ to 1 LSB 400 ms max to final value
TEMPERATURE RANGES	
Operating	
–1 option	–55°C to +125°C
–3 option	0°C to +70°C
Storage	–55°C to +135°C
POWER SUPPLIES	

	±15 VDC	Logic Supply
Nominal Voltage		
Voltage Range	+11 to +16.5V	+4.5V to +15 supply
Absolute Max Voltage	+18V	+18V
Current or Impedance	15 mA max*	Z_{IN} = 5 KΩ min

*Does not include current required by 60 Hz active transformers.

PHYSICAL CHARACTERISTICS	
Converter	
Type	36 pin double DIP
Size	0.78 x 1.9 x 0.21 inch (2.0 x 4.8 x 0.53 cm)
Weight	1 oz max (28 g)
400 Hz Transformer	
Type	Encapsulated module. Signal input uses 2 modules (T1A and T1B). Ref uses 1 module (T2).
Size	0.8 x 0.6 x 0.3 inch (2 x 1.5 x 0.8 cm)
Weight	0.4 oz max (11 g)
60 Hz Transformer	
Type	Encapsulated module. Signal transformer and reference transformer each consist of one such module.
Size	1.125 x 1.125 x 0.42 inch (2.86 x 2.86 x 1.07 cm)
Weight	0.7 oz max (20 g)

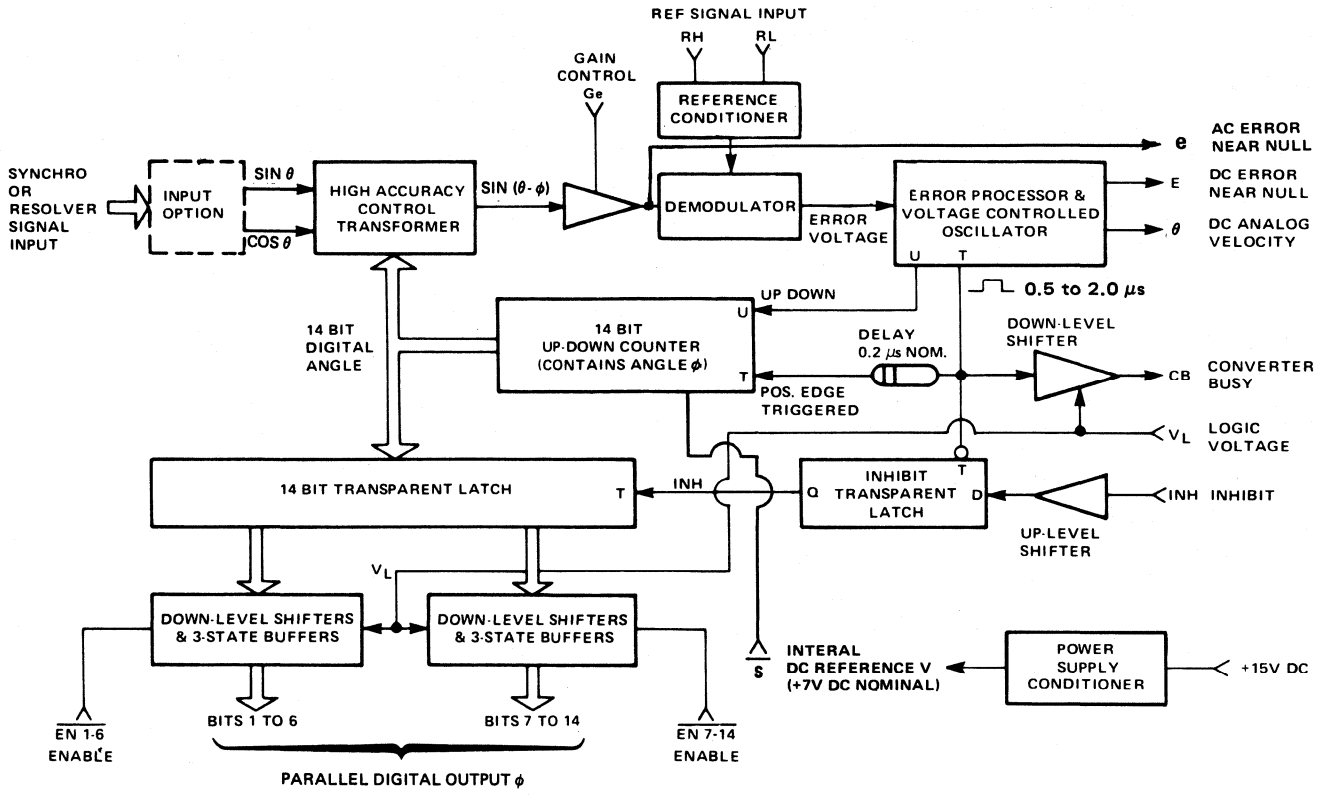


FIGURE 1. HSDC-8915 SERIES BLOCK DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION

The circuit shown in the HSDC-8915 block diagram, Figure 1, consists of three main parts: the signal input option; a feedback loop whose elements are the control transformer, demodulator, error processor, and up-down counter; and digital interface circuitry including various latches and buffers.

The input options accept a synchro or resolver input and produce a resolver type output for the control transformer. The first two options, called solid state synchro and resolver input, accept synchro and resolver signal inputs directly, and provide signal isolation; it is a voltage follower buffer and requires an external signal conditioner such as a transformer. Both options, the solid state input and the external transformer isolated buffer, are available for the following standard inputs:

All input options are DC coupled with broadband characteristics up to 1000 Hz. HSDC-8915 Series converters are usable to 10 KHz with slight degradation in accuracy – consult factory for further information.

In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The internal converter operates with signals in resolver format, sin θ cos ωt and cos θ cos ωt. Synchro signals are of the form sin θ cos ωt, sin $(\theta + 120^\circ)$ cos ωt, and sin $(\theta + 240^\circ)$ cos ωt. Diagrams on the following page show synchro and resolver signals as a function of the angle θ.

The feedback loop produces a 14 bit digital angle Φ which tracks the analog input angle θ to within the specified accuracy of the converter. The control transformer performs the following trigonometric computation:

$$\sin(\theta - \Phi) = \sin\theta \cos\Phi - \cos\theta \sin\Phi$$

where θ is the angle representing the synchro or resolver shaft position, and Φ is the digital angle contained in the up-down counter in the converter. The tracking process consists of continually adjusting Φ to make $(\theta - \Phi) \rightarrow 0$, so that Φ will represent the shaft position θ.

The output of the demodulator is an analog DC level proportional to sin $(\theta - \Phi)$. The error processor integrates this sin $(\theta - \Phi)$ error signal, and the output of the integrator is used to control the frequency of a voltage controlled oscillator. This oscillator produces "clock" pulses which are accumulated by the up-down counter. The up-down counter is functionally an incremental integrator. Therefore there are two stages of integration, making the converter a Type II tracking servo. In a Type II servo, the voltage controlled oscillator always settles to a counting rate which makes $d\Phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available so long as the maximum tracking rate of the converter is not exceeded.

The digital interface circuitry has three main functions: to latch the output bits during an Inhibit command so that stable data can be read out, to furnish both 14 bit parallel and 3-state data formats, and to act as a buffer between the internal CMOS logic and the external logic level.

continuous tracking of the feedback loop. This is a new feature, since S/D and R/D converters usually lock the up-down counter while an Inhibit is applied. In the HSDC 8915 Series Monobrids, therefore, the digital angle Φ is always updated and the Inhibit can be applied for an arbitrary amount of time. The Inhibit transparent latch and the 0.2 μs delay are also parts of the Inhibit circuitry, whose detailed operation is described in the Logic Output/Input Section.

When testing or evaluating the converter, it is advisable to limit the power supply currents as follows:

+15V Supply Limit at 20 mA.
Logic Supply V_L at 2 mA + Digital Load at Logic 1.

Analog circuits inside the 8915 module are referenced to an internal DC reference level V which rides at +7V nominal with respect to the external ground (GND). V should not be connected to the external ground.

VOLTAGE FOLLOWER BUFFER INPUT

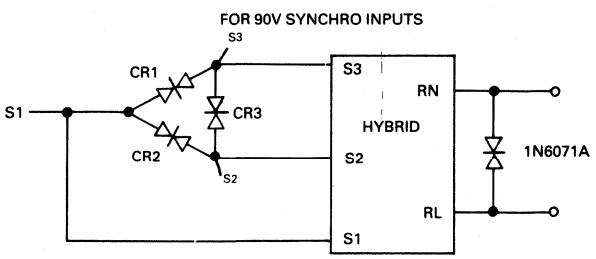
Voltage follower buffer units require a signal isolation transformer or a similar signal conditioner that provides a 1.0V rms nominal resolver type signal referenced to the internal DC level V. This input option may be preferred in applications where the signal conditioner can be integrated with other components, as in many multiplexed systems.

SOLID STATE BUFFER INPUTS

The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection, so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed the following values:

Input	Common Mode Maximum	Max Transient Peak Voltage
11.8V L-L	60V Peak	150V
26 V L-L	60V Peak	150V
90 V L-L	182V Peak	500V
Reference	210V Peak	1000V

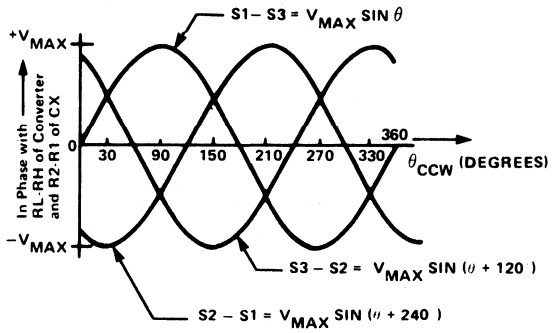
90 V line-to-line systems may have voltage transients which exceed the 500V specification listed above. These transients can destroy the thin film input resistor network in the hybrid. Therefore, 90V L-L solid state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro or resolver voltages are switched on or off. For instance, a 1000V transient can be generated when the



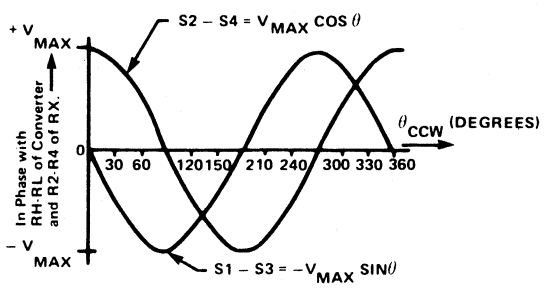
CR1, CR2 and CR3 are 1N6068A, 100V bipolar transient voltage suppressors or equivalent.

Non-standard synchro and resolver voltage levels can be accommodated with no degradation in the specifications. A unit should be selected whose voltage level 11.8V, 26V, or 90V is the next higher standard level above that of the non-standard signal. To correct the error gradient, a resistor R of the following value in ohms must be added between pins Ge and V:

$$R = \frac{1000}{A-1} \quad \text{where } A = \frac{\text{Standard Signal Voltage}}{\text{Non-Standard Signal Voltage}}$$



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

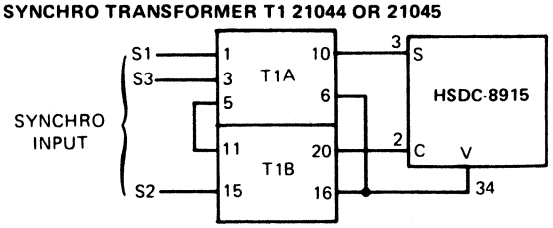
SYNCHRO AND RESOLVER SIGNALS

TRANSFORMERS

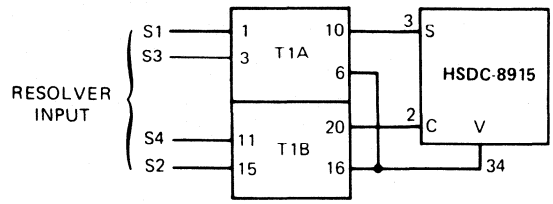
Transformer connection diagrams are shown in Figure 2. These transformers are designed for the voltage follower buffer input options HSDC 8915 and HSDC 8916. However, the reference transformers may also be used with the solid state buffer input options.

Note that the 60Hz transformers are active transformers. They have op-amp outputs and require connections to the +15V power supply as shown in Figure 2. Active devices are provided because passive transformers require considerably more volume at 60 Hz than at 400 Hz.

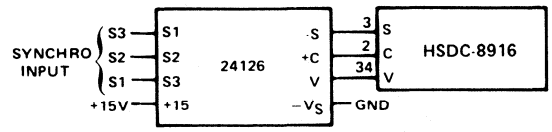
400 Hz SYNCHRO TRANSFORMER T1 21044 OR 21045



400Hz RESOLVER TRANSFORMER T1 21046 OR 21047 OR 21048

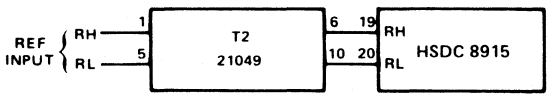


60 Hz SYNCHRO TRANSFORMER 24126



Note: Synchro inputs must be connected as shown for +sine and −cosine.

400 Hz REF TRANSFORMER 21049



60 Hz REF TRANSFORMER 24133

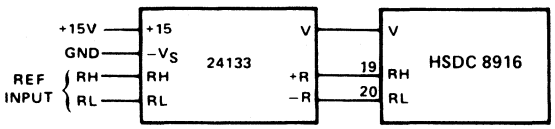
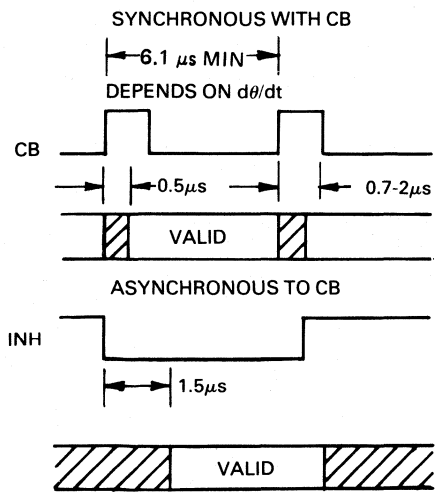


FIGURE 2 TRANSFORMER CONNECTION DIAGRAM

LOGIC OUTPUTS AND INPUTS

CAUTION: Appropriate handling procedures should be used to prevent damages to CMOS circuits.

Logic outputs consist of 14 parallel data bits and a Converter Busy (CB). All logic outputs are short-circuit proof to ground and to positive voltages as high as V_L. The CB output is a positive 0.5-2.0 μs pulse, and data changes about 0.2μs after the leading edge of the pulse because of an internal delay (see Figure 1). Data is valid 0.5μs after the leading edge of a CB. If the converter is operated with fewer than 14 bits, the unused LSB bits should be left unconnected.



TIMING DIAGRAM AT 10 RPS

The parallel digital outputs are gated to provide an 8 and a 6 line byte for microprocessor bus interfacing. When the Enables for the gates are at logic 0, the gate outputs are at normal logic 1 or 0, depending on the bit state. When the Enables are at logic 1, the gate outputs are high impedance and the microprocessor sees an essentially open line. Outputs are valid 0.5μs after an Enable is driven to logic 0. For 14 bit parallel output operation when the 3-state feature is not used, the Enable lines should be tied to logic 0.

The Inhibit (INH) logic input locks the 14 bit transparent latch so that the bits will remain stable while data is being transferred (see Figure 1). The output is stable 0.5μs after the Inhibit is driven to logic 0. A logic 0 at the T input locks the 14 bit latch, and a logic 1 allows the bits to change. The purpose of the INH transparent latch is to prevent the transmission of invalid data when there is an overlap between the CB and INH. While the counter is not being updated the CB is at logic 0 and the INH latch is transparent. When the CB goes to logic 1 the INH latch is locked. If a CB occurs after an INH has been applied, the 14 bit latch will remain locked and its data cannot change until the CB returns to logic 0. If an INH is applied during a CB pulse, the 14 bit latch will not lock until the CB pulse is over. The purpose of the 0.2μs delay is to prevent a race condition between the CB and the INH in which the up-down counter begins to change just as an INH is applied.

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. The output data change is initiated by the leading edge of the CB pulse, delayed by the 0.2μs (nominal) delay. The output becomes stable in less than 0.5μs even though the CB pulse may last longer. Data transfer can be made synchronous with the leading edge of CB, delayed by 0.5μs. (See Timing Diagram.)

An Inhibit input, regardless of its duration, does not affect converter update. A simple method of interfacing to a computer, asynchronous to CB pulse, is to (a) apply the inhibit, (b) wait 1.5μs min.,(c) transfer the data and (d) release the inhibit.

ANALOG OUTPUTS

The analog outputs are V, e, and θ. V is an internal DC reference, +7.5VDC nominal. The outputs e, E, and θ ride on the internal DC reference voltage V, and should be measured with respect to V. Outputs can swing ±5V when the voltage level of the +15V power supply is +15V. The output swing swing changes proportionally if the level is not at +15V.

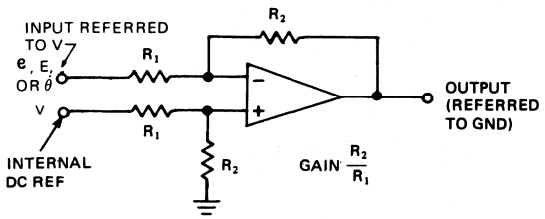
Output e is the AC error voltage sin $(\theta - \Phi)$ near the null point. Its average amplitude at nominal input voltage for +1 LSB of error (equivalent to $(\theta - \Phi) = 0.022°$) is 16 mV rms.

E is a DC voltage proportional to the error $(\theta - \Phi)$ near the null point, with −1 VDC output per +LSB of error.

θ is a DC voltage proportional to the angular velocity $d\theta/dt = d\Phi/dt$. A +1 VDC output corresponds to +2.1 rps for 400 Hz units, and +0.54 rps for 60 Hz units.

Maximum loading for each analog output is 1.0 mA. Outputs e, E, and θ are not required for normal operation of the converter; V is used as internal DC reference with the voltage follower buffer option.

The figure shows a difference circuit which may be used to reference the analog outputs with respect to normal ground instead of the internal DC reference ground V.



DIFFERENCE CIRCUIT FOR ANALOG OUTPUTS

The output e, E and $\hat{\theta}$ are not closely controlled or characterized. Consult factory for further information.

USE AS A CT

The HSDC-8915 Series S/D can be used as a "Solid State CT". This is analogous to the function of a rotary control transformer except here the rotary shaft input is replaced by a digital angle. Referring to the equation below, the output is an AC voltage (e) which varies as the sine of the difference between the analog input angle and the digital angle.

$$e = \sin(\theta - \phi)\cos\omega t$$

where θ is the analog angle and ϕ is the digital angle.

Control transformers are frequently used as error signal generators in closed servo loops. They are useful when digital remote control of a position servo must be accomplished.

The procedure to enable this function is to disable the up-down counter by setting pin 30 ($\overline{S}$) to logic "0" and using the digital output lines (which are bidirectional) as digital inputs. Note that "e" rides on the internal DC reference voltage "V" (approximately 7.5V) and a differential amplifier should be used to reference this signal to real (circuit) ground as shown in diagram under analog outputs.

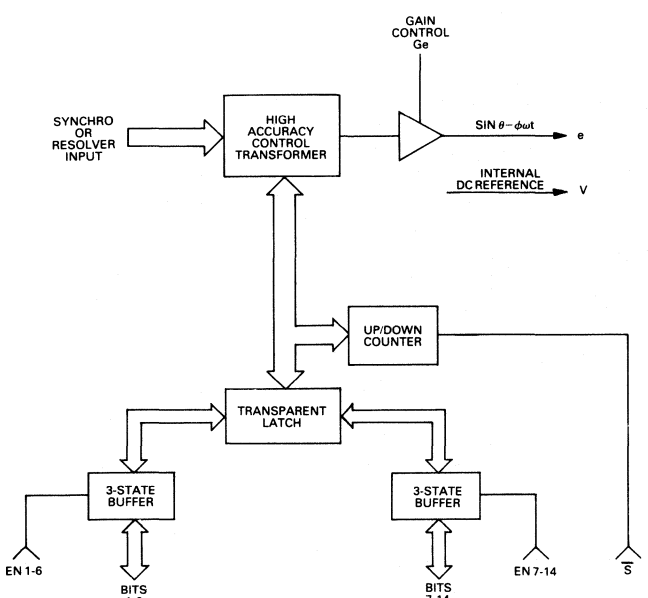


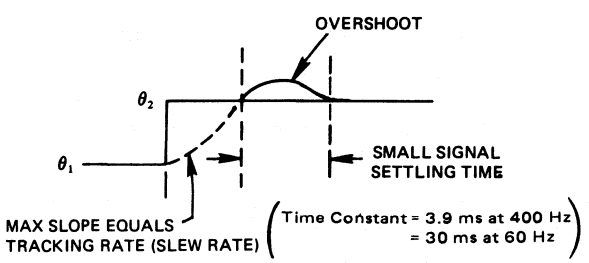
FIGURE 3. CT BLOCK DIAGRAM

The gain control function (Ge) is still operative in CT mode and the effect is the same as when used as an S/D. If you adjust the gain for a lower than nominal line-to-line signal, the error magnitude will remain the same, i.e., 16mV/LSB. If you adjust the gain for a lower signal level but come in with the "nominal" signal level, the error amplitude will be correspondingly gained-up (by the factor $V_{nominal}/V_{lower}$), however the usable error range (dynamic range) is correspondingly reduced.

DYNAMIC PERFORMANCE

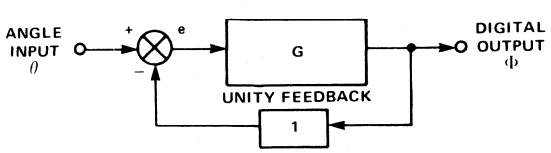
A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the HSDC-8915 Series superior dynamic performance, as listed in the specifications.

If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The response to a step input is shown below. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT

The loop dynamics of the tracking converter is shown in the diagram. The closed loop transient response is nominally critically damped. All loop dynamics can be determined from the diagram and formulas listed.



For 60 Hz

$$G = \frac{33^2\left(\frac{S}{13}+1\right)}{S^2\left(\frac{S}{130}+1\right)\left(\frac{S}{550}+1\right)}$$

For 400 Hz

$$G = \frac{255^2\left(\frac{S}{100}+1\right)}{S^2\left(\frac{S}{1000}+1\right)^2\left(\frac{S}{2000}+1\right)}$$

CONVERTER LOOP DYNAMICS

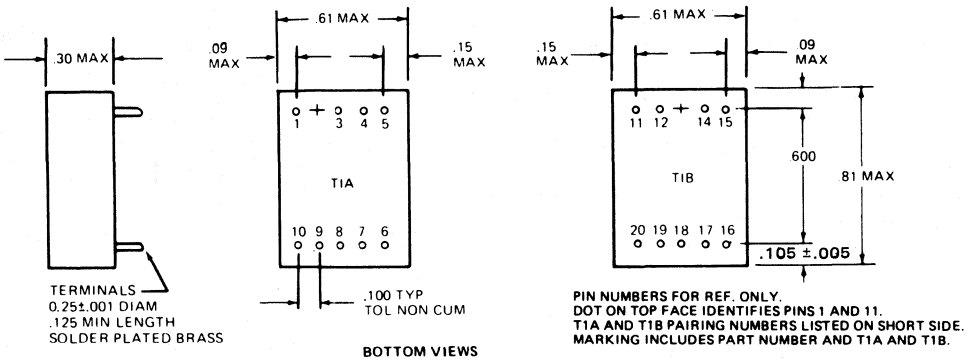
TRANSFORMER DIAGRAMS

These external transformers are for use with converter modules with voltage follower buffer inputs.

400 Hz SYNCHRO AND RESOLVER TRANSFORMER DIAGRAMS (T1A AND T1B)

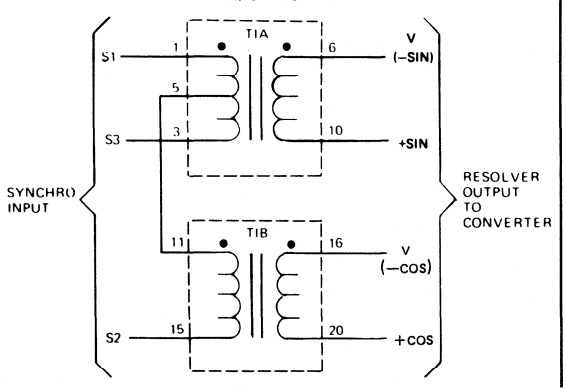
EACH TRANSFORMER CONSISTS OF TWO SECTIONS, T1A AND T1B

1. MECHANICAL OUTLINES

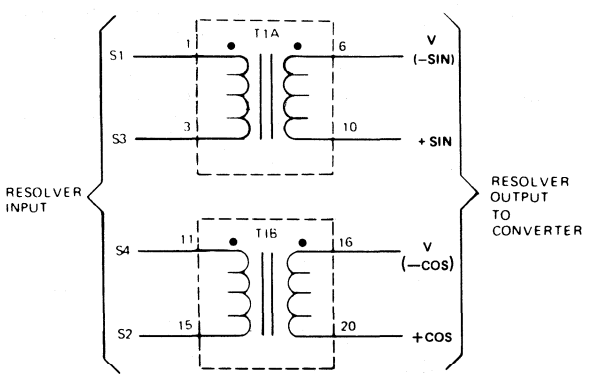


2. SCHEMATIC DIAGRAMS

A. SYNCHRO

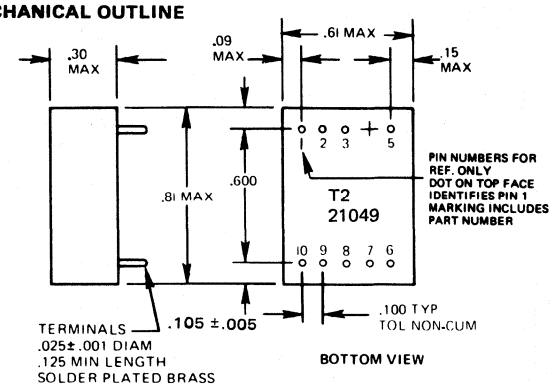


B. RESOLVER

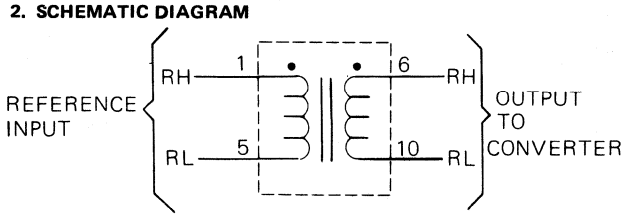


400 Hz REFERENCE TRANSFORMER DIAGRAMS (T2)

1. MECHANICAL OUTLINE

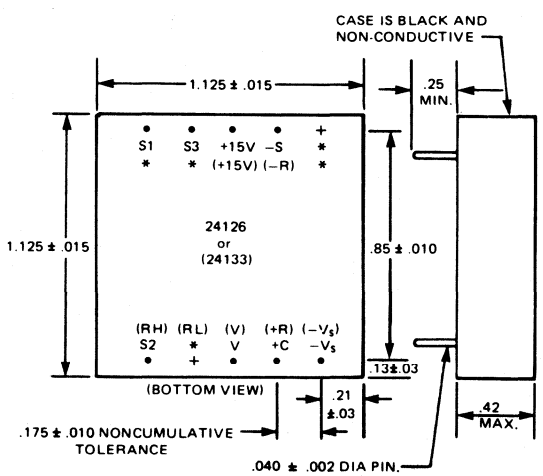


2. SCHEMATIC DIAGRAM



60 Hz SYNCHRO AND REFERENCE TRANSFORMER DIAGRAMS

The mechanical outline is the same for the synchro input transformer (24126) and the reference input transformer (24133), except for the pins. Pins for the reference transformer are shown in parenthesis ( ) below. An asterisk * indicates that the pin is omitted.



RELIABILITY

MTBF values are very high because the use of custom monolithics greatly decreases the number of active components, because thin film resistor networks are used, and because of careful thermal design. Summaries of MTBF calculations and susceptibility information are available on request.

All DDC hybrids are built in accordance with requirements of MIL-STD-883. Screening is based on the requirements of Method 5004/5008 except for burn in, which is optional. To specify preburn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) is 6,400,000 hours, Ground Benign, at 25°C.

ORDERING INFORMATION

1. Converters may be ordered as follows.

HSDC - 8915 –1 –a –883B

- MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883, DDC procedures
  - Blank = Same, except pre burn in test and burn in are omitted.
- Accuracy:
  - Blank = ±4 minutes ±0.9 LSB (Standard)
  - a = ±2.6 minutes max. (High Accuracy)
- Operating Temperature Range:
  - 1 = –55°C to +125°C
  - 3 = 0°C to +70°C
- Input Type:
  - Voltage Follower Buffer (requires external signal conditioner such as an isolation transformer):
    - 8915 = 400 Hz
    - 8916 = 60 Hz
  - Solid State Synchro (direct input):
    - 8917 = 400 Hz, 11.8V L-L
    - 8918 = 400 Hz, 90V L-L
    - 8919 = 60 Hz, 90V L-L
  - Solid State Resolver (direct input):
    - 8920 = 400 Hz, 11.8V L-L
    - 8921 = 400 Hz, 26V L-L
    - 8922 = 400 Hz, 90V L-L

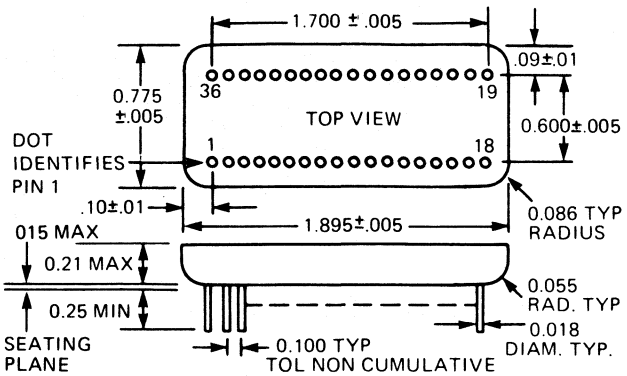
2. Reference and signal transformers for the voltage follower buffer input converters must be ordered separately as follows:

Type	Frequency	Ref. Voltage	L-L Voltage	Part Numbers Ref. Xfmr.	Part Numbers Signal Xfmr.
Synchro	400 Hz	115V	90V	21049	21045*
Synchro	400 Hz	26V	11.8V	21049	21044*
Resolver	400 Hz	115V	90V	21049	21048*
Resolver	400 Hz	26V	26V	21049	21047*
Resolver	400 Hz	26V	11.8V	21049	21046*
Synchro†	60 Hz	115V	90V	24133-1 24133-3	24126-1 24126-3

*The part number for each 400 Hz synchro or resolver isolation transformer includes two separate modules as shown in the outline drawings.

†60 Hz synchro transformers are available in two temperature ranges:
- 1 = –55°C to +105°C
- 3 = 0°C to +70°C

MECHANICAL OUTLINE
36 PIN DOUBLE DIP



NOTES

1. Dimensions shown are in inches.
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

PIN CONNECTION TABLE

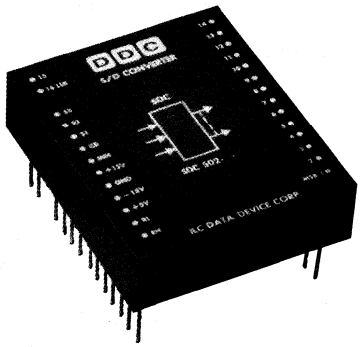
PIN	FUNCTION Solid St. Resolver	FUNCTION Solid St. Synchro	FUNCTION Volt. Fol. Buffer	PIN	FUNCTION
1	S1	S1	N.C.	19	RH (Ref. High)
2	S2	S2	COS	20	RL (Ref. Low)
3	S3	S3	SIN	21	N.C.
4	S4	N.C.	N.C.	22	E (Filtered DC Error Out)
5	Bit 1 MSB			23	θ (Analog Velocity Out)
6	Bit 2			24	CB (Converter Busy)
7	Bit 3			25	$\overline{\text{EN 7-14}}$ (Enable, Bits 7 to 14)
8	Bit 4			26	$\overline{\text{EN 1-6}}$ (Enable, Bits 1 to 6)
9	Bit 5			27	e (AC Error Out)
10	Bit 6			28	V_L (Logic Voltage Input)
11	Bit 7			29	GND
12	Bit 8			30	$\overline{S}$
13	Bit 9			31	Ge (Gain Control)
14	Bit 10			32	+15V (Power Supply In)
15	Bit 11			33	INH (Inhibit)
16	Bit 12			34	V (Internal DC Ref.)
17	Bit 13			35	BC (Buffered Cos)
18	Bit 14 LSB			36	BS (Buffered Sin)

NOTES

BS and BC pins are used in other applications.

SDC-502 SERIES*

16 BIT S/D OR R/D CONVERTERS
Accuracy ±40 sec



DESCRIPTION AND APPLICATIONS

The 16 bit, 400 Hz SDC-502 Series are high resolution synchro-to-digital or resolver-to-digital tracking converters with standard pin configurations. They use a patented control transformer algorithm that provides inherently high accuracy and jitter-free output. Two accuracy options are available: ±1 minute which is standard for 16 bit S/D converters, and ±40 seconds for higher accuracy requirements. The reference voltage for the converter is synthesized from the signal input for optimum quadrature rejection. Signal to reference phase shifts of up to 50° will not affect the accuracy. The input frequency range is 350 to 1000 Hz, and can be extended to 10 kHz with only slight degradation in accuracy when the voltage follower buffer input option is used. SDC-502 Series converters are used when 16 bit resolution and high accuracy are required. Such applications include radar target tracking. The SDC-502 can replace two-speed synchro systems in situations such as azimuth angle indicators where greater mechanical simplicity is desired. Other applications include simulators and automatic test equipment (ATE).

FEATURES

- *HIGH ACCURACY*
  ±1 Minute, Standard
  ±40 Seconds, High Accuracy Option
- *SYNTHESIZED REFERENCE*
  Improves Quadrature Rejection
- *NO TRIMS, NO ADJUSTMENTS*
- *TRANSFORMER ISOLATION*
- *ALL COMMON 400 Hz L-L LEVELS*

*Patented

SPECIFICATIONS

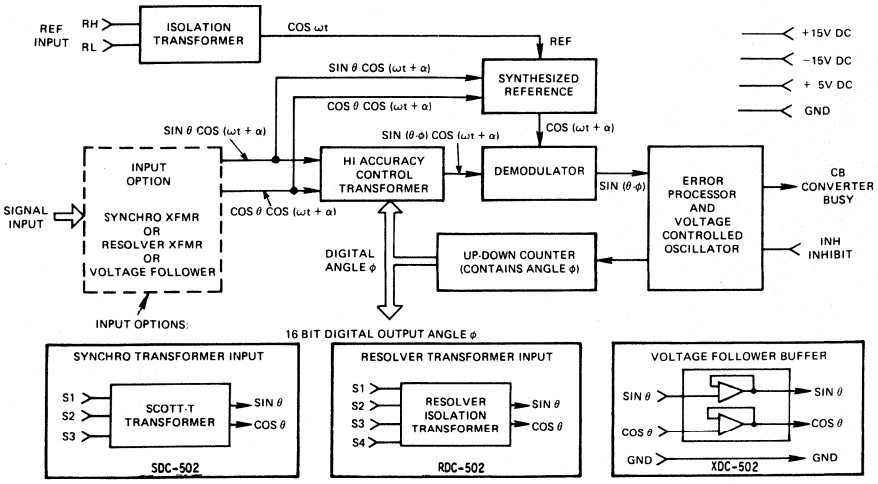
Apply over temperature range, power supply range, reference frequency and amplitude range, ± 10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	UNIT	VALUE
RESOLUTION	Bits	16 bits
ACCURACY		
Standard Unit	min	±1 (±3 LSB)
High Accuracy (Option a)	sec	±40 (± 2 LSB)
REFERENCE and SIGNAL INPUTS*		
Reference input		
Type		Transformer isolated, input impedance is maintained with power off.
Frequency Range	Hz	350-1000 (other frequencies available on special order).
Allowable Phase Shift	degrees	± 50 max relative to input signal for full accuracy.
Breakdown Voltage	V	500 min to ground.
SIGNAL INPUT		
Transformer Input		
Breakdown Voltage	V	500 min to ground.
Voltage Levels and Frequencies		See Table Below.

	SIGNAL INPUT			REFERENCE INPUT	
MODEL NUMBER	INPUT TYPE	LEVEL (L-L BALANCED)	INPUT IMPEDANCE	LEVEL	INPUT IMPEDANCE (RESISTIVE)
XDC-502-4	Direct	2V, 400 Hz 25V without damage	20mΩmin	10-50V rms	80kΩmin
SDC-502-L	Synchro	11.8V L-L, 400 Hz	40kΩmin	10-50V rms	80kΩmin
SDC-502-H	Synchro	90V L-L, 400 Hz	500kΩmin	40-150V rms	300kΩmin
RDC-502-L	Resolver	11.8V, L-L	100kΩmin	10-50V rms	80kΩmin
RDC-502-M	Resolver	26V, L-L	200kΩmin	10-50V rms	80kΩmin

*Other voltage levels and frequencies available on special order.

PARAMETER	UNIT	VALUE
DIGITAL INPUT/OUTPUT (TTL LOGIC)		
Inhibit Input (INH)		Logic 0 inhibits converter Loading is 0.2 Std. TTL loads plus 18kΩmin pull-up resistor to +5V supply
Digital Outputs (Low Power Schottky)		
Drive Capability	TTL Loads	2 Std.
16 Parallel Data Bits		Natural binary angle; positive logic 0.5-1.5μs positive pulse
Converter Busy (CB)		Data changes on leading edge Data valid 0.5μs after leading edge
DYNAMIC CHARACTERISTICS		
Input Rate for Full Accuracy (Min. Range)	rps (°/sec)	0-1.25 (450)
Acceleration for 1LSB Lag	(°/sec²)	124 typ.
Velocity Constant		K_V = ∞ (Type II servo loop)
Acceleration Constant		K_A = 22,500 sec⁻² nominal
Settling Time	ms	500 to ±1LSB of final value
For 179° Step Change	ms	600ms to final value
POWER REQUIRED		
Nominal Voltage		+15V Supply / −15V Supply / +5V Logic Supply
Voltage Range	V	+11 to +16.5 / −11 to −16.5 / +4.5 to +5.5
Max Voltage Without Damage		+18V / −18V / +7V
Current	ma	10 typ / 27 typ / 100 typ
	ma	15 max / 40 max / 150 max
TEMPERATURE RANGES		
Operating		
-1 Option	°C	−55 to +105
-3 Option	°C	0 to +70
Storage	°C	−55 to +125
PHYSICAL CHARACTERISTICS		
Size	in	3.125 x 2.625 x 0.82 (79.4 x 66.7 x 20.8 mm)
Weight	oz	7 oz typ (200g)



SDC-SERIES BLOCK DIAGRAM

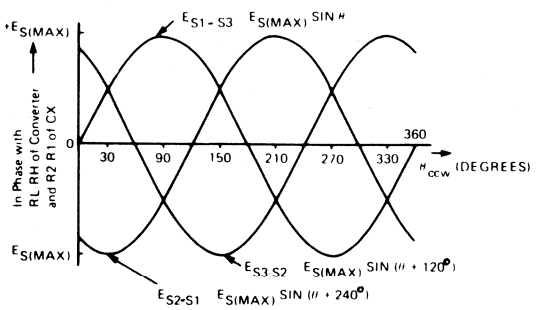
TECHNICAL INFORMATION

INTRODUCTION

Two key features that help the 16 bit SDC-502 Series to achieve its high ±40 second accuracy are its high accuracy control transformer and its synthesized reference. The control transformer produces an inherently more accurate, jitter-free output because it is based on an improved algorithm. The synthesized reference eliminates errors caused by quadrature voltage because its output is in phase with the signal input.

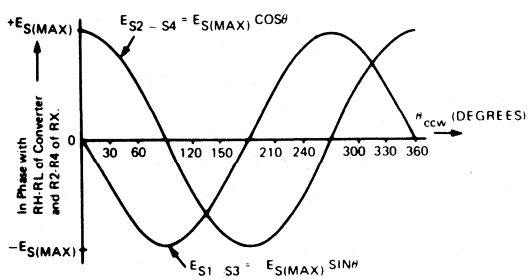
A synchro or resolver signal generally leads the reference signal by about 6° because these transducers are inductive. When an uncompensated reference signal is used to demodulate the control transformer output, quadrature voltages are not completely eliminated. In a 12 or 14 bit converter it is not necessary to compensate for the phase lead in the reference signal. A 6° phase shift will, however, cause problems for the much more accurate SDC-502. As shown in the Block Diagram, the 16 bit converter synthesizes its own cos ($\omega t + \alpha$) reference signal from the sin θ cos ($\omega t + \alpha$), cos θ cos ($\omega t + \alpha$) signal inputs and from the cosωt reference input. The phase angle of the synthesized reference signal is determined by the signal input, and the reference input is used to choose between the +180° and −180° phases. The synthesized reference will always be exactly in phase with the signal input, and quadrature errors will therefore be eliminated.

In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The internal converter in the SDC-502 Series operates with signals in resolver format, i.e., sin θ cosωt and cos θ cosωt, as shown in the Block Diagram. Synchro signals are of the form sin θ cosωt, sin (θ + 120°) cosωt, and sin (θ + 240°) cosωt. The diagrams show synchro and resolver signals as a function of the angle θ.



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ)

SYNCHRO SIGNALS



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

RESOLVER SIGNALS

The main components of the SDC-502 are connected in a feedback loop consisting of the control transformer, the demodulator, the error processor and voltage controlled oscillator, and the up-down counter. θ is the angle of the synchro or resolver shaft, and ϕ is the 16 bit digital angle contained in the up-down counter. The tracking process consists of continually changing ϕ to make (θ-ϕ) →0, so that ϕ will be equal to the shaft position θ.

The control transformer output is a modulated carrier signal with an amplitude sin (θ - ϕ). The control transformer performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

The output of the demodulator is an analog DC level proportional to sin (θ - ϕ). The error processor integrates this error signal sin (θ - ϕ), and the output of the integrator is used to control the frequency of a voltage controlled oscillator. This oscillator produces "clock" pulses which are accumulated by the up-down counter. The up-down counter is functionally an incremental integrator. Therefore there are two stages of integration, making the converter a Type II tracking loop. There will be no position error due to velocity, because in a Type II loop, the voltage controlled oscillator always settles to a counting rate which makes dϕ/dt equal to dθ/dt without lag. The only errors will be momentary (transient) errors during acceleration or deceleration. The output data will always be fresh and available without lag so long as the maximum tracking rate of the converter is not exceeded.

INPUT OPTIONS

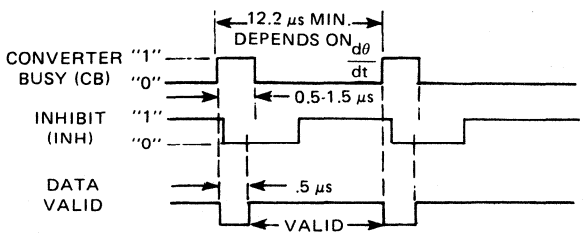
The SDC-502 has two kinds of input options. The transformer input options isolate the input, step down the signal voltage, and provide a resolver type signal for the internal high accuracy control transformer. The voltage follower buffer input option is a dual voltage follower for the sin θ and cos θ inputs. The voltage follower input requires a line-to-line level of 2V rms ±10% which can be obtained by reducing the resolver reference voltage level. It is a relatively low cost option because there is no transformer and because high accuracy is more easily achieved when the transformer is eliminated. The buffer inputs are DC coupled with broadband characteristics. Full accuracy is achieved up to 1000 Hz, and the frequency range can be extended to 10 kHz with only slight degradation in accuracy (consult factory for further information).

To prevent damage to the input transformers, the maximum voltage should not exceed the specified input voltage by more than 30%. The maximum common mode voltage (DC plus recurrent AC peak) should not exceed 500V.

TIMING

The timing waveforms of the converter are shown in the Timing Diagram. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy pulse (CB). The CB is a positive pulse 0.5 to 1.5μsec long. Data changes on the leading edge of the CB pulse, and data can be transferred 0.5μsec after the leading edge. The trailing edge of the CB can be used to transfer data.

The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the inhibit is applied. The converter will ignore an inhibit applied during the "busy" interval until that interval is over. Timing is as follows: (a) apply the inhibit, (b) wait 0.5μs, (c) transfer the data, and (d) release the inhibit. Extra CB pulses will not occur if the input angle changes while the counter is locked by the INH.



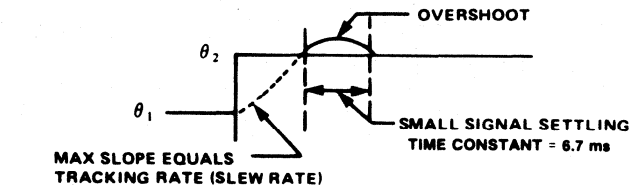
TIMING DIAGRAM

DYNAMIC PERFORMANCE

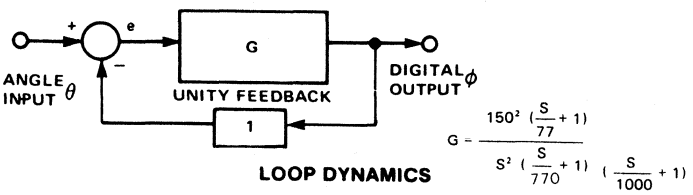
A Type II servo loop ($K_v = \infty$) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltages are not the ±15 VDC nominal values, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage. The +15V supply voltage will determine the positive maximum velocity, and the —15V supply voltage will determine the negative maximum velocity.

So long as the maximum tracking rate is not exceeded, there will be no lag in the converter output due to velocity. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The figure shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.

The loop dynamics of the converter are given in the diagram. The closed loop transient response is nominally critically damped. All loop dynamics can be determined from the diagram and formulas listed.



RESPONSE TO A STEP INPUT

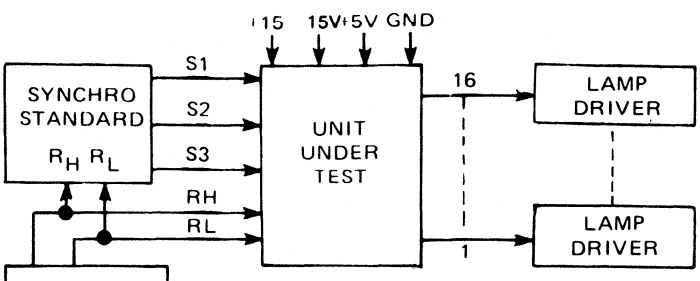


LOOP DYNAMICS

ACCURACY TESTS

Because of the high accuracy of these converters, only laboratory-grade synchro or resolver substitution boxes or standards should be used. If synchro standards are not available, arrangements may be made to use DDC's facilities for "source inspection" at no extra cost.

To test the unit, test equipment may be arranged as shown. A lamp-driver or suitable readout is necessary for each of the data outputs. The Synchro Standard is set to the test angles. The angles corresponding to the lights which are on are added and compared with the standard angle.



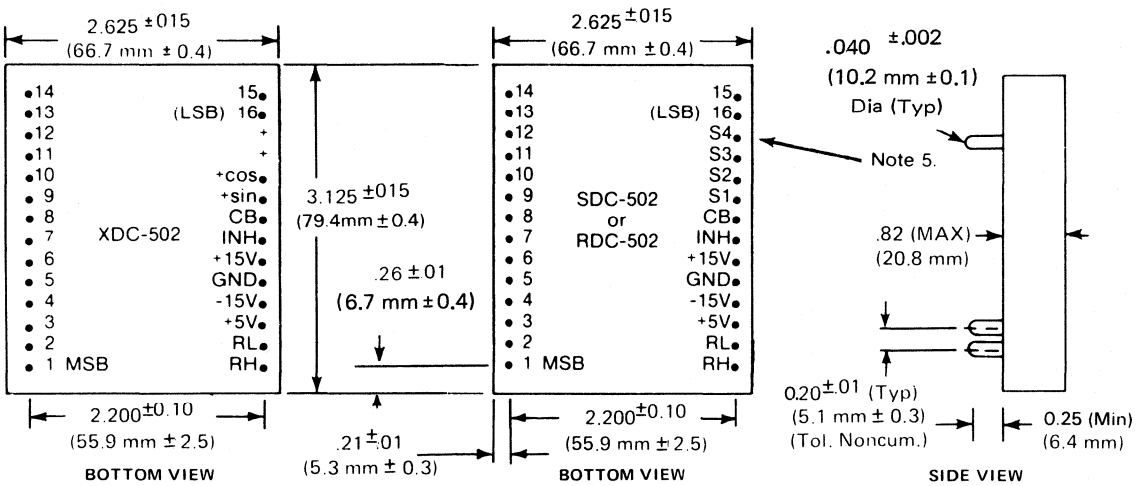
ACCURACY TEST CIRCUIT

POWER SUPPLIES

The main power supplies can vary over their specified ranges with no change in the converter specifications except for a proportional change in the maximum tracking rates. The power supplies are capacitively decoupled internally.

When testing or evaluating the converters, it is advisable to limit the current from each of the three power supplies. Set each limit to 50% greater than the maximum current listed for that supply in the specifications table.

MECHANICAL OUTLINES



NOTES
1. Pin labels on bottom view are for reference only.
2. All dimensions shown are in inches.
3. Pin material meets solderability requirements of MIL-STD-202E, Method 208C
4. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.
5. Pin S4 is present on Resolver units, and omitted on Synchro units.

ORDERING INFORMATION

SDC-502-L-1-a

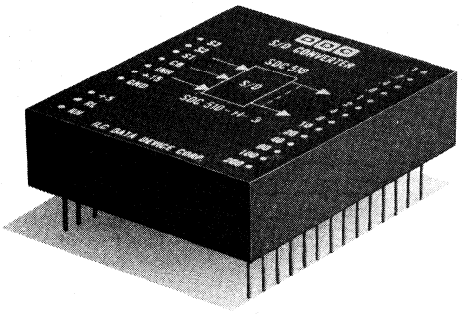
- Accuracy:
  - Blank = ±1 minute (Standard)
  - a = ±40 seconds (High Accuracy)
- Temperature Range (Operating)
  - 1 = -55°C to +105°C
  - 3 = 0°C to + 70°C
- Signal Input Voltage:
  - -H = 90V L-L, 400Hz (Synchro Only)
  - -L = 11.8V L-L, 400Hz (Synchro or Resolver)
  - -M = 26V L-L, 400Hz (Resolver Only)
  - -4 = 2V L-L, 400Hz (Direct Only)
- Optional Inputs:
  - SDC - Synchro
  - RDC - Resolver
  - XDC - Voltage Follower Buffer

CONFIGURATIONS CURRENTLY AVAILABLE

Resolver Input	All Devices currently available are offered throughout the specified temperature and accuracy ranges, listed in the ordering information.
RDC-502-L	
RDC-502-M	
Synchro Input	
SDC-502-H	
SDC-502-L	
Direct Input	
XDC-502-4	

If a socket is required, order socket number 9010.

4 DECADE BCD S/D AND R/D CONVERTERS
Resolution 0.1°; Accuracy ±0.1° ±0.9 LSB



FEATURES

- *UNIPOLAR (0–360°) OR BIPOLAR (±180°) OUTPUT*
- *SIGNAL AND REFERENCE INPUTS:*
  Internal transformer isolation at 60 Hz and 400 Hz
  All common L-L voltage levels and frequencies
- *LOGIC:*
  TTL compatible
  4 decade parallel BCD angle
  Converter Busy and Inhibit
- *POWER REQUIRED:*
  +15V DC and +5V DC

DESCRIPTION

This series is a group of low-cost, high-resolution synchro-to-BCD and resolver-to-BCD tracking converters. They convert 3-wire synchro or 4-wire resolver output information continuously into BCD angle format, error-free at rates of 0° to 1080° per second. These are the smallest, lightest and most accurate devices on the market within their price range.

Transformer-isolated high-input impedance to both signal and reference eliminates loading errors. Utilizing a type II servo loop, these converters have no velocity lag up to the specified tracking rate, and output data is always fresh and continuously available. Each unit is fully trimmed and requires no adjustments or calibrations in the field.

APPLICATIONS

These units may be used wherever analog angle data from a synchro or resolver must be converted rapidly and accurately to BCD digital form for display, storage, or analysis. Because these units are extremely rugged, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial and commercial applications. Military ground support and avionics uses include ordnance control, radar tracking systems, navigation and collision avoidance systems.

SPECIFICATIONS

Apply over temperature range, ±5% variation of power supply voltages, reference frequency range, ±10% signal and reference amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE		
RESOLUTION	0.1°(3-1/2 decade BCD)		
CODING	0° – 359.9° for SDC 510 ±179.9° for SDC 511		
ACCURACY	±6 minutes ±0.9 LSB		
ANALOG INPUT CHARACTERISTICS			
Synchro Input*:	Signal Frequency Range	Signal Input Impedance (L-L Balanced, Resistive)	
90V L-L, 400 Hz (Option H)	350–1000 Hz	600 KΩ min	
90V L-L, 60 Hz (Option I)	47–1000 Hz	100 KΩ min	
11.8V L-L, 400 Hz (Option L)	350–1000 Hz	10 KΩ min	
90V L-L, 60 Hz (Option 6)	47–1000 Hz	500 KΩ min	
Resolver Input*:			
90V L-L, 400 Hz (Option H)	350–1000 Hz	600 KΩ min	
26V L-L, 400 Hz (Option M)	350–1000 Hz	100 KΩ min	
11.8V L-L, 400 Hz (Option L)	350–1000 Hz	10 KΩ min	
Reference Input*:	Reference Voltage	Current	
Option H	115V	1.2 mA	
Options M, L	26V	5 mA	
Options I, 6	115V	3.3 mA	
*Transformer isolated. Other voltages and frequencies available on special order.			
DIGITAL INPUT/OUTPUT			
Logic Type	TTL/DTL compatible		
Input			
Inhibit (INH)	2 Standard TTL loads Logic "0" inhibits		

PARAMETER	VALUE	
DIGITAL INPUT/OUTPUT (Cont'd)		
Outputs		
Drive Capability	5 Standard TTL loads	
4 decade BCD	Parallel positive logic; 14 lines; 0.1° to 200° for SDC 510 and 0.1° to 100° plus sign bit for SDC 511.	
Converter Busy (CB)	2 to 4μs positive pulse	
DYANAMIC CHARACTERISTICS		
Input Rate for Full Accuracy		
400 Hz Units	1080°/sec	
60 Hz Units	360°/sec	
Acceleration for 1 LSB Lag		
400 Hz Units	4000°/sec²	
60 Hz Units	250°/sec²	
POWER SUPPLIES		
Voltage	+15V ±5%	+5V ±5%
Absolute Max Voltage	+18V	+7V
Current	40 mA max	450 mA max
TEMPERATURE RANGES		
Operating		
–1 Option	–55° to +105°C	
–3 Option	0° C to +70°C	
Storage	–55°C to +125°C	
PHYSICAL CHARACTERISTICS		
Size	2.625 x 3.125 x 0.82 inch (6.67 x 7.94 x 2.08 cm)	
Weight	7 oz typ (300g)	

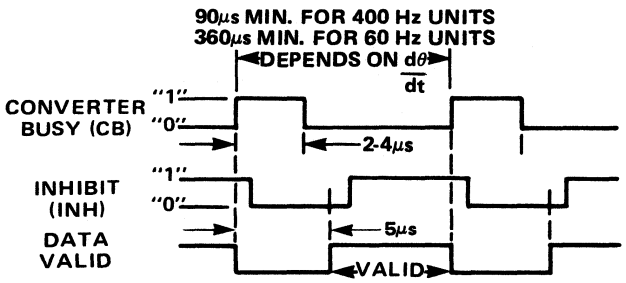
TECHNICAL INFORMATION

ANGLE OUTPUTS

The digital output bits on the SDC-510 go from 0.1° to 200°, giving output angles over the range 0° to 359.9°. On the SDC-511, the 200° bit is replaced by a sign bit, with + represented by logic 0, so that the output angle ranges from −179.9° to +179.9°.

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a CONVERTER BUSY pulse. During the 2-4μs "busy" pulse, the output data is changing and should not be transferred into the computer input buffer. The converter will ignore an INHIBIT command applied during the "busy" interval until that interval is over. Extra CB pulses will not occur if the input angle changes while the counter is locked by the INH. A simple method of interfacing to a computer is to: (a) apply the inhibit, (b) wait 5μs, (c) transfer the data, and (d) release the inhibit.

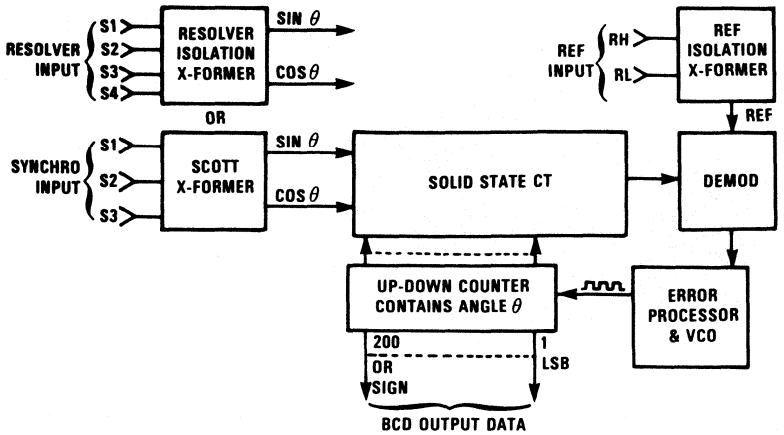


TIMING DIAGRAM

POWER SUPPLIES

Two supplies are required. They should be well regulated and, when testing or evaluating the converter on the bench, be of the current-limited type. Set the current limiting as follows:

+15V supply at 6 mA
+5V supply at 500 mA



BLOCK DIAGRAM

ORDERING INFORMATION

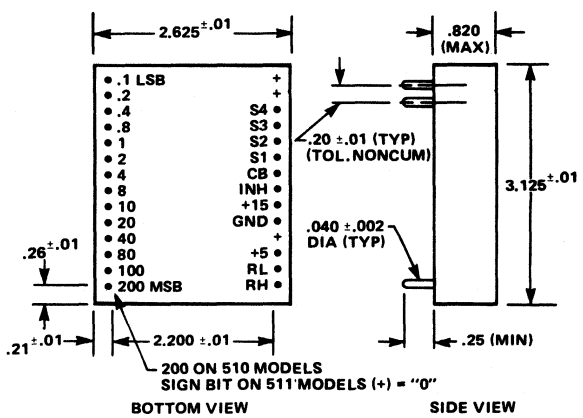
SDC – 510 – H – 1

- 1 — Temperature Range (Operating):
  - 1 = −55°C to +105°C
  - 3 = 0°C to +70°C
- H — Signal Input Voltage and Frequency:
  - H = 90V L-L, 350 – 1000 Hz (Synchro or Resolver)
  - I = 90V L-L, 47 – 1000 Hz (Synchro Only)
  - M = 26V L-L, 350 – 1000 Hz (Resolver Only)
  - L = 11.8V L-L, 350 – 1000 Hz (Synchro or Resolver)
  - 6 = 90V L-L, 47 – 1000 Hz (Synchro Only – With External Transformer)
- 510 — Output Code:
  - 510 = 0 to 359.9°
  - 511 = ±179.9°
- SDC — Input Type:
  - SDC = Synchro
  - RDC = Resolver

If a socket is required, order socket number 9010.

MECHANICAL DIAGRAMS AND TRANSFORMER CONNECTIONS

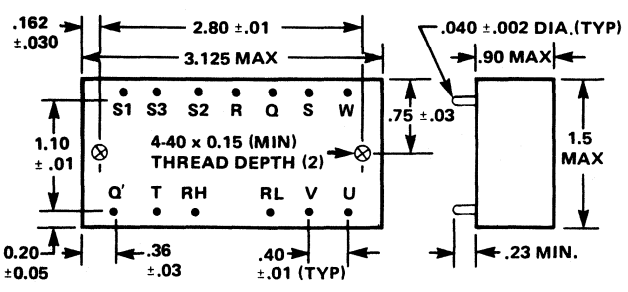
1. CONVERTER MODULE MECHANICAL OUTLINE



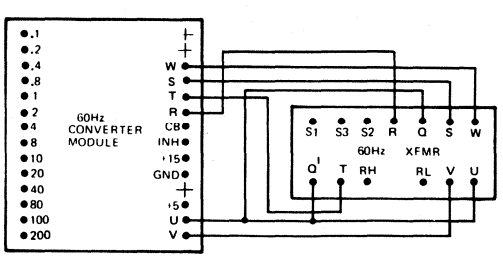
Notes:

1. Pin material is electrosoldered brass per MIL-F-14072, M222.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.
3. Pin S4 is present on Resolver options only.
4. The above pin designations are for internal transformer options H, M, L and I. For external transformer option 6, the signal and reference input pins are labeled as shown on the transformer connection diagram.

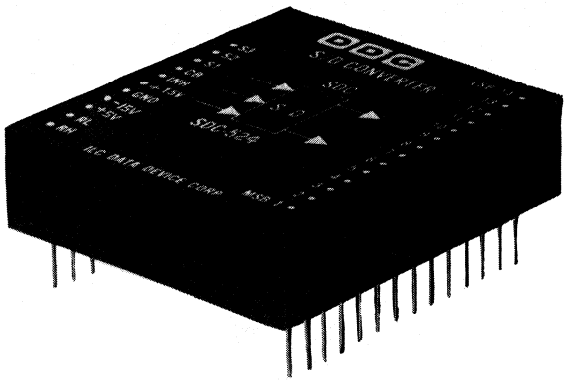
2. TRANSFORMER MECHANICAL OUTLINE



3. TRANSFORMER CONNECTION DIAGRAM



12 AND 14 BIT S/D AND R/D CONVERTERS
Low Cost Tracking Converters



FEATURES

- *STANDARD 12 AND 14 BIT CONVERTERS*
- *ACCURACY:*
  ±6 minutes ±0.9 LSB for 12 bits
  ±4 minutes ±0.9 LSB for 14 bits
- *SIGNAL AND REFERENCE INPUTS:*
  Internal transformer isolation
  All common L-L voltage levels and frequencies
- *LOGIC:*
  TTL, and low power Schottky options
  Parallel binary angle output
  Converter Busy and Inhibit
- *POWER REQUIRED:*
  ±15V DC and logic voltage supply

DESCRIPTION

DDC's SDC-520 series is the second generation tracking S/D converter and is pin-for-pin compatible with standard modular converters. Available with 12- or 14-bit resolution, the units accept either 3 wire synchro or 4 wire resolver information and provide continually updated digital angle data without velocity lag. The converters measure .82 x 2.625 x 3.125 and weigh only 7 oz. Their high input impedance, transformer isolation and transient protection insure trouble free system integration.

APPLICATIONS

Constructed of all MIL-grade parts (no plastic), and meeting the requirements of MIL-STD-202E, the SDC-520 series is suitable for both military and industrial applications. These converters are used in ground support, avionics, fire control, radar tracking, navigation and collision avoidance systems, as well as in machine tool and table positioning control systems. Their low cost makes them price-competitive in systems previously using optical and magnetic encoders.

SPECIFICATIONS

PARAMETER	VALUE		PARAMETER	VALUE
RESOLUTION, BITS	SDC-522: 12	SDC-524: 14	**POWER SUPPLY REQUIREMENTS** (4)(5)	+15 / −15V / +5/V_L
ACCURACY, WORST CASE (1)	6 min ±0.9 LSB	4 min ±0.9 LSB	For TTL (−TT−) Units: Max (Typ) mA	50(40) / 20(15) / 350(275)
CODING	Natural Binary Angle		For L.P. (−LS−) Schottky Units:	50(40) / 20(15) / 110(80)
DIGITAL OUTPUT	Parallel Positive Logic, 12, or 14-bit angle data, converter busy		**SYNCHRO RATES**	
DIGITAL INPUT	Inhibit, logic "0" = INH		No. of BITS / MAX TRACKING RATE (°/sec) / SETTLING* TIME FOR 179° STEP (ms) / ACCEL. FOR 1 LSB LAG (°/sec²)	
LOGIC TYPE	−TT − for TTL −LS − for low power Schottky		400 Hz Units	
SYNCHRO INPUT (2) (3)			12 / 14,400 / 130 / 3,500	
11.8 V rms L-L 350-1000 Hz into 10 KΩ min L-L balanced −L−			14 / 3,600 / 200 / 880	
90V rms L-L 350-1000 Hz into 600 KΩ min L-L balanced −H−			60 Hz Units	
90V rms L-L 47-440 Hz into 500 KΩ min L-L balanced −6−			12 / 3,600 / 520 / 176	
90V rms L-L 47-440 Hz into 100 KΩ min L-L balanced −I−			14 / 900 / 800 / 44	
RESOLVER INPUT (2)(3)			*For settling to final value.	
11.8V rms L-L 350-1000 Hz into 10 KΩ min L-L balanced −L−			**TEMPERATURE RANGES**	
26V rms L-L 350-1000 Hz into 100 KΩ min L-L balanced −M−			Operating	
90V rms L-L 350-1000 Hz into 600 KΩ min L-L balanced −H−			−1 Units	−55°C to 105°C
REFERENCE INPUT (2)(3)			−3 Units	0°C to +70°C
26V at 5 mA rms 350-1000 Hz −L− −M−			Storage	−55°C to +125°C
115V at 1.2 mA rms 350-1000 Hz −H−				
115V at 3.3 mA rms 47-440 Hz −6− −I−				

(1) Accuracy applies over operating temperature range, power supply voltage range, frequency range, and ±10% amplitude variation of signal and reference.

(2) Other input voltages and frequencies available

(3) Transformer isolated

(4) Units can operate on voltages between ±11 to ±16.5 VDC

TECHNICAL INFORMATION

LOGIC INPUTS/OUTPUTS

The SDC-520 series is available with TTL, CMOS, or low power Schottky logic. Load and drive capability of these are given below:

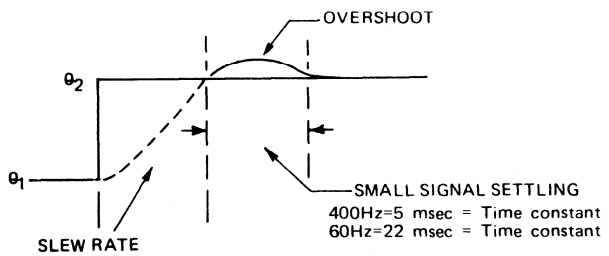
TTL Units: Output drive capability (fan out) is 5 standard unit TTL loads. The inhibit (INH) load is two standard loads.

Low Power Schottky Units: Output drive capability (fan out) is two standard unit TTL loads. Inhibit (INH) load is a 0.5 standard unit load.

DYNAMIC PERFORMANCE

Response to a step input is critically damped with one overshoot as illustrated below.

The first portion of the response is initial slewing and is the maximum tracking rate of the converter. The one initial overshoot follows which is inherent to the type II servo. The return to within final value is a function of the small signal setting time.



RESPONSE TO A STEP INPUT

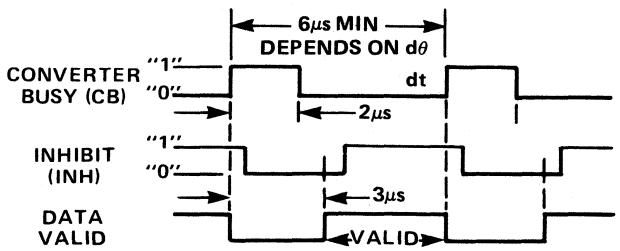
The nominal open loop transfer functions for the SDC-522/524 are

$$\frac{45^2\ (\frac{S}{22}+1)}{S^2\ (\frac{S}{220}+1)} \qquad \text{For 60 Hz}$$

$$\frac{200^2\ (\frac{S}{100}+1)}{S^2\ (\frac{S}{1000}+1)} \qquad \text{For 400 Hz}$$

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy pulse. During the 2μs "busy" pulse, the output data is changing and should not be transferred into the computer output buffer. The converter will ignore an inhibit command applied during the "busy" interval until that interval is over. A simple method of interfacing to a computer is to (a) apply the inhibit, (b) wait 3μs, (c) transfer the data, and (d) release the inhibit.



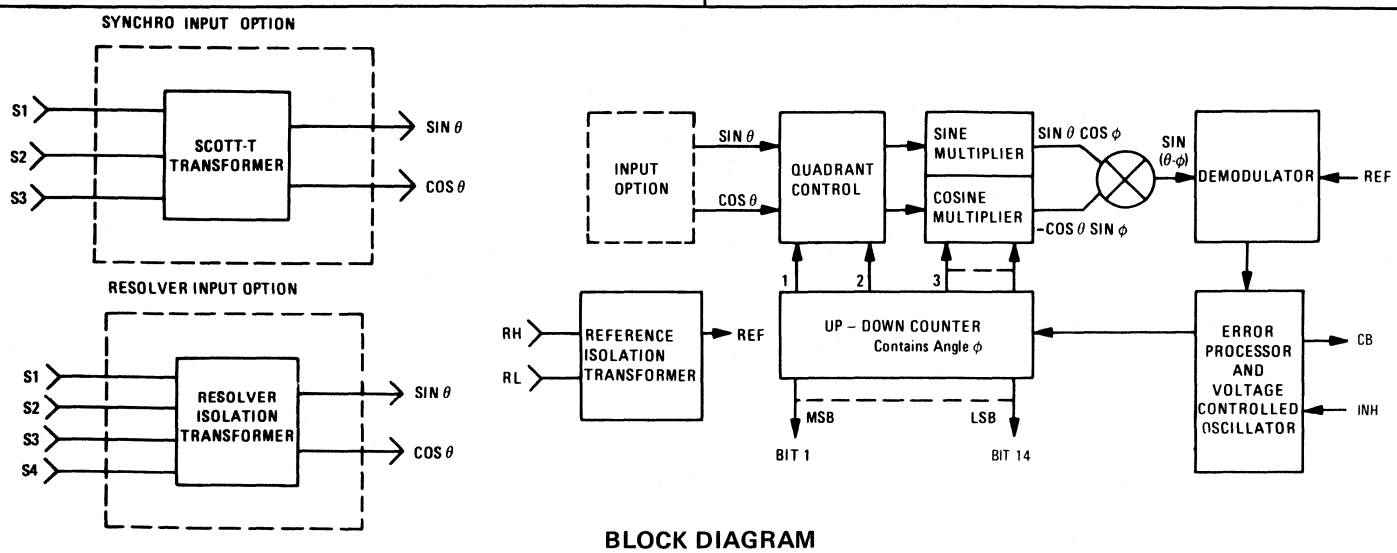
TIMING DIAGRAM

POWER SUPPLIES

Three supplies are required. They should be well regulated and, when testing or evaluating the converter on the bench, be of the current limited type. Set the current limiting as follows:

–TT–	–LS–
+15.0V @ 70 mA	70 mA
–15.0V @ 25 mA	25 mA
+5.0V @ 400 mA	150 mA

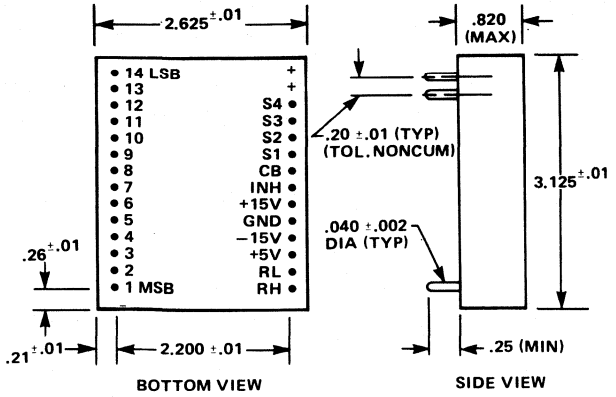
Although specified for ±15V operation, the SDC-520 series will operate on ±12V power supplies with a reduction in maximum tracking rate to 6 rps for 400 Hz units and 2 rps for 60 Hz units. Accuracy remains the same. For minimum power operation the SDC-520 series can be operated on +15 and +V alone with no –15V. Maximum tracking rate is then reduced to 2.5 rps and 1 rps, respectively.



BLOCK DIAGRAM

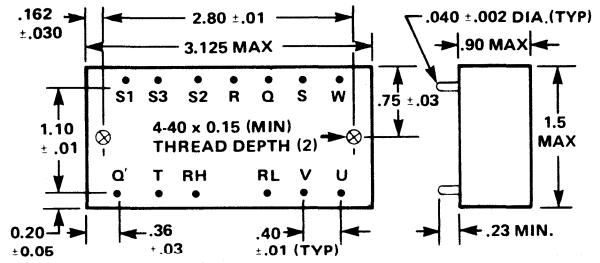
MECHANICAL OUTLINES

1. CONVERTER MODULES

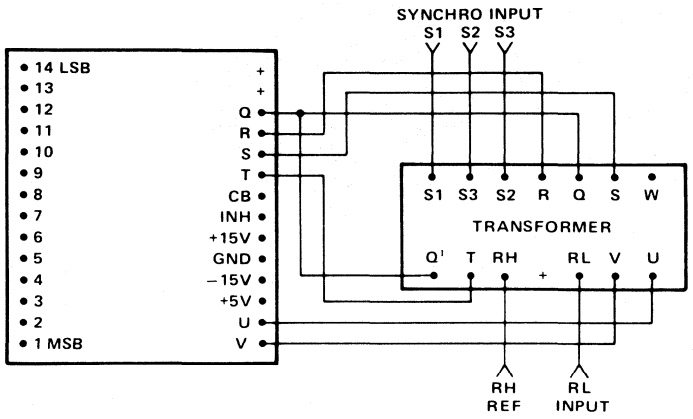


Notes:
1. Pin material is electrosoldered brass per MIL-F-14072, M222.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.
3. Pins 13 and 14 are omitted for 12 bit units.
4. Pin S4 is present on Resolver options only.
5. The above pin designations are for internal transformer options H, M, L, and I. For external transformer option 6, the signal and reference input pins are labeled as shown on the transformer connection diagram.

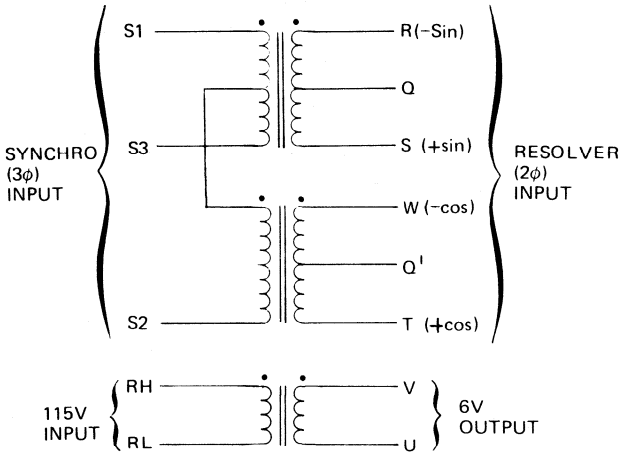
2. 60 Hz EXTERNAL TRANSFORMER MODULE



60 Hz TRANSFORMER CONNECTION DIAGRAM



TRANSFORMER INTERNAL SCHEMATIC



ORDERING INFORMATION

SDC − 524 − TT − 6 − 3

Temperature Range (Operating):
−3 = 0°C to +70°C
−1 = 55° to 105°C

Input:
6 = 90V rms L-L 50-440 Hz, 115V rms ref (Syn. Only)
H = 90V rms L-L 400 Hz, 115V rms ref
M = 26V rms L-L 400 Hz, 26V rms ref (Resolver Only)
L = 11.8V rms L-L 400 Hz, 26V rms ref
I = 90V rms L-L 50-440 Hz, 115V rms (Syn. Only)

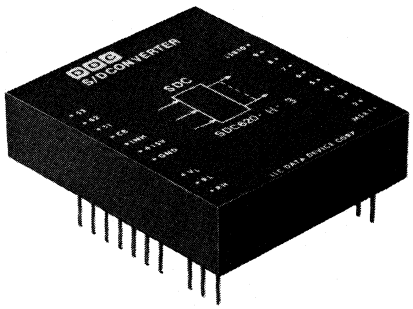
Logic Type:
TT = TTL
LS = Lowpower Schottky

Resolution:
522 = 12 bits
524 = 14 bits

Input Format:
SDC = Synchro
RDC = Resolver

External 60 Hz transformer is supplied with −6 option when ordered as above.

If a socket is required for any of the converter modules, order Socket 9010.



10 BIT S/D AND R/D CONVERTER
Low Cost; Internal Transformers

FEATURES

- *STANDARD 10 BIT CONVERTER*
- *ACCURACY: ±21 minutes*
- *SIGNAL AND REF INPUTS:*
  Internal transformer isolation
  Broadband input: 360 – 1000 Hz or 47 – 1000 Hz
  All common L-L voltage levels
- *LOGIC:*
  TTL and CMOS compatible
  10 bit parallel binary angle
  Converter Busy and Inhibit
- *POWER REQUIRED:*
  +15V DC and logic voltage supply

DESCRIPTION

The SDC-620 is a low-cost, medium resolution, synchro-to-digital or resolver-to-digital converter. It converts three-wire synchro or four-wire resolver input information continuously into 10-bit digital angle format. All standard synchro and resolver inputs can be accommodated. Utilizing a true Type II servo loop principle, the SDC-620 has no velocity lag up to the specified tracking rate, and output data is always fresh and continuously available. The use of CMOS logic accounts for very low power consumption — less than 150 mw. Each unit is fully trimmed and requires no adjustment or calibration in the field.

APPLICATIONS

The SDC-620 may be used wherever analog angle data from a synchro or resolver must be converted rapidly and accurately to digital form for transmission, storage or analysis. Because these units are extremely rugged and stable, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial, commercial and military applications. Military ground support and avionics uses include ordnance control, radar tracking systems, navigation, and collision avoidance systems.

SPECIFICATIONS

Apply over temperature range, power supply range, reference frequency range, ±10% signal and reference amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE	
RESOLUTION	10 bits	
ACCURACY (All Conditions)	±21 minutes max (= ±0.3516° = ±1 LSB)	
SIGNAL AND REFERENCE INPUT		
Synchro Input*:	Signal Frequency Range	Signal Input Impedance (L-L Balanced)
90V L-L, 400 Hz (Option H)	360 – 3000 Hz	500 KΩ min
90V L-L, 60 Hz (Option I)	47 – 1000 Hz	150 KΩ min
11.8 L-L, 400 Hz (Option L)	360 – 3000 Hz	10 KΩ min
Resolver Input*:		
90V L-L, 400 Hz (Option H)	360 – 3000 Hz	350 KΩ min
26V L-L, 400 Hz (Option M)	360 – 3000 Hz	50 KΩ min
11.8V L-L, 400 Hz (Option L)	360 – 3000 Hz	10 KΩ min
Reference Input*:	Nominal Ref. Voltage	Maximum Ref. Current
Option H	115 V rms	1.2 mA rms
Option I	115 V rms	3.3 mA rms
Options M, L	26 V rms	5 mA rms
*Transformer isolated. Other voltages and frequencies available on special order.		
DIGITAL INPUT/OUTPUT		
Logic Type	CMOS Logic; TTL and CMOS Compatible	
Inhibit Input (INH)	Logic "0" inhibits	
Loading	30 KΩ min pull-up resistor to V_L	
Outputs		
10 Parallel Data Bits	Natural binary angle; positive logic	
Converter Busy (CB)	1.5 – 3 μsec positive pulse; data changes on leading edge	
Drive Capability	4 Std. TTL loads	

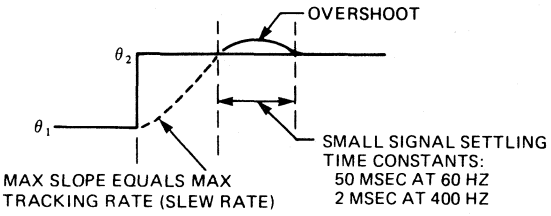
PARAMETER	VALUE	
DYNAMIC CHARACTERISTICS	400 Hz	60 Hz
Max Input Rate for Full Accuracy	36,000°/sec min	2,520°/sec min
Settling Time		
For Normal Tracking (Up to Specified Input Rate)	No Lag Error	No Lag Error
For 179° Step Change		
Settling to 1 LSB	25 msec typ	700 msec typ
Settling to Final Value	30 msec typ 50 msec max	800 msec typ 1000 msec max
Velocity Constant (Type II Servo Loop)	$K_v = \infty$	$K_v = \infty$
Acceleration Constant	K_a = 240,000 sec^{-2} typ	K_a = 400 sec^{-2} typ
Acceleration for 1 LSB Lag	84,000°/sec^2 typ	140°/sec^2 typ
POWER SUPPLIES		
Nominal Voltage	+15V Main Supply	V_L Logic Supply
Voltage Range	+11 to +17V	+4.5V to Main Supply
Max. Voltage Without Damage	+20V	+20V
Current or Impedance	6 mA typ 12 mA max	Z_{in} = 10 KΩ min
TEMPERATURE RANGES		
Operating		
–1 Option	–55°C to +105°C	
–3 Option	0°C to +70°C	
Storage	–55°C to +125°C	
PHYSICAL CHARACTERISTICS		
Size (Encapsulated Module)	3.125 x 2.625 x 0.82 inch (7.94 x 6.67 x 2.08 cm)	
Weight	7 oz (200 g)	

TECHNICAL INFORMATION

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the SDC-620 superior dynamic performance, as listed in the specifications. If the power supply voltage is not the +15 VDC nominal value, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage.

So long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The figure below shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.



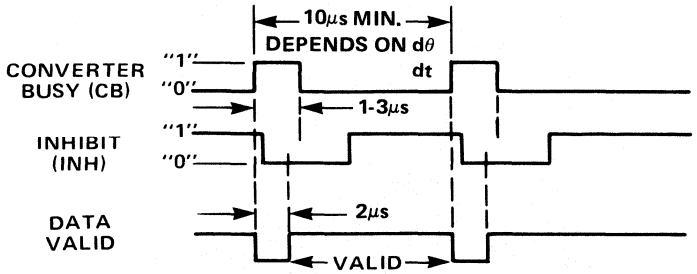
RESPONSE TO A STEP INPUT

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy pulse (CB). The output data change is initiated by the leading edge of the CB pulse. The output becomes stable in less than 2μs, even though the CB pulse may last longer. The converter will ignore an inhibit command applied during the "busy" interval until that interval is over. A simple method of interfacing to a computer is to (a) apply the inhibit, (b) wait 2μs, (c) transfer the data, and (d) release the inhibit.

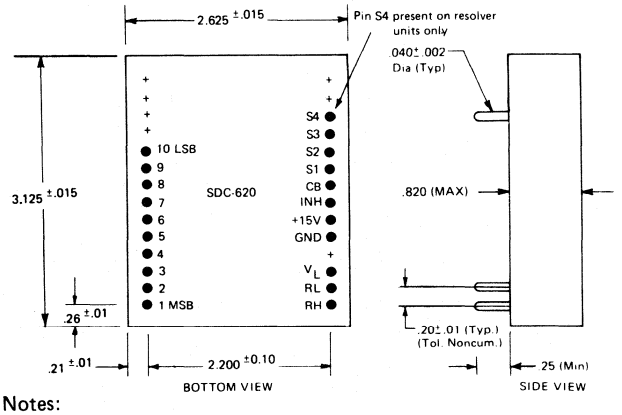
TRANSFORMER INPUT

To prevent damage to the signal and reference input transformers, the maximum voltage should not exceed the specified input voltage by more than 30%. The maximum common mode voltage (DC plus recurrent AC peak) should not exceed 500V.



TIMING DIAGRAM

MECHANICAL OUTLINE



Notes:

1. Pin material is electrosoldered brass per MIL-F-14072, M222.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.

ORDERING INFORMATION

If a socket is required, order socket number 9010.

SDC–620–H–1

- Temperature Range (Operating):
  - 1 = –55°C to +105°C
  - 3 = 0°C to +70°C
- Signal Input Voltage and Frequency:
  - H = 90V L-L, 400 Hz (Synchro or Resolver)
  - I = 90V L-L, 60 Hz (Synchro only)
  - M = 26V L-L, 400 Hz (Resolver only)
  - L = 11.8V L-L, 400 Hz (Synchro or Resolver)
- Input Type:
  - SDC = Synchro
  - RDC = Resolver

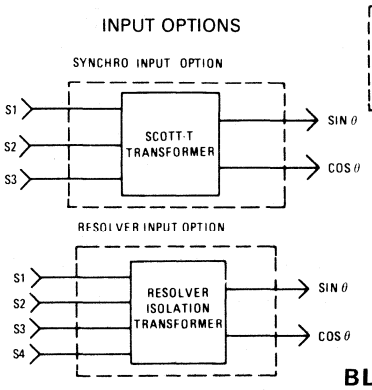
For 60 Hz:

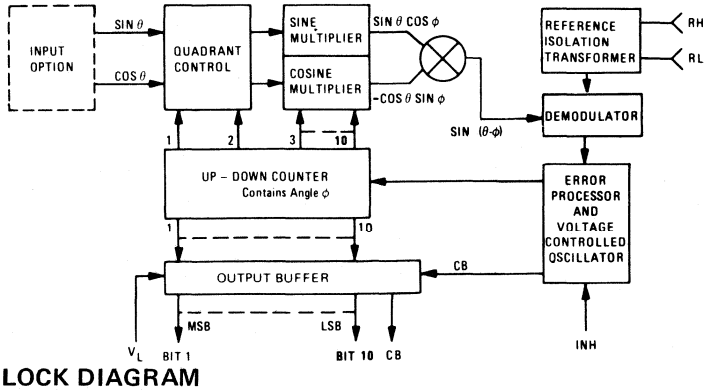
$$G = \frac{100^2 \left(\frac{S}{54} + 1\right)}{S^2 \left(\frac{S}{540} + 1\right)}$$

For 400 Hz:

$$G = \frac{490^2 \left(\frac{S}{256} + 1\right)}{S^2 \left(\frac{S}{2560} + 1\right)}$$

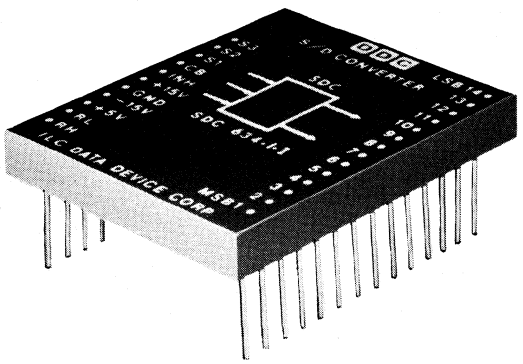
NOMINAL OPEN LOOP TRANSFER FUNCTIONS





BLOCK DIAGRAM

10, 12 OR 14 BIT S/D OR R/D CONVERTER
Low Profile; Internal Transformers



DESCRIPTION

The SDC 630, 632 and 634* series are low cost, low profile synchro to digital and resolver to digital tracking converters with standard pin configurations. They use a unique control transformer algorithm that provides inherently higher accuracy and jitter-free output. Utilizing a type II servo loop, these converters have no velocity lag up to the specified tracking rate and output data is always fresh and continuously available. Each unit is fully trimmed and requires no adjustments or calibrations in the field.

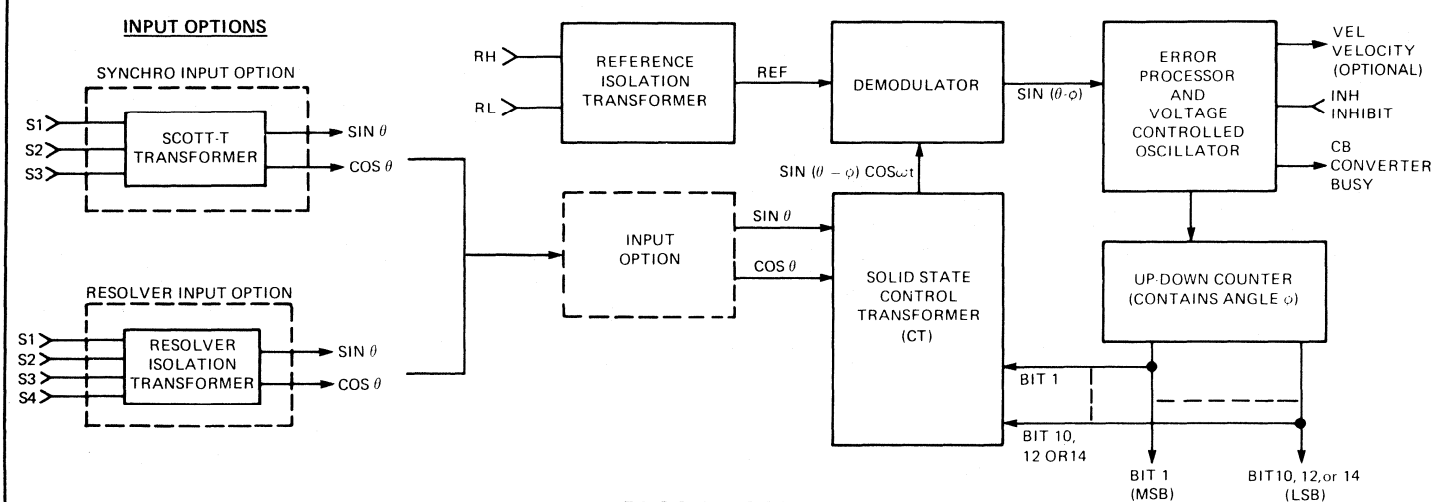
APPLICATIONS

These converters may be used wherever analog angle data from a synchro or resolver must be converted rapidly and accurately to digital form for transmission, storage or analysis. Because these units are extremely rugged and stable, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial, commercial and military applications. Military ground support and avionics uses include ordnance control, radar tracking systems, navigation, and collision avoidance systems.

FEATURES

- *STANDARD LOW PROFILE CONVERTERS WITH OPTIONAL VELOCITY OUTPUT*
- *ACCURACY:*
  10 BIT: ±21 MINUTES
  12 BIT: ±8.5 MINUTES
  14 BIT: ±4 MIN ±0.9 LSB OR ±2.6 MIN (HIGH ACCURACY)
- *SIGNAL AND REF INPUT:*
  INTERNAL TRANSFORMER ISOLATION
  ALL COMMON L-L LEVELS AND FREQUENCIES
- *LOGIC:*
  TTL COMPATIBLE
  PARALLEL BINARY ANGLE OUTPUT
  CONVERTER BUSY AND INHIBIT
- *POWER REQUIRED:*
  ±15V DC AND +5V DC

*Patented



BLOCK DIAGRAM

SPECIFICATIONS

Apply over temperature range, power supply range, reference frequency and amplitude range, ±10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE		
	SDC-630	SDC-632	SDC-634
RESOLUTION	10 bits	12 bits	14 bits
ACCURACY			
Standard Units	±21 min	±8.5 min	±4 min ±0.9 LSB
High Accuracy Option	–	–	±2.6 min
SIGNAL AND REFERENCE INPUT			
Synchro Input*:	Signal Frequency Range	Signal Input Impedance (L-L Balanced, Resistive)	
90V L-L, 400 Hz (Option H)	350–1000 Hz	148 KΩ min	
90V L-L, 60 Hz (Option I)	47–1000 Hz	148 KΩ min	
11.8V L-L, 400 Hz (Option L)	350–1000 Hz	19 KΩ min	
Resolver Input*:			
90V L-L, 400 Hz (Option H)	350–1000 Hz	148 KΩ min	
26V L-L, 400 Hz (Option M)	350–1000 Hz	42 KΩ min	
11.8V L-L, 400 Hz (Option L)	350–1000 Hz	19 KΩ min	
Reference Input*:	Reference Voltage Range	Ref. Input Impedance (Resistive)	
Options H, I	40–150V rms	300 KΩ min	
Options M, L	10–50V rms	80 KΩ min	
*Transformer isolated. Other voltages and frequencies available on special order.			
DIGITAL/INPUT OUTPUT			
Logic Type	TTL		
Inhibit Input (INH) Loading	Logic "0" inhibits 0.2 Std. TTL loads plus 18 KΩ min pull-up resistor to +5V supply		
Outputs			
Type	Low power Schottky (can drive remote loads)		
10, 12, or 14 Parallel Data Bits	Natural binary angle; positive logic		
Converter Busy (CB)	0.5 to 1.5μsec positive pulse. Data changes on leading edge for SDC-630, and on trailing edge for SDC-632/634.		
Drive Capability	2 Std. TTL loads (5 Std. load capability available on special order-consult factory)		
VELOCITY OUTPUT (ON SPECIAL ORDER ONLY)			
Type	Derived from an op-amp with low impedance output Positive output for increasing angle		
Voltage Range	±10V min		
Scale Factor (For SDC-634 – Others on Request)			
Options H, M, and L	.6V per rps nominal (10V = 15 rps)		
Option I	3.3V per rps nominal (10V = 2.7 rps)		

DYNAMIC CHARACTERISTICS	MIN	TYP	MIN	TYP
Input Rate for Full Accuracy (Min Range)				
Options H, M, L (400 Hz)	0 –50 rps	0–40 rps 60	0–10 rps	15
Option I (60 Hz)	0–12.5 rps	0–10 rps 15	0–1.25 rps	3
Acceleration for 1 LSB Lag				
Options H, M, L (400 Hz)	12,600°/sec² typ	4500°/sec² typ	610°/sec² typ	
Option I (60 Hz)	770°/sec² typ	295°/sec² typ	20°/sec² typ	
Settling Time				
For Normal Tracking (Up to Specified Input Rate)	No lag error	No lag error	No lag error	
For 179° Step Change (Typical Values)				
Options H, M, L (400 Hz)				
Settling to 1 LSB	80 msec	90 msec	150 msec	
Settling to Final Value	100 msec	110 msec	200 msec	
Option I (60 Hz)				
Settling to 1 LSB	300 msec	300 msec	800 msec	
Settling to Final Value	500 msec	360 msec	1000 msec	
Velocity Constant (Type II servo loop)	$K_V = \infty$	$K_V = \infty$	$K_V = \infty$	

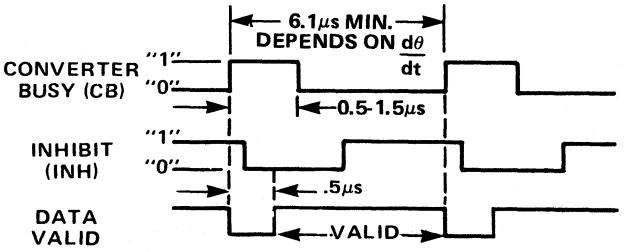
PARAMETER	VALUE		
	SDC-630	SDC-632	SDC-634
DYNAMIC CHARACTERISTICS (Cont'd)			
Acceleration Constant (Nominal Values)			
Options H, M, L (400 Hz)	K_a = 36,000 sec²	K_a = 54,000 sec²	K_a = 27,800 sec²
Option I (60 Hz)	K_a = 2,200 sec²	K_a = 3,600 sec²	K_a = 900 sec²
POWER SUPPLIES			
Nominal Voltage	+15V Supply	–15V Supply	+5V Logic Supply
Voltage Range	+11 to +16.5V	–11 to –16.5V	+4.5 to +5.5V
Max. Voltage Without Damage	+18V	–18V	7V
Current			
SDC-630 (632) Typical	8 mA (4)	18 mA (18)	80 mA (80)
Maximum	13 mA (6)	30 mA (30)	120 mA (120)
SDC-634 Typical	10 mA	20 mA	100 mA
Maximum	15 mA	30 mA	150 mA
TEMPERATURE RANGES			
Operating			
–1 Option	–55°C to +105°C		
–3 Option	0°C to +70°C		
Storage	–55°C to +125°C		
PHYSICAL CHARACTERISTICS			
Size (Encapsulated Module)	3.125 x 2.625 x 0.43 inch (7.94 x 6.67 x 1.07 cm)		
Weight	4 oz (113 g)		

TECHNICAL INFORMATION

TIMING

The figure below shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy impulse (CB). The CB is a positive pulse 0.5 to 1.5μsec long. Data changes on the leading edge of the CB pulse, and data can be transferred 0.5μsec after the leading edge.

The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the inhibit is applied. The converter will ignore an inhibit applied during the "busy" interval until that interval is over. Timing is as follows: (a) apply the inhibit, (b) wait 0.5μs, (c) transfer the data, and (d) release the inhibit. Extra CB pulses will not occur if the input angle changes while the counter is locked by the INH.

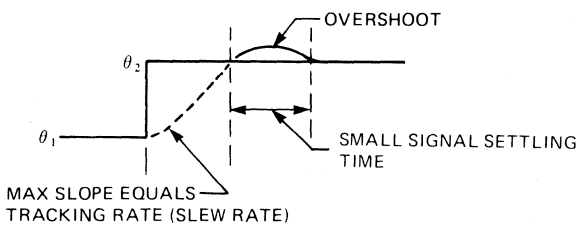


TIMING DIAGRAM

DYNAMIC PERFORMANCE

A type II servo loop (KV = ∞) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltages are not the +15 VDC nominal values, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage. The +15 V supply voltage will determine the positive maximum velocity, and the −15 V supply voltage will determine the negative maximum velocity.

So long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The figure shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to a final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT

The nominal open loop transfer function is given by

$$G = \frac{A^2 \left(\frac{S}{B} + 1\right)}{S^2 \left(\frac{S}{10B} + 1\right)}$$

where the parameters A and B are:

		SDC-630	SDC-632	SDC-634
400 Hz	A	190 sec^{-1}	226 sec^{-1}	167 sec^{-1}
	B	91 sec^{-1}	100 sec^{-1}	56 sec^{-1}
60 Hz	A	46 sec^{-1}	58 sec^{-1}	30 sec^{-1}
	B	23 sec^{-1}	26 sec^{-1}	10 sec^{-1}

POWER SUPPLIES

The main power supplies can vary over their specified ranges with no change in the converter specifications except for a proportional change in the maximum tracking rates.

When testing or evaluating the converters, it is advisable to limit the current to each of the three power supplies. Set each limit to 50% greater than the maximum current listed for that supply in the specifications table.

TRANSFORMER INPUT

To prevent damage to the input transformers, the maximum steady state voltage should not exceed the specified input voltage by more than 30%. The maximum common mode voltage (DC plus recurrent AC peak) should not exceed 500 V.

ACCOMMODATING NON-STANDARD INPUT VOLTAGES

The signal and reference input levels of the SDC-630 series can be resistively scaled to accommodate non-standard voltages. A converter should be selected that is the next lower standard voltage and the voltage is then scaled up with resistors in series with the synchro and/or reference inputs.

For a synchro input (SDC), a resistor ^{R}SIG is added in series with S1, S2 and S3, which is determined as follows:

^{R}SIG = 1.11K (New L-L Voltage − Standard Unit Voltage)

That is, 1.11K for each volt above that for which the standard unit is designed.

Example: An SDC-634-L (11.8V) is to be used at 50V L-L

^{R}SIG - 1.11K (50–11.8) = 42.4K

The closest available high grade resistor with a low temperature coefficient of resistance should be used, and the three resistors should be matched to each other as closely as possible. In general, a 0.1% difference will introduce 1.7 arc minutes of additional error due to the effect on $\frac{SIN}{COS}$ ratio relationship.

The ABSOLUTE value of the resistor is not critical.

In the case of the RESOLVER version (RDC), the equation is:

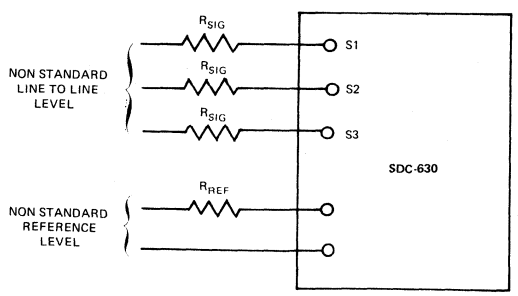
^{R}SIG = 2.2K (New L-L level − Standard Unit L-L level)

The calculated resistors are connected in series with S1 and S2 respectively. Note only two resistors required. The required resistor matching and its effect on accuracy, is the same as for a synchro input (See Figure).

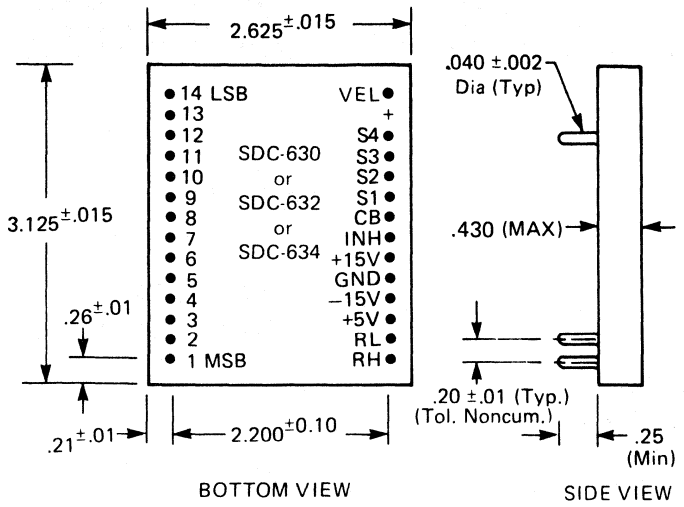
The Reference Voltage treatment is similar, but the value selected is not critical.

^{R}Ref = 2.8K (New ref − standard ref)

Here, even a 10% tolerance is adequate.



MECHANICAL OUTLINE



Notes:

1. Pin material is electrosoldered brass per MIL-F-14072, M222.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.
3. Pins 13 and 14 are omitted for SDC-632, and pins 11, 12, 13 and 14 are omitted for SDC-630.
4. Velocity output pin VEL is present only if requested on special order.
5. Pin S4 is present on Resolver units, and omitted on Synchro units.

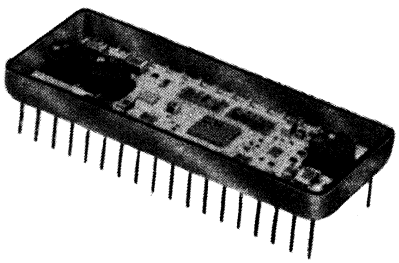
ORDERING INFORMATION

If a socket is required, order socket number 9010.

SDC–634–H–1–a–R

- R = Enhanced reliability
- High Accuracy Version
  ±2.6 Minutes (SDC-634 only)
- Temperature Range (operating):
  1 = –55° C to +105° C
  3 = 0° C to +70° C
- Signal Input Voltage and Frequency:
  H = 90V L-L, 400 Hz (Synchro or Resolver)
  I = 90V L-L, 60 Hz (Synchro only)
  M = 26V L-L, 400 Hz (Resolver only)
  L = 11.8V L-L, 400 Hz (Synchro or Resolver)
- Resolution:
  634 = 14 bits
  632 = 12 bits
  630 = 10 bits
- Input Type:
  SDC = Synchro
  RDC = Resolver

TRANSFORMER ISOLATED 14 BIT MONOLITHIC HYBRID S/D AND R/D TRACKING CONVERTERS



DESCRIPTION

The SDC-14510 Monobrid™ Series is a complete 14 Bit synchro to digital or resolver to digital converter with built-in signal and reference transformers for 60 Hz and 400 Hz operation in a single DDIP hybrid package. Most of its circuitry has been incorporated into a custom monolithic chip, thereby greatly reducing parts count inside the hybrid. Because of the internal micro-transformers, the SDC-14510 Monobrid provides greater isolation as well as increased common mode voltages. The Monobrid combination of monolithic and hybrid technologies allows a more sophisticated design with better performance. Power consumption is reduced, reliability is increased and costs are lowered.

Features included in the SDC-14510 Series are 3-state output in two bytes, analog velocity signal, error voltage outputs, broadband input and a transparent latch, which allows the converter to keep tracking even while an Inhibit is being applied.

The SDC-14510 Series is available in two accuracy grades of ±5.3 minutes and ±8.5 minutes. The accuracy is not affected by carrier amplitude variation, because the conversion is ratiometric. Phase sensitive detection in the error loop rejects quadrature and noise. Adjustments and calibration are never required.

Converters from this series are available in either the 360 Hz to 1000 Hz or 47 Hz to 440 Hz frequency ranges. The output angle is a natural binary code, parallel positive logic and TTL compatible. Synchronization to a computer is via a Converter Busy (CB) output and an Inhibit input.

Only one main power supply (+15V DC nominal) is required. The supply can vary from +11V to +16.5V with no degradation in the converter's performance. An external logic power supply (+5V DC) is also required. Except for the TTL 3-state output buffers, internal logic is CMOS, and all logic inputs and outputs are buffered to the external logic level.

APPLICATIONS

With 3-state output and an Inhibit that does not stop the tracking process, the SDC-14510 Series converters are especially suited for bus multiplexing and interfacing with microprocessors. These converters are ideal for use with remotely located and hard to access equipment, where low power requirements, small size, transformer isolation, and high MTBF are required. All units are processed to MIL-STD-883 and are well suited to the most stringent industrial and military applications. In conjunction with other devices, they are easily adapted for closed loop control.

Designed for printed circuit board mounting by standard techniques, the SDC-14510 Series can be readily incorporated into other equipment by the OEM user.

FEATURES

- *INTERNAL TRANSFORMERS FOR 60Hz or 400Hz OPERATION*
- *7 RPS TRACKING*
- *ACCURACY: ±5.3 MINUTES OR ±8.5 MINUTES*
- *3-STATE LATCHED OUTPUTS FOR MICROPROCESSOR DATA BUS*
- *INHIBIT DOES NOT INTERRUPT TRACKING*
- *7.5 TTL LOAD DRIVE CAPABILITY*

*Patented

NOTE: Monobrid® is a registered trademark of ILC Data Device Corporation.

SPECIFICATIONS

Over reference amplitude, temperature and power supply ranges, 10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY	
Normal	±8.5 minutes max (total error)
High Accuracy	±5.3 minutes max (total error)
SIGNAL AND REFERENCE INPUT	
Synchro Input†	
90V L-L, 400 Hz	350-1000 Hz, 148 kΩ min
90V L-L, 60 Hz	47- 440 Hz, 148 kΩ min
11.8V L-L, 400 Hz	350-1000 Hz, 19 kΩ min
Resolver Input†	
26V L-L, 400 Hz	350-1000 Hz, 57 kΩ min
11.8V L-L, 400 Hz	350-1000 Hz, 26 kΩ min
Reference Input†	Voltage Range / Input Impedance
	40-150V rms, 300 k
	10-50V rms, 80 k
†Transformer isolated.	
DIGITAL INPUT/OUTPUT	
Outputs (except CB)	
Logic Type	TTL Compatible; 3-state
Drive Capability	7.5 standard TTL loads
Coding (Bit 1 to 14)	Natural binary angle; positive logic
Output Leakage Current (Off-state)	±20μA
Output Short Circuit Current	−225 mA max (Note 1)
Converter, Busy (CB) (Note 2)	0.5 to 2.0μs positive pulse; leading edge initiates converter update
Drive Capability	1 standard TTL load (−1.6 mA at 0.4V)
Logic Type	TTL compatible CMOS
Inputs	
Inhibit (INH)	Logic "0" inhibits
Loading	Z in ⩾ 25 kΩ pull-up resistor to +5V
Enables (EN-M and EN-L)	Logic "0" enables
	Logic "1" off-state
High Level Input Current	20 μA at 2.7V
Low Level Input Current	0.2 mA at 0.4V
Output Enable and Disable Time	50 ns max
NOTE 1: Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.	
NOTE 2: CB and CB' are the same signals. The only difference being CB' is a 3-state output enabled by EN-M.	
ANALOG OUTPUTS	
Internal DC Reference (V)	+15V DC/2 ≅ 7.5V nominal
Unfiltered DC Error Voltage (D)	−6.5 mV DC average per LSB of error
Filtered DC Error Voltage (E)	−1V DC per + LSB of error (±3 LSB range)
DYNAMIC CHARACTERISTICS	
Input Rate	
At 400 Hz	0 to 7 rps min
At 60 Hz	0 to 2 rps min
Velocity Constant	$K_v = \infty$ (type II servo loop)
Acceleration Constant	
At 400 Hz	Ka = 11,800 sec^{-2} nominal
At 60 Hz	Ka = 240 sec^{-2} nominal
Settling Time	
For 179° Step Change	
At 400 Hz	270 ms typ to 1 LSB
	320 ms max to final value
At 60 Hz	600 ms typ to 1 LSB
	650 ms max to final value
TEMPERATURE RANGES	
Operating	
−1XX	−55°C to +125°C
−3XX	0°C to +70°C
Storage	−55°C to +135°C
POWER SUPPLIES	+15V DC / +5V DC
Nominal Voltage	
Voltage Range	+11 to +16.5V / +4.5 to +5.5V
Absolute Max. Voltage	+18V / +7V
Current	15 mA max / 65 mA typ, 110 mA max
PHYSICAL CHARACTERISTICS	
Type	36 pin Double DIP
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3mm)
Weight	1 oz. max (28g)

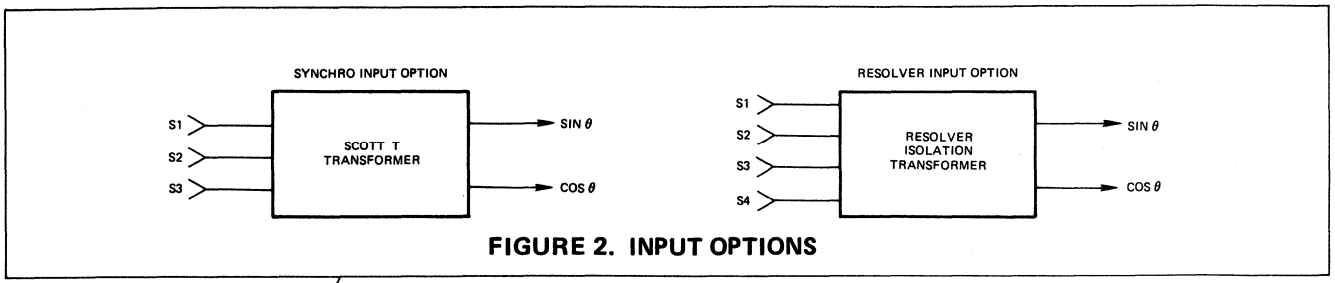


FIGURE 2. INPUT OPTIONS

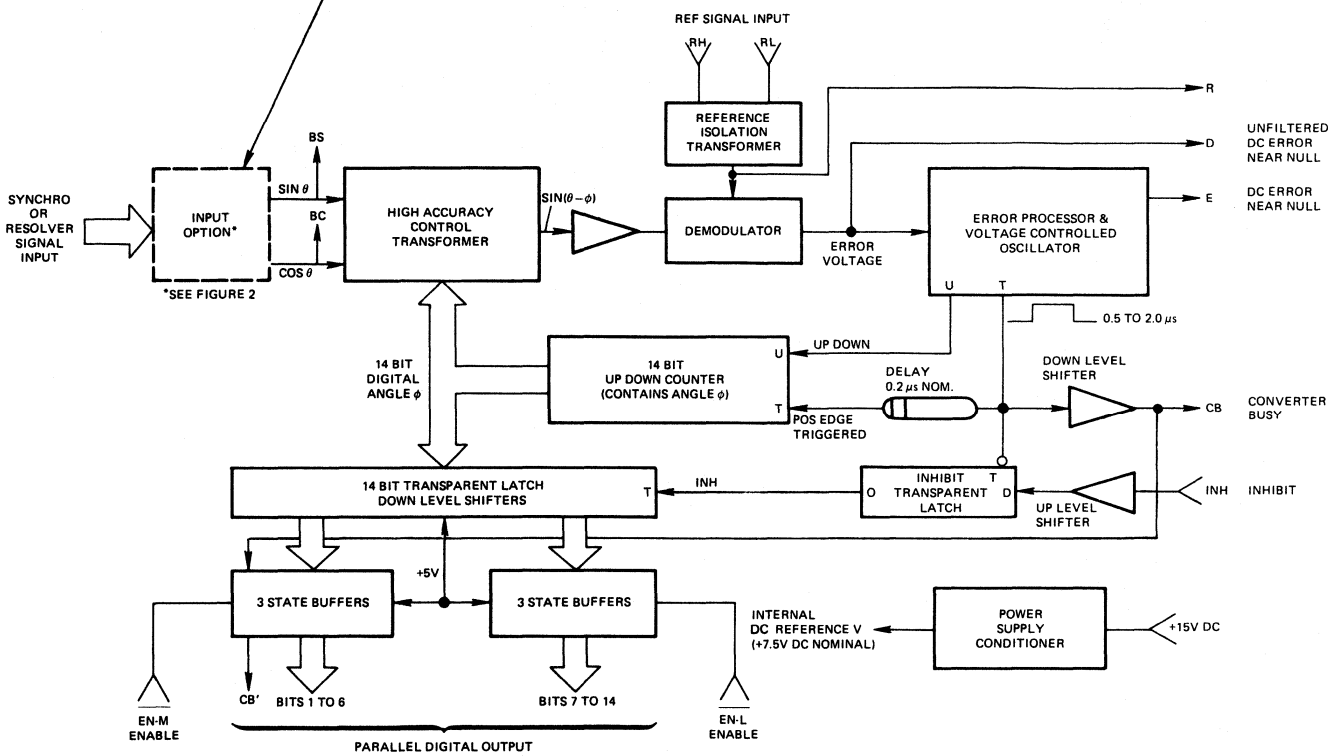


FIGURE 1. SDC-14510 SERIES BLOCK DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION

The circuit shown in the SDC-14510 block diagram, Figure 1, consists of three main parts: the signal input option; a feedback loop whose elements are the control transformer, demodulator, error processor, and up-down counter; and digital interface circuitry including various latches and buffers.

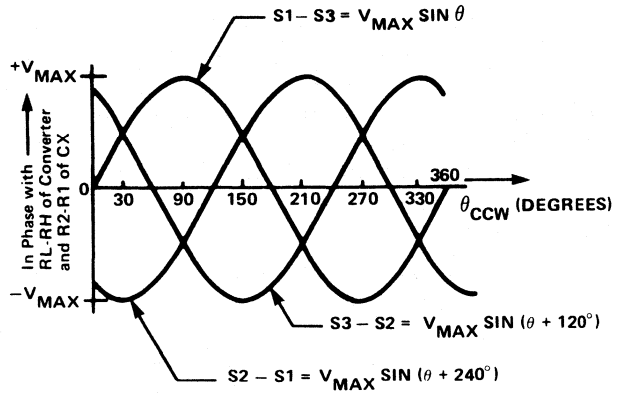
The input options accept a synchro or resolver input and produce a resolver type output for the control transformer. In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The internal converter operates with signals in resolver format, $\sin\theta \cos\omega t$ and $\cos\theta \cos\omega t$. Synchro signals are of the form $\sin\theta \cos\omega t$, $\sin(\theta + 120°)\cos\omega t$, and $\sin(\theta + 240°)\cos\omega t$. Diagrams on the following page show synchro and resolver signals as a function of the angle θ.

The feedback loop produces a 14 bit digital angle Φ which tracks the analog input angle θ to within the specified accuracy of the converter. The control transformer performs the following trigonometric computation:

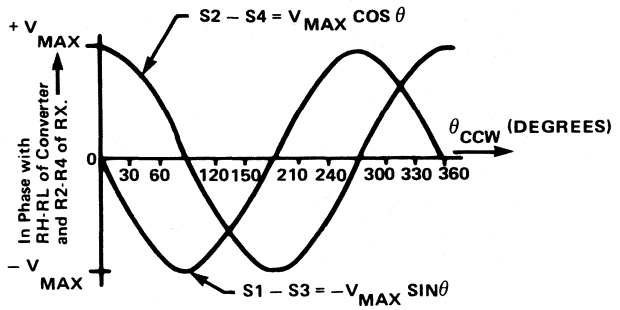
$$\sin(\theta - \Phi) = \sin\theta \cos\Phi - \cos\theta \sin\Phi$$

where θ is the angle representing the synchro or resolver shaft position, and Φ is the digital angle contained in the up-down counter in the converter. The tracking process consists of continually adjusting Φ to make $(\theta - \Phi) \rightarrow 0$, so that Φ will represent the shaft position θ.

The output of the demodulator is an analog DC level proportional to $\sin(\theta - \Phi)$. The error processor integrates this $\sin(\theta - \Phi)$ error signal and the output of the integrator is used to control the frequency of a voltage controlled oscillator. This oscillator produces "clock" pulses which are accumulated by the up-down counter. The up-down counter is functionally an incremental integrator. Therefore there are two stages of integration, making the converter a Type II tracking servo. There will be no position error due to velocity, because in a Type II servo, the voltage



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2–R4 Excited.

SYNCHRO AND RESOLVER SIGNALS

controlled oscillator always settles to a counting rate which makes $d\Phi/dt$ equal to $d\theta/dt$ without lag. The only errors will be momentary (transient) errors during acceleration or deceleration. The output data will always be fresh and available without lag so long as the maximum tracking rate of the converter is not exceeded.

The digital interface circuitry has three main functions: to latch the output bits during an Inhibit command so that stable data can be read out, to furnish both 14 bit parallel and 3-state data formats, and to act as a buffer between the internal CMOS logic and the external logic level.

Applying an Inhibit command will lock the data in the 14 bit transparent latch without interfering with the continuous tracking of the feedback loop. This is a new feature, since S/D and R/D converters usually lock the up-down counter while an Inhibit is applied. In the SDC-14510 Series Monobrids, therefore, the digital angle Φ is always updated and the Inhibit can be applied for an arbitrary amount of time. The Inhibit transparent latch and the 0.2 μs delay are also parts of the Inhibit circuitry, whose detailed operation is decribed in the Logic Output/Input Section.

When testing or evaluating the converter, it is advisable to limit the power supply currents as follows:

+15V Supply Limit at 70 mA.
+ 5V Supply Limit at 150 mA.

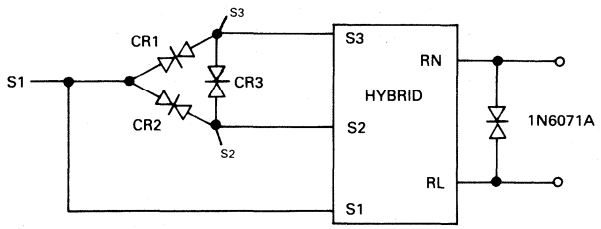
Analog circuits inside the SDC-14510 module are referenced to an internal DC reference level V which rides at 7.5V nominal with respect to the external ground (GND). V should not be connected to the external ground.

SIGNAL INPUTS

The recurrent AC peak + DC common mode voltage should not exceed the following values:

Input	Common Mode Maximum	Max Transient Peak Voltage (Normal Mode)
11.8V L-L	500V Peak	150V
26 V L-L	500V Peak	150V
90 V L-L	500V Peak	500V
Reference	500V Peak	500V

90V line-to-line synchros may have voltage transients, which exceed the 500V specification listed above. These transients can destroy the thin film input resistor network in the hybrid. These modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro voltages are switched on or off. For instance, a 1000V transient can be generated when the primary of a CX or TX driving a synchro input is opened.



CR1, CR2 and CR3 are 1N6068A, 100V bipolar transient voltage suppressors or equivalent.

CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

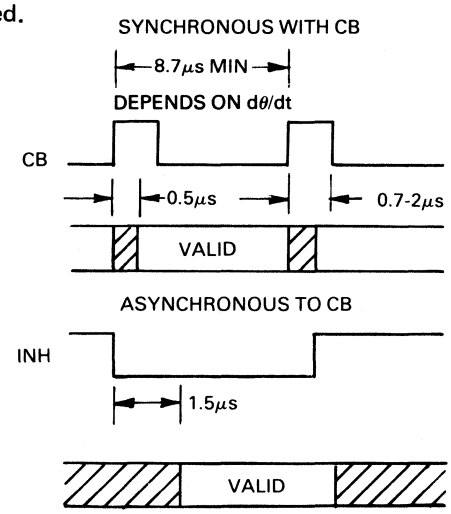
LOGIC OUTPUTS AND INPUTS

Logic outputs consist of 14 parallel data bits, Converter Busy (CB) and CB', which is a 3-state buffered CB. The CB output is a positive 0.5–2.0 μs pulse, and data changes

about 0.2 μs after the leading edge of the pulse because of an internal delay (see Figure 1). Data is valid 0.5 μs after the leading edge of a CB.

The parallel digital outputs are gated to provide an 8 and a 6 line byte for microprocessor bus interfacing. When the Enables for the gates are at logic 0, the gate outputs are at normal logic 1 or 0, depending on the bit state. When the Enables are at logic 1, the gate outputs are high impedance and the microprocessor sees an essentially open line. Outputs are valid 50 ns after an Enable is driven to logic 0. For 14 bit parallel output operation when the 3-state feature is not used, the Enable lines should be tied to logic 0. Outputs are in the high impedance state 50 ns after an Enable is driven to logic 1.

The Inhibit (INH) logic input locks the 14 bit transparent latch so that the bits will remain stable while data is being transferred (see Figure 1). The output is stable 0.5 μs after the Inhibit is driven to logic 0. A logic 0 at the T input locks the 14 bit latch, and a logic 1 allows the bits to change. The purpose of the INH transparent latch is to prevent the transmission of invalid data when there is an overlap between the CB and INH. While the counter is not being updated the CB is at logic 0 and the INH latch is transparent. When the CB goes to logic 1 the INH latch is locked. If a CB occurs after an INH has been applied, the 14 bit latch will remain locked and its data cannot change until the CB returns to logic 0. If an INH is applied during a CB pulse, the 14 bit latch will not lock until the CB pulse is over. The purpose of the 0.2 μs delay is to prevent a race condition between the CB and the INH in which the up-down counter begins to change just as an INH is applied. Since the SDC-14510 Series contain CMOS devices, standard CMOS handling procedure should be followed.



TIMING DIAGRAM

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. The output data change is initiated by the leading edge of the CB pulse, delayed by the 0.2μs (nominal) delay. The output becomes stable in less than 0.5μs even though the CB pulse may last longer. Data transfer can be made synchronous with the leading edge of CB, delayed by 0.5μs. (See Timing Diagram.)

An Inhibit input, regardless of its duration, does not affect converter update. A simple method of interfacing to a computer, asynchronous to CB pulse, is to (a) apply the inhibit, (b) wait 1.5 μs min., (c) transfer the data and (d) release the inhibit.

ANALOG OUTPUTS

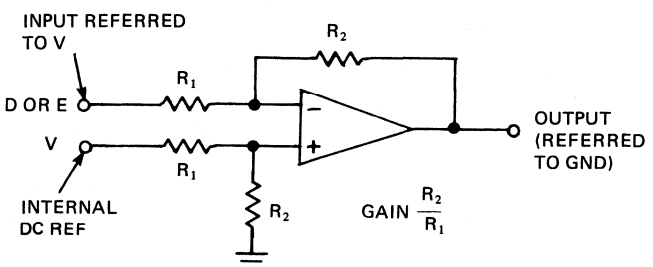
The analog outputs are V, D and E. V is an internal DC reference, +7.5V DC nominal. The outputs D and E ride on the reference voltage V, and should be measured with respect to V. Outputs can swing ±5V when the voltage level of the +15V power supply is +15V. The output swing changes proportionally if the level is not at +15V.

Output D is the unfiltered DC error voltage sin $(\theta - \Phi)$ near the null point. Its average amplitude at nominal input voltage for +1 LSB of error (equivalent to $(\theta - \Phi) = 0.022^\circ$) is −6.5 mV average.

E is a DC voltage proportional to the error $(\theta - \Phi)$ near the null point, with −1V DC output per + LSB of error.

Maximum loading for each analog output is 1.0 mA. Outputs D and E are not required for nomal operation of the converter.

The figure shows a difference circuit which may be used to reference the analog outputs with respect to external ground instead of the internal reference V.

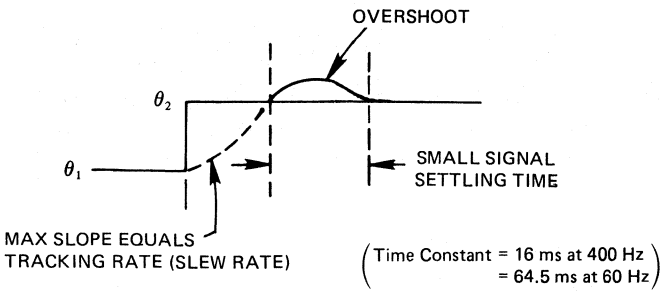


DIFFERENCE CIRCUIT FOR ANALOG OUTPUTS

The outputs D and E are not closely controlled or characterized. Consult factory for further information.

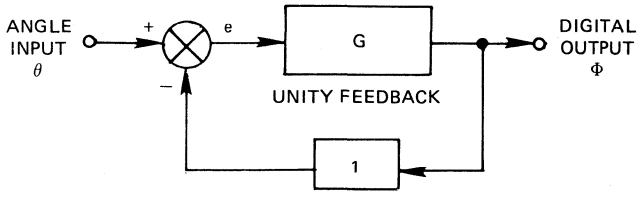
DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the SDC-14510 Series superior dynamic performance, as listed in the specifications. As long as the maximum tracking rate of 7 rps is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The response to a step input is shown below. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT

The loop dynamics of the tracking converter is shown in the diagram. The closed loop transient response is nominally critically damped. All loop dynamics can be determined from the diagram and formulas listed.



FOR 60 Hz

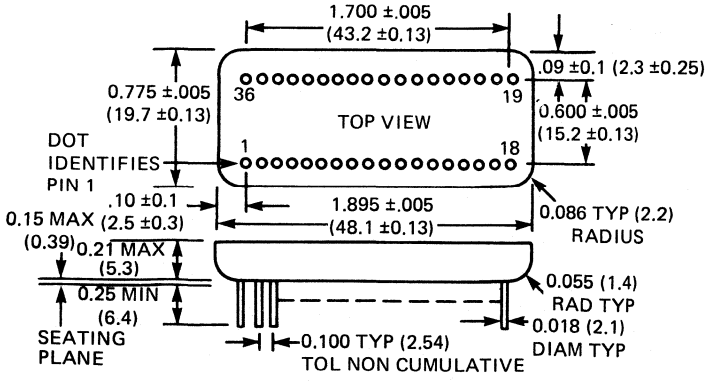
$$G = \frac{15.5^2\left(\frac{S}{9.7} + 1\right)}{S^2\left(\frac{S}{97} + 1\right)^2}$$

FOR 400 Hz

$$G = \frac{62^2\left(\frac{S}{39} + 1\right)}{S^2\left(\frac{S}{390} + 1\right)^2}$$

CONVERTER LOOP DYNAMICS

MECHANICAL OUTLINE
36 PIN DOUBLE DIP



NOTES:
1. Dimensions shown are in inches. (millimeters)
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-883, Method 2003.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.
7. This unit contains CMOS devices; standard stacic handling procedure should be followed.

RELIABILITY

MTBF values are very high because the use of custom monolithics greatly decreases the number of active components, because thin film resistor networks are used, and because of careful thermal design. Summaries of MTBF calculations are available on request.

All SDC-14510's are built in accordance with requirements of MIL-STD-883. Screening is based on requirements of Method 5008 (burn in is optional). To specify preburn in tests and burn in, see ordering information. The computed MTBF is 3,800,000 hours, Ground Benign, at 25°C.

PIN CONNECTION TABLE

PIN	FUNCTION		PIN	FUNCTION
	Resolver	Synchro		
1	S1	S1	19	RH (Ref. High)
2	S2	S2	20	RL (Ref. Low)
3	S3	S3	21	R (Ref)
4	S4	N.C.	22	E (Filtered DC Error Out)
5	Bit 1 MSB		23	CB'
6	Bit 2		24	CB (Converter Busy)
7	Bit 3		25	$\overline{\text{EN-L}}$ (Enable, Bits 7 to 14)
8	Bit 4		26	$\overline{\text{EN-M}}$ (Enable, Bits 1 to 6)
9	Bit 5		27	D (Unfiltered DC Error Out)
10	Bit 6		28	+5V (Logic Voltage Input)
11	Bit 7		29	GND
12	Bit 8		30	N.C.
13	Bit 9		31	N.C.
14	Bit 10		32	+15V (Power Supply In)
15	Bit 11		33	INH (Inhibit)
16	Bit 12		34	V (Internal DC reference)
17	Bit 13		35	BC (Buffered Cos)
18	Bit 14 LSB		36	BS Buffered Sin)

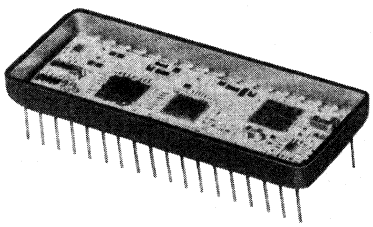
NOTES: BS and BC pins are used in other applications.

ORDERING INFORMATION

SDC – 1451X – XXX

- Input Type: SDC = Synchro, RDC = Resolver
- Family Code
- Input: 0 = 11.8V, 400 Hz, Synchro, 26V Ref. 1 = 90V, 400 Hz, Synchro, 115V Ref. 2 = 90V, 60 Hz, Synchro, 115V Ref. 4 = 26V, 400 Hz, Resolver, 26V Ref. 5 = 11.8V, 400 Hz, Resolver, 26V Ref.
- Temperature Range: 1 = –55°C to +125°C, 3 = 0° to +70°C
- Rel. Grade: 0 = Std., 1 = 883B
- Accuracy: 2 = ±8.5', 3 = ±5.3'

16 BIT MONOLITHIC HYBRID S/D AND R/D TRACKING CONVERTERS



DESCRIPTION

The SDC-14520 Monobrid® Series* is a complete 16 bit synchro-to-digital or resolver-to-digital converter contained in a single hybrid module. Most of its circuitry has been incorporated into a custom designed monolithic chip, thereby greatly reducing parts count inside the hybrid. The Monobrid® combination of monolithic and hybrid technologies allows a more sophisticated design with better performance and additional features to fit inside a standard 36 pin DDIP hybrid package. Power consumption is reduced, reliability is increased, and costs are lower.

New features found in the SDC-14520 Series are 3-state output in two bytes; ± 1.3 minute accuracy; transparent latch, which allows continuous tracking while an inhibit is applied; and control transformer capability. Included are other innovative features, found in recent DDC Synchro Converters, such as analog velocity output, error voltage output, solid state signal and reference isolation, broadband input and capability to accommodate non-standard line-to-line voltage levels.

The SDC-14520 Series is available in accuracy grades of ±1.3, ±2.6 and ±5.3 minutes. The accuracy is not affected by carrier amplitude variation because the conversion is ratiometric. Phase sensitive detection in the error loop rejects quadrature and noise. Adjustments and calibration are never required.

The SDC-14520 Series accepts broadband inputs: 360 to 1000 Hz or 47 to 1000 Hz. The input signal isolation is solid state and the internal differential solid state input has high common mode rejection.

Output angle is natural binary code, parallel positive logic, and TTL/CMOS compatible. Synchronization to a computer is via a Converter Busy output and an Inhibit input.

Only one main power supply is required. Its +15V DC nominal level can range from +11 to +16.5 volts with no degradation in performance. The SDC-14520 is also connected to the external logic power supply. Internal logic is CMOS, and all logic inputs and outputs are buffered to the external logic level. TTL or any external CMOS logic level between +4.5V and the +15V supply level can be accomodated.

APPLICATIONS

With three-state output and an Inhibit that does not stop the tracking process, SDC-14520 Series converters are especially suited for bus multiplexing and interfacing with microprocessors. These converters are ideal for remotely located and hard to access equipment where low power requirements, small size, and high MTBF are critical. All units are processed to MIL-STD-883. They are well suited to the most stringent and severe industrial or military and avionics applications. In conjunction with other devices, they are easily adapted for closed loop control.

Designed for printed circuit board mounting by standard techniques, the SDC-14520 Series can be readily incorporated into other equipment by the OEM user. Because of their low cost, they are competitive with discrete S/D converters in many applications.

FEATURES

- *LOW POWER: 300 mW TYPICAL*
- *ACCURACY: ±1.3 MINUTES*
- *3-STATE LATCHED OUTPUTS FOR MICROPROCESSOR DATA*
- *USEABLE AS CONTROL TRANSFORMER (CT)*
- *INHIBIT DOES NOT INTERRUPT TRACKING*
- *LOGIC: TTL AND CMOS COMPATIBLE 16 BIT PARALLEL BINARY ANGLE*

*Patented

Note: Monobrid® is a registered trademark of ILC Data Device Corporation.

SPECIFICATIONS

Over reference amplitude, temperature and power supply ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	16 bits
ACCURACY:	
–XX3 Accuracy Options	±5.3 minutes max.
–XX4 (see Ordering	±2.6 minutes max.
–XX5 Information)	±1.3 minutes max.
REFERENCE INPUT	
Carrier Frequency Ranges	
Nominal 400 Hz Units	360-1000 HZ
Nominal 60 Hz Units	47-1000 Hz
Reference Input Characteristics	
Voltage Range	4-130V rms
Input Impedance	250 KΩ min. single ended 500 KΩ min. differential
Common Mode Range	DC common mode plus recurrent AC peak = 210V max.

SYNCHRO/RESOLVER SIGNAL INPUTS
SOLID STATE BUFFER INPUT
Minimum Input Impedance (Balanced)

	Z_{IN} Line to Line	Z_{IN} Each Line to GND
Synchro		
90V L-L	130 KΩ	85 KΩ
11.8V L-L	17.5 KΩ	11.5 KΩ

	Z_{IN} Single Ended	Z_{IN} Differential	Z_{IN} Each Line to GND
Resolver			
90V L-L	175 KΩ	350 KΩ	175 KΩ
26V L-L	50 KΩ	100 KΩ	50 KΩ
11.8V L-L	23 KΩ	46 KΩ	23 KΩ

Common Mode Ranges	
For 90V L-L Input	182V max. } DC Common mode plus
For 26 V L-L Input	60V max. } recurrent AC peak
For 11.8V L-L Input	60V max. }

DIGITAL INPUT/OUTPUT	
Logic Type	TTL/CMOS compatible, depending on logic supply voltage
Outputs:	
16 Parallel Data Bits	Natural binary angle positive logic
Converter Busy (CB)	0.5-2.0 μs positive pulse, leading edge initiates counter update
Drive Capability	1 standard TTL load, 1.6 mA at 0.4V (logic "0") 10 standard TTL loads, 0.4 mA at 2.8V (logic "1") 10μA max. high impedance
Inputs:	
Inhibit Input (INH)	$Z_{IN} \geq 25K\Omega$ pull up resistor to V_L INH – Logic 0 inhibits
Enable, Bits 1 to 8 ($\overline{EN\ MSB}$) }	$\overline{EN\ MSB}$ and $\overline{EN\ LSB}$ – Logic 0 enables
Enable, Bits 9 to 16 ($\overline{EN\ LSB}$) }	Logic 1 high impedance
$\overline{S}$ (Control Transformer)	Logic 0 for use as CT
Logic Type	CMOS Compatible – Logic "0" $\leq 0.3\ V_L$, "1" $\geq 0.7\ V_L$
Accuracy	±4 minutes
Loading	CMOS

PARAMETER	VALUE
VOLTAGE FOLLOWER BUFFER INPUT (DIRECT)	
Input Signal Type	Sin and cos resolver signals referenced to converter internal ground V (not to external GND)
Sin/Cos Voltage Range	1V nominal, 1.15V max.
Max. Voltage Without Damage	15V rms continuous. 100V peak transient
Input Impedance	Z_{IN} > 10 MΩ (transient protected voltage follower)
ANALOG OUTPUTS	
Internal D.C. Reference (V)	+7.5VDC nominal
filtered AC Error Voltage (e)	16 mV rms AC per LSB of error
DC Velocity Voltage ($\dot{\theta}$)	+1 VDC per +0.5 rps at 400 Hz +1 VDC per +0.14 rps at 60 Hz
DYNAMIC CHARACTERISTICS	
Input Rate	
At 400 Hz	0 to 2.5 rps min.
At 60 Hz	0 to .62 rps min.
Velocity Constant	$K_V = \infty$ (No limitation with Type II servo loop)
Acceleration Constant	
At 400 Hz	K_a = 16,000 sec^{-2} nominal
At 60 Hz	K_a = 1000 sec^{-2} nominal
Settling Time	
For 179° Step Change	
At 400 Hz	500 ms max typ to 1 LSB 550 ms max to final value
At 60 Hz	1500 ms typ to 1 LSB 1600 ms max to final value
TEMPERATURE RANGES	
Operating	
–1 option	–55°C to +125°C
–3 option	0°C to +70°C
Storage	–55°C to +135°C
POWER SUPPLIES	
Nominal Voltage	+15 VDC / Logic Supply
Voltage Range	+11 to +16.5V / +4.5V to +15 Supply
Absolute Max Voltage	+18V / +18V
Current or Impedance	15 mA max. / Z_{IN} = 5 KΩ min.
PHYSICAL CHARACTERISTICS	
Type	36 pin double DIP
Size	0.78 x 1.9 x 0.21 inch (19.8 x 48.3 x 5.3 mm)
Weight	1 oz. max (28g)

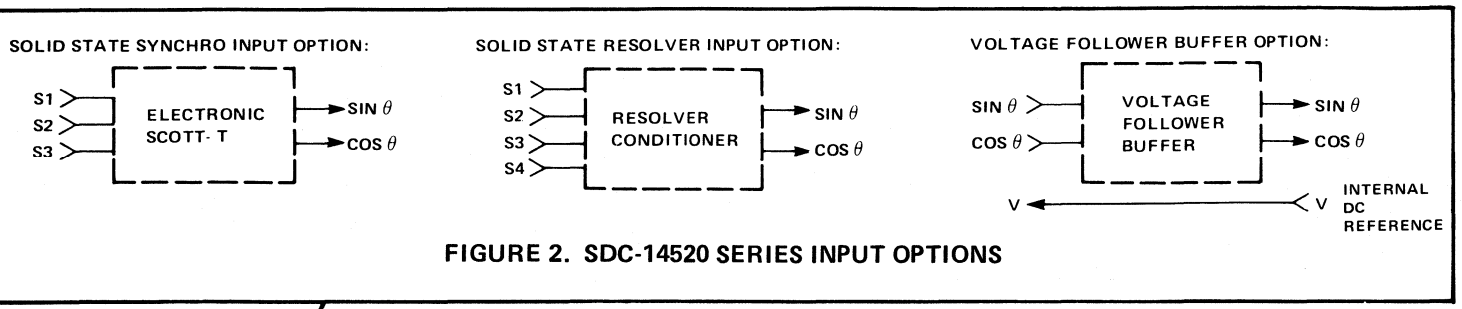


FIGURE 2. SDC-14520 SERIES INPUT OPTIONS

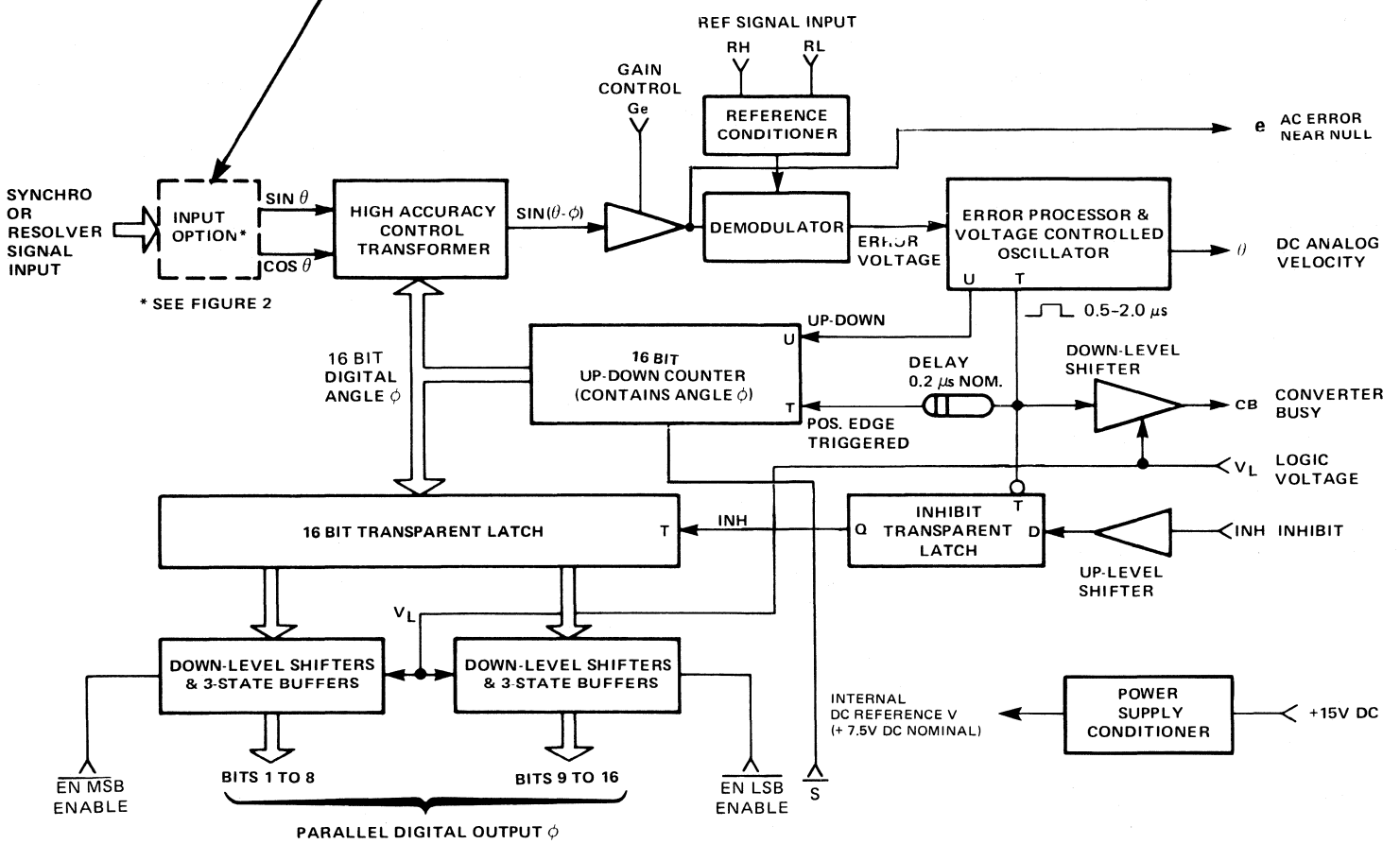


FIGURE 1. SDC-14520 SERIES BLOCK DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION

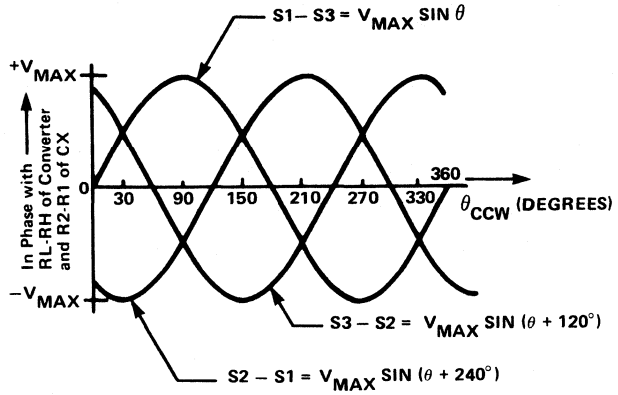
The circuit shown in the SDC-14520 block diagram, Figure 1, consists of three main parts: the signal input option; a feedback loop whose elements are the control transformer, demodulator, error processor, and up-down counter; and digital interface circuitry including various latches and buffers.

The input options accept a synchro or resolver input and produce a resolver type output for the control transformer. The first two options, called solid state synchro and resolver input (see Figure 2), accept synchro and resolver signal inputs directly, and provide signal isolation internally. The third option was designed for direct input, it is a voltage follower buffer and requires an external signal conditioner such as a transformer. Both options, the solid state input and the external transformer isolated buffer, are available for the following standard inputs:

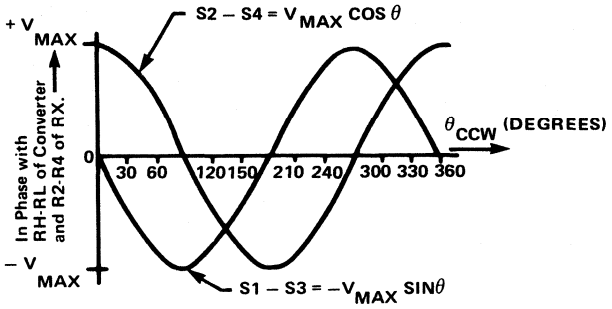
All input options are DC coupled with broadband characteristics up to 1000 Hz. SDC-14520 Series converters are useable to 10 KHz with slight degradation in accuracy-consult factory for further information.

In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The internal converter operates with signals in resolver format, sin θ cos ωt and cos θ cos ωt. Synchro signals are of the form sin θ cos ωt, sin (θ + 120°) cos ωt, and sin (θ + 240°) cos ωt. Diagrams on the following page show synchro and resolver signals as a function of the angle θ.

The feedback loop produces a 16 bit digital angle Φ which tracks the analog input angle θ to within the specified



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

SYNCHRO AND RESOLVER SIGNALS

accuracy of the converter. The control transformer performs the following trigonometric computation:

$$\sin(\theta - \Phi) = \sin\theta \cos\Phi - \cos\theta \sin\Phi$$

where θ is the angle representing the synchro or resolver shaft position, and Φ is the digital angle contained in the up-down counter in the converter. The tracking process consists of continually adjusting Φ to make $(\theta - \Phi) \rightarrow 0$, so that Φ will represent the shaft position θ.

The output of the demodulator is an analog DC level proportional to sin $(\theta - \Phi)$. The error processor integrates this sin $(\theta - \Phi)$ error signal, and the output of the integrator is used to control the frequency of a voltage controlled oscillator. This oscillator produces "clock" pulses which are accumulated by the up-down counter. The up-down counter is functionally an incremental integrator. Therefore there are two stages of integration, making the converter a Type II tracking servo. In a Type II servo, the voltage controlled oscillator always settles to a counting rate which makes $d\Phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available so long as the maximum tracking rate of the converter is not exceeded.

The digital interface circuitry has three main functions: to latch the output bits during an Inhibit command so that stable data can be read out, to furnish both 16 bit parallel and 3-state data formats, and to act as a buffer between the internal CMOS logic and the external logic level.

Applying an Inhibit command will lock the data in the 16 bit transparent latch without interfering with the continuous tracking of the feedback loop. This is a new feature, since S/D and R/D converters usually lock the up-down counter while an Inhibit is applied. In the SDC-14520 Series Monobrids, therefore, the digital angle Φ is always updated and the Inhibit can be applied for an arbitrary amount of time. The Inhibit transparent latch and the 0.2 μs delay are also parts of the Inhibit circuitry, whose detailed operation is described in the Logic Output/Input Section.

When testing or evaluating the converter, it is advisable to limit the power supply currents as follows:

+15V Supply Limit at 20 mA.
Logic Supply V_L at 2 mA + Digital Load at Logic 1.

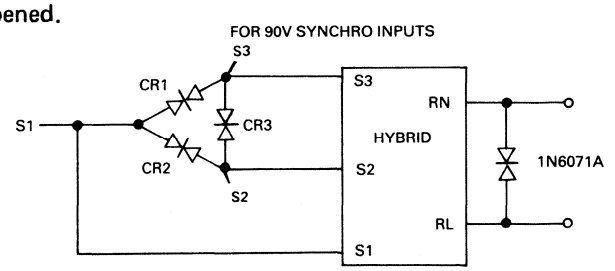
Analog circuits inside the SDC-14520 module are referenced to an internal DC reference level V which rides at +7.5V nominal with respect to the external ground (GND). V should not be connected to the external ground.

SOLID STATE BUFFER INPUTS

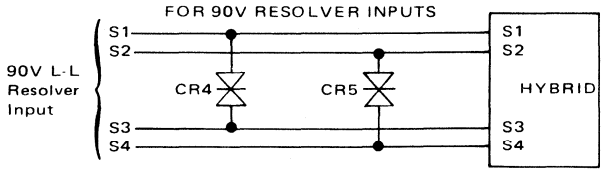
The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection, so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed the following values:

Input	Common Mode Maximum	Max Transient Peak Voltage
11.8V L-L	60V Peak	150V
26 V L-L	60V Peak	150V
90 V L-L	182V Peak	500V
Reference	210V Peak	1000V

90V line-to-line systems may have voltage transients which exceed the 500V specification listed above. These transients can destroy the thin film input resistor network in the hybrid. Therefore, 90V L-L solid state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro or resolver voltages are switched on or off. For instance, a 1000V transient can be generated when the primary of a CX or TX driving a synchro or resolver input is opened.



CR1, CR2 and CR3 are 1N6068A, 100V bipolar transient voltage suppressors or equivalent.



CR 4 and CR5 are 1N6137, 200V bi-polarity transient voltage suppressors or equivalent.

CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

Non-standard synchro and resolver voltage levels can be accommodated with no degradation in the specifications. A unit should be selected whose voltage level 11.8V, 26V, or 90V is the next higher standard level above that of the non-standard signal. To correct the error gradient, a resistor R of the following value in ohms must be added between pins Ge and V:

$$R = \frac{1000}{A\text{-}1} \text{ where } A = \frac{\text{Standard Signal Voltage}}{\text{Non-Standard Signal Voltage}}$$

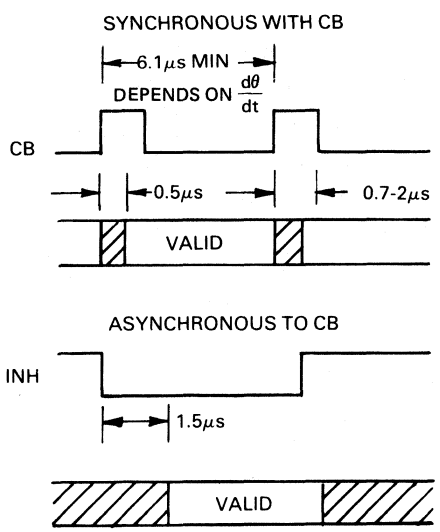
VOLTAGE FOLLOWER BUFFER INPUT

Voltage follower buffer units require a signal isolation transformer or a similar signal conditioner that provides a 1.0V rms nominal resolver type signal referenced to the internal converter ground V. This input option may be preferred in applications where the signal conditioner can be integrated with other components, as in many multiplexed systems.

LOGIC OUTPUTS AND INPUTS

Logic outputs consist of 16 parallel data bits and a Converter Busy (CB). All logic outputs are short-circuit proof to ground and to positive voltages as high as V_L. The CB output is a positive 0.5—2.0 μs pulse, and data changes about 0.2 μs after the leading edge of the pulse because of an internal delay (see Figure 1). Data is valid 0.5 μs after the leading edge of a CB.

The parallel digital outputs are gated to provide two 8 line bytes for microprocessor bus interfacing. When the Enables for the gates are at logic 0, the gate outputs are at normal logic 1 or 0, depending on the bit state. When the Enables are at logic 1, the gate outputs are high impedance and the microprocessor sees an essentially open line. Outputs are valid 0.5 μs after an Enable is driven to logic 0. For 16 bit parallel output operation when the 3-state feature is not used, the Enable lines should be tied to logic 0.



TIMING DIAGRAM

The inhibit (INH) logic input locks the 16 bit transparent latch so that the bits will remain stable while data is being transferred (see Figure 1). The output is stable 0.5 μs after the Inhibit is driven to logic 0. A logic 0 at the T input locks the 16 bit latch, and a logic 1 allows the bits to change. The purpose of the INH transparent latch is to prevent the transmission of invalid data when there is an overlap between the CB and INH. While the counter is not being updated the CB is at logic 0 and the INH latch is transparent. When the CB goes to logic 1 the INH latch is locked. If a CB occurs after an INH has been applied, the 16 bit latch will remain locked and its data cannot change until the CB returns to logic 0. If an INH is applied during a CB pulse, the 16 bit latch will remain locked and its data cannot change until the CB returns to logic 0. If an INH is applied during a CB pulse, the 16 bit latch will not lock until the CB pulse is over. The purpose of the 0.2 μs delay is to prevent a race condition between the CB and the INH in which the up-down counter begins to change just as an INH is applied.

Since the SDC-14520 Series contain CMOS devices standard CMOS handling procedures should be followed.

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. The output data change is initiated by the leading edge of the CB pulse, delayed by the 0.2μs (nominal) delay. The output becomes stable in less than 0.5μs even though the CB pulse may last longer. Data transfer can be made synchronous with the leading edge of CB, delayed by 0.5μs. (See Timing Diagram.)

An Inhibit input, regardless of its duration, does not affect converter update. A simple method of interfacing to a computer, asynchronous to CB pulse, is to (a) apply the inhibit, (b) wait 1.5 μs min., (c) transfer the data and (d) release the inhibit.

ANALOG OUTPUTS

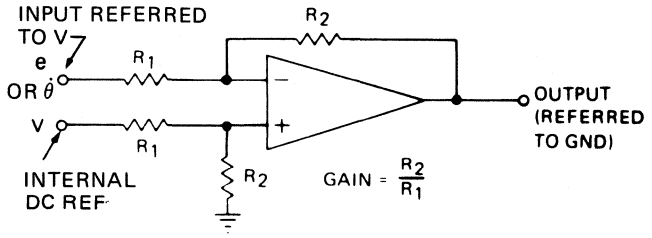
The analog outputs are V, e and $\dot{\theta}$. V is an internal analog DC reference, +7.5 VDC nominal. The outputs e, and $\dot{\theta}$ ride on the DC reference voltage V, and should be measured with respect to V. Outputs can swing ±5V when the voltage level of the +15V power supply is +15V. The output swing changes proportionally if the level is not at +15V.

Output e is the filtered AC error voltage sin $(\theta - \Phi)$ near the null point. Its average amplitude at nominal input voltage for +1 LSB of error (equivalent to $(\theta - \Phi) = 0.0055^\circ$) is 16 mV rms.

$\dot{\theta}$ is a DC voltage proportional to the angular velocity $d\theta/dt = d\Phi/dt$. A +1 VDC output corresponds to +0.5 rps for 400 Hz units, and +0.13 rps for 60 Hz units.

Maximum loading for each analog output is 0.5 mA. Outputs e and $\dot{\theta}$ are not required for normal operation of the converter; V is used as reference with the voltage follower buffer option.

The figure shows a difference circuit which may be used to reference the analog outputs with respect to normal ground instead of the internal DC reference V.



DIFFERENCE CIRCUIT FOR ANALOG OUTPUTS

The output e and $\dot{\theta}$ are not closely controlled or characterized. Consult factory for further information.

USE AS A CT

The SDC-14520 Series S/D can be used as a "Solid State CT". This is analagous to the function of a rotary control transformer except here the *rotary* shaft input is replaced by a *digital* angle. Referring to the equation below, the output is an AC voltage (e) which varies as the sine of the difference between the analog input angle and the digital angle.

$$e = \sin(\theta - \phi)\cos\omega t$$

where θ is the analog angle and ϕ is the digital angle.

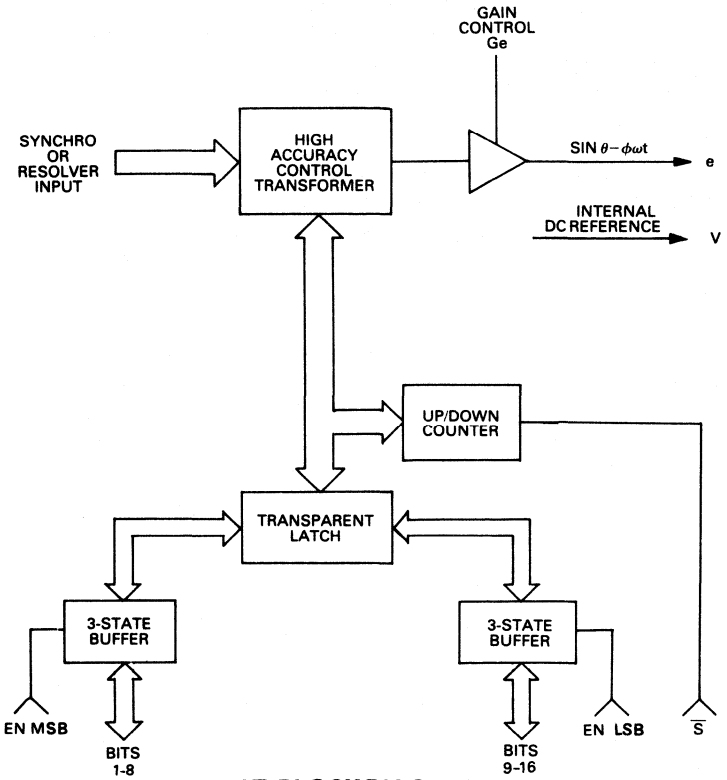
Control transformers are frequently used as error signal generators in closed servo loops. They are useful when digital remote control of a position servo must be accomplished.

The procedure to enable this function is to disable the up-down counter by setting pin 30 ($\overline{S}$) to logic "0" and using the digital output lines (which are bidirectional) as digital inputs. Note that "e" rides on the internal DC reference voltage "V" (approximately 7.5V) and a differential amplifier should be used to reference this signal to real (circuit) ground as shown in the diagram under analog outputs.

The gain control function (Ge) is still operative in CT mode and the effect is the same as when used as an S/D. If you adjust the gain for a lower than nominal line-to-line signal, the error magnitude will remain the same, i.e., 16mV/LSB. If you adjust the gain for a lower signal level but come in with the "nominal" signal level, the error amplitude will be correspondingly gained-up (by the factor $V_{nominal}/V_{lower}$), however the usable error range (dynamic range) is correspondingly reduced.

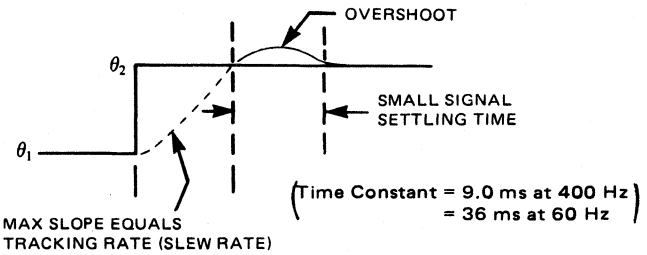
DYNAMIC PERFORMANCE

A type II servo loop ($K_V = \infty$) and very high acceleration constants give the SDC-14520 Series superior dynamic performance, as listed in the specifications.

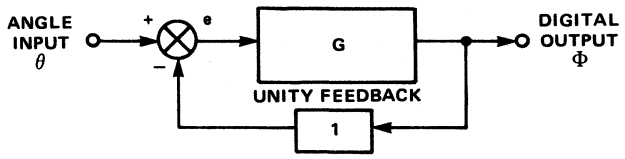


CT BLOCK DIAGRAM

If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The response to a step input is shown below. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT



For 60 Hz

$$G = \frac{33^2\left(\frac{S}{13}+1\right)}{S^2\left(\frac{S}{130}+1\right)\left(\frac{S}{550}+1\right)}$$

For 400 Hz

$$G = \frac{127^2\left(\frac{S}{50}+1\right)}{S^2\left(\frac{S}{500}+1\right)\left(\frac{S}{2000}+1\right)}$$

CONVERTER LOOP DYNAMICS

The loop dynamics of the tracking converter is shown in the diagram. The closed transient response is nominally critically damped. All loop dynamics can be determined from the diagram and formulas listed.

RELIABILITY

MTBF values are very high because the use of custom monolithics greatly decreases the number of active components, because thin film resistor networks are used, and because of careful thermal design. Summaries of MTBF calculations are available on request.

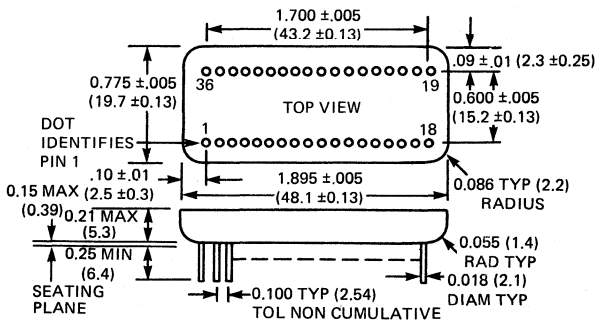
All Model SDC-14520 converters are built in accordance with requirements of MIL-STD-883. Screening is based on the requirements of Method 5004/5008 (burn in is optional). To specify preburn in tests and burn in see ordering information. The computed MTBF value for MIL-STD-883 processing (including burn in) is 6,400,000 hours, Ground Benign, at 25°C.

PIN CONNECTION TABLE

PIN	FUNCTION		
	Solid St. Resolver	Solid St. Synchro	Volt. Fol. Buffer
1	S1	S1	NC
2	S2	S2	COS
3	S3	S3	SIN
4	S4	NC	NC
5	Bit 1 MSB		
6	Bit 2		
7	Bit 3		
8	Bit 4		
9	Bit 5		
10	Bit 6		
11	Bit 7		
12	Bit 8		
13	Bit 9		
14	Bit 10		
15	Bit 11		
16	Bit 12		
17	Bit 13		
18	Bit 14		
19	RH (Ref High)		
20	RL (Ref Low)		
21	Bit 15		
22	Bit 16 LSB		
23	$\dot{\theta}$ (Analog Velocity Out)		
24	CB (Converter Busy)		
25	$\overline{\text{EN LSB}}$ (Enable, Bits 9 to 16)		
26	$\overline{\text{EN MSB}}$ (Enable, Bits 1 to 8)		
27	e (AC Error Out)		
28	V_L (Logic Voltage Input)		
29	GND		
30	$\overline{S}$		
31	Ge (Gain Control)		
32	+15V (Power Supply In)		
33	INH (Inhibit)		
34	V (Internal DC Reference)		
35	BC (Buffered Cos)		
36	BS (Buffered Sin)		

NOTES:
BS and BC pins are used in other applications

MECHANICAL OUTLINE
36 PIN DOUBLE DIP



NOTES
1. Dimensions shown are in inches. (millimeters)
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

ORDERING INFORMATION

SDC-1452X – X X X

Accuracy:
3 = ±5.3′
4 = ±2.6′
5 = ±1.3′

Rel. Grade 0 = Std.
1 = 883

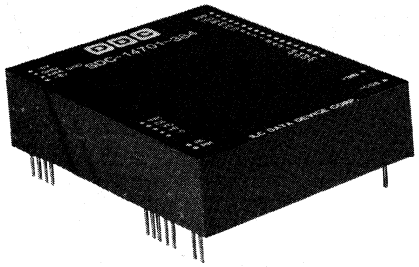
Temperature (operating):
1 = –55°C to +125°C
3 = 0°C to +70°C

Input:
0 = 11.8V, 400 Hz, Synchro
1 = 90V, 400 Hz, Synchro
2 = 90V, 60 Hz, Synchro
4 = 26V, 400Hz, Resolver
5 = 11.8V, 400 Hz, Resolver
6 = 90V, 400 Hz, Resolver
7 = 1V, 400 Hz, Resolver (Direct)
8 = 1V, 60 Hz, Resolver (Direct)

Family Code

Input Type:
SDC = Synchro
RDC = Resolver
XDC = Direct Input (1V)

SDC-14700*



5 DECADE SYNCHRO AND RESOLVER TO BCD CONVERTER

DESCRIPTION

The SDC-14700 converter is a pin programmable, high resolution (0.01°) synchro and resolver to BCD tracking converter. It continuously converts 3 wire synchro or 4 wire resolver information into BCD angle format, at rates up to 180° per second. Its operating frequency range is 47 Hz to 1200 Hz. The unit is available in accuracy grades of ±0.03° and ±0.05°.

An SDC-14701 converter, which operates with a 2 V signal, is also available. The SDC-14701 allows for the use of an inexpensive standard 400 Hz, 26/11.8 V or 26/12.6 V resolver at 60 Hz reference.

Both the SDC-14700 and the SDC-14701 are equipped with a ±2° offset adjust for system zeroing (Figure 1).

Digital outputs are CMOS and TTL compatible. The unique control transformer algorithm used in these units provide for inherently higher accuracy and jitter free output. Utilizing a type II servo loop, the converter has no velocity lag up to 180° per second, and the output data is always fresh and continuously available. Each unit is factory trimmed and requires no field adjustments or calibrations.

APPLICATIONS

The broad capabilities of the SDC-14700 and the SDC-14701 make them cost effective devices for use in systems where analog angle information must be converted into accurate high resolution BCD data. They are suitable for rugged industrial and commercial applications. Military uses include ground support and avionics, such as ordance control, radar tracking systems, navigation and collision avoidance systems.

FEATURES

- *HIGH RESOLUTION: 0.01° (5 DECADE)*
- *HIGH ACCURACY: ±0.03° OR ±0.05°*
- *PIN PROGRAMMABLE: ACCEPTS ALL STANDARD SYNCHROS OR RESOLVERS*
- *OFFSET ADJUST FOR SYSTEM ZEROING*
- *FREQUENCY RANGE: 47 Hz TO 1200 Hz*

*Patented

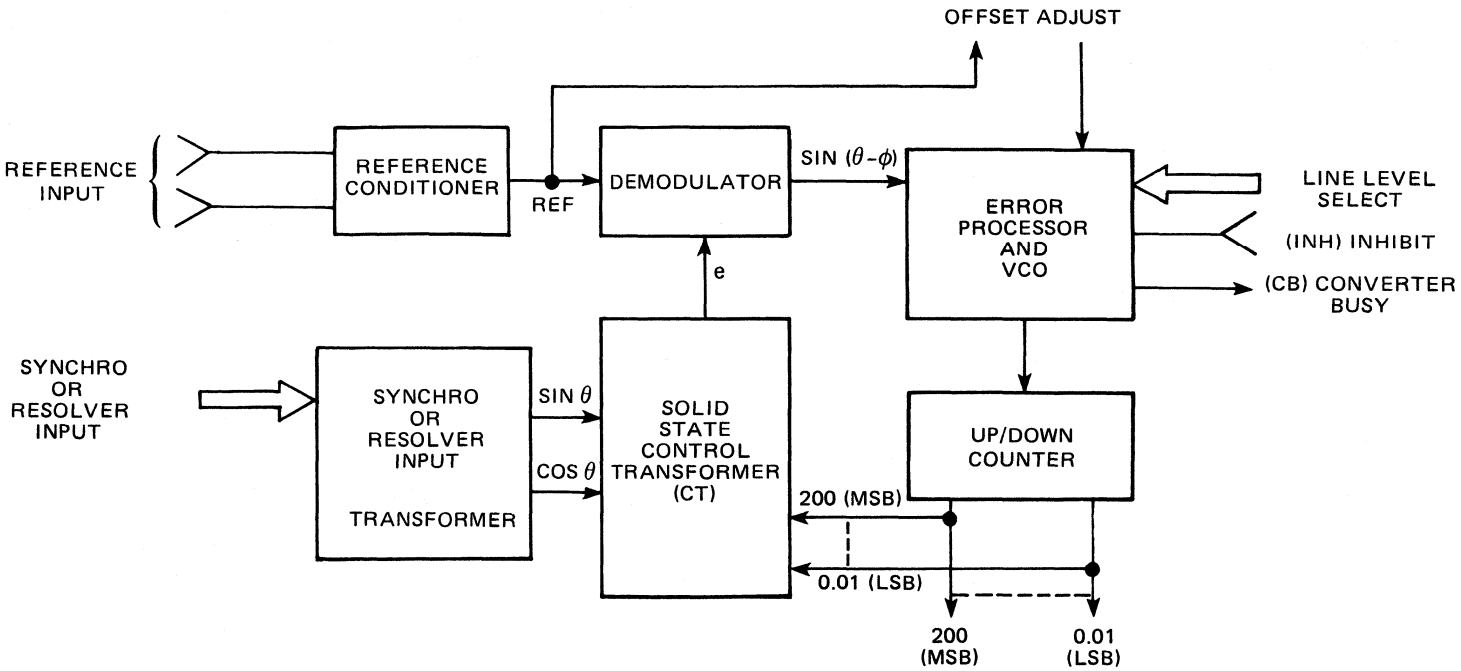


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS FOR SDC-14700

Apply over temperature range, power supply range, reference frequency and amplitude range, ±10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	0.01° (5 BCD digits)
ACCURACY	
Standard	±0.05°
High Accuracy	±0.03°
REPEATABILITY	Within 0.01°
ANGLE RANGE	
(Continuous rotation)	0° to +359.99°
REFERENCE INPUT	
Input Type	Solid state differential
Voltage Level	10 to 126 V rms
Frequency	47 to 1200 Hz
Input Impedance	
Single ended	148 kΩ min
Differential	296 kΩ min
Harmonic Content	±10% max
SIGNAL INPUTS	
Input Type (Pin Programmable)	Synchro or Resolver, transformer isolated
Voltage (Line to Line – Pin Programmable)	11.8, 26 or 90 V, ±10%
Allowed Phase Shift	±10° max, relative to reference
Input Impedance	
Resolver	170 kΩ min } resistive balanced,
Synchro	148 kΩ min } transformer isolated
Breakdown Voltage	500 V min to logic ground
DIGITAL INPUT/OUTPUT	
Logic Type	TTL/CMOS Compatible
Input	
Inhibit (INH)	"1" or open = track "0" or GND = inhibit "0" current = 0.04 mA max.
Outputs	
Drive Capability	"0" current = 0.4 mA max.
5 decade BCD	Parallel positive logic; 18 lines
Converter Busy (CB)	4 to 10 μs positive pulse
DYNAMIC CHARACTERISTICS	
Tracking Rate	180°/sec
Settling Time (to 1 LSB for 179° step)	3 sec
Acceleration For 1 LSB Lag	3.5°/sec²
Open Loop Transfer Function	$G = \frac{18.6^2\left(\frac{S}{9}+1\right)}{S^2\left(\frac{S}{90}+1\right)}$
OFFSET ADJUST	
(Insensitive to Reference Level)	±2° min by external potentiometer
POWER SUPPLY REQUIREMENTS	
Voltage	−8 V ±10% / +5 V ±5%
Absolute Maximum Voltage	−11 V / +7 V
Current	40 mA max. 25 mA typ. / 100 mA max.
TEMPERATURE RANGE	
Operating	
−3XX	0°C to +70°C
Storage	−55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size	2.625 x 3.125 x 0.82 inch (67 x 79 x 21 mm)
Weight	7 oz, typ (300 g)

SPECIFICATIONS FOR SDC-14701

Apply over temperature range, power supply range, reference frequency and amplitude range, ±10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	0.01° (5 BCD digits)
ACCURACY	
Standard	±0.05°
High Accuracy	±0.03°
REPEATABILITY	Within 0.01°
ANGLE RANGE	
(Continuous rotation)	0° to +359.99°
REFERENCE INPUT	
Input Type	Solid state differential
Voltage Level	6 V rms ±10%
Frequency	57-63 Hz
Input Impedance	
Single ended	20 kΩ min
Differential	40 kΩ min
Harmonic Content	±10% max
SIGNAL INPUTS	
Input Type	Resolver
Voltage (Line to Line)	2 V ±10°
Input Impedance	20 MΩ min
DIGITAL INPUT/OUTPUT	
Logic Type	TTL/CMOS Compatible
Input	
Inhibit (INH)	"1" or open = track "0" or GND = inhibit "0" current = 0.04 mA max.
Outputs	
Drive Capability	"0" current = 0.4 mA max.
5 decade BCD	Parallel positive logic; 18 lines
Converter Busy (CB)	4 to 10 μs positive pulse
DYNAMIC CHARACTERISTICS	
Tracking Rate	180°/sec
Settling Time (to 1 LSB for 179° step)	3 sec
Acceleration For 1 LSB Lag	3.5°/sec²
Open Loop Transfer Function	$G = \frac{18.6^2\left(\frac{S}{9}+1\right)}{S^2\left(\frac{S}{90}+1\right)}$
OFFSET ADJUST	
(Insensitive to Reference Level)	±2° min by external potentiometer
POWER SUPPLY REQUIREMENTS	
Voltage	−8 V ±10% / +5 V ±5%
Absolute Maximum Voltage	−11 V / +7 V
Current	40 mA max. 25 mA typ. / 100 mA max.
TEMPERATURE RANGE	
Operating	
−3XX	0°C to +70°C
Storage	−55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size	2.625 x 3.125 x 0.82 inch (67 x 79 x 21 mm)
Weight	7 oz, typ (300 g)

TECHNICAL INFORMATION

ANGLE OUTPUTS

The digital output bits of the SDC-14700 and SDC-14701 are 0.01° to 200°, giving output angles over the range of 0° to 359.99°.

TIMING

Figure 2 shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy pulse (CB). The CB is a positive pulse 4 to 10 μsec long. Data changes on the leading edge of the CB pulse, and data can be transferred 1 μsec after the leading edge.

The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the inhibit is applied. Timing is as follows: (a) apply the inhibit, (b) wait 1 μs, (c) transfer the data, and (d) release the inhibit. Extra CB pulses will not occur if the input angle changes while the counter is locked by the INH.

SIGNAL INPUT SDC-14700 (PIN PROGRAMMABLE)

For synchro operation, connect S to SS. For resolver operation, it is recommended that S3 be connected to S3'. For 90 V input no additional connection is required. For 26 V or 11.8 V input, connect 26 V or 11.8 V to ANA GND respectively (see SDC-14700 mechanical outline).

SIGNAL INPUT SDC-14701 (DIRECT INPUT)

The SDC-14701 is not pin programmable. This module accepts only 2 V ±10% resolver inputs. The + sin and + cos signals should be connected to + SIN and + COS pins respectively. The − sin and − cos should be connected to ANA GND (see SDC-14701 mechanical outline).

SDC-14701 OPERATION

The SDC-14701 is designed to be used with an inexpensive standard 400 Hz, 26/11.8 V or 26/12.6 V resolver. The resolver should be operated with a 6 V @ 60 Hz reference. By operating a 400 Hz (26/11.8 or 26/12.6) resolver at 6 V @ 60 Hz, a signal voltage of 2 V with a 45° phase lead is generated. The SDC-14701 has a phase lead circuit designed into the reference input to compensate for the input signal phase lead.

OFFSET ADJUST

By connecting a 10 KΩ potentiometer between the −0 and +0, and the wiper to VO, an offset adjustment of up to ±2° can be made. Since the signal is derived from the reference, the angle offset will not be affected by variations in the reference level (see Figure 1).

POWER SUPPLIES

Two supplies are required. They should be well regulated and, when testing or evaluating the converter on the bench, be of the current limited type. Set the current limiting as follows:

− 8 V supply at 75 mA
+ 5 V supply at 150 mA

If a − 8 V supply is not available, a −15 V supply, with a 6.8 V zener in series, may be used.

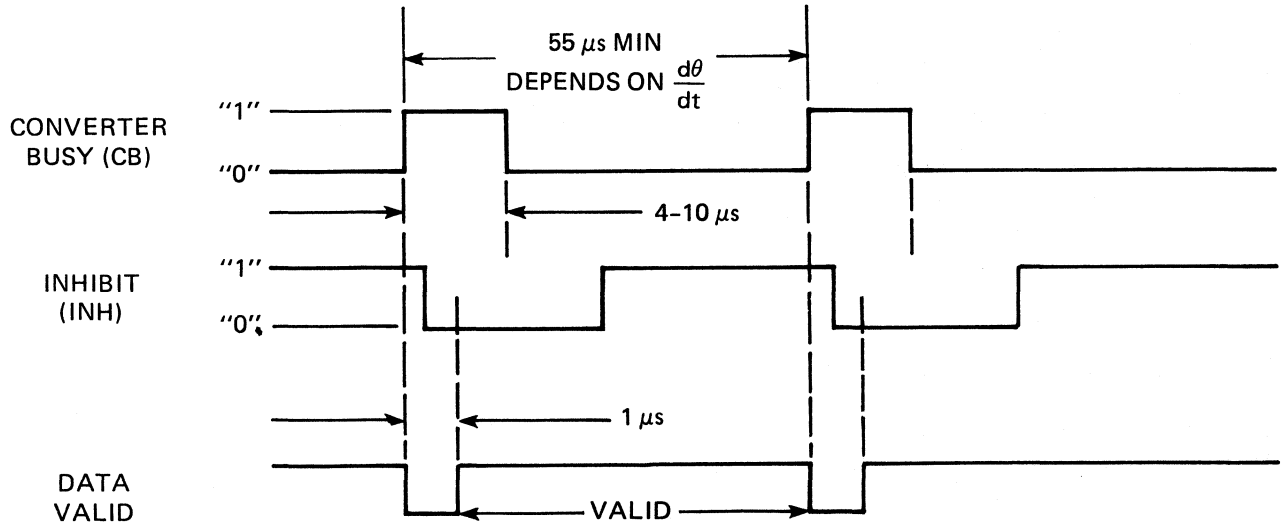
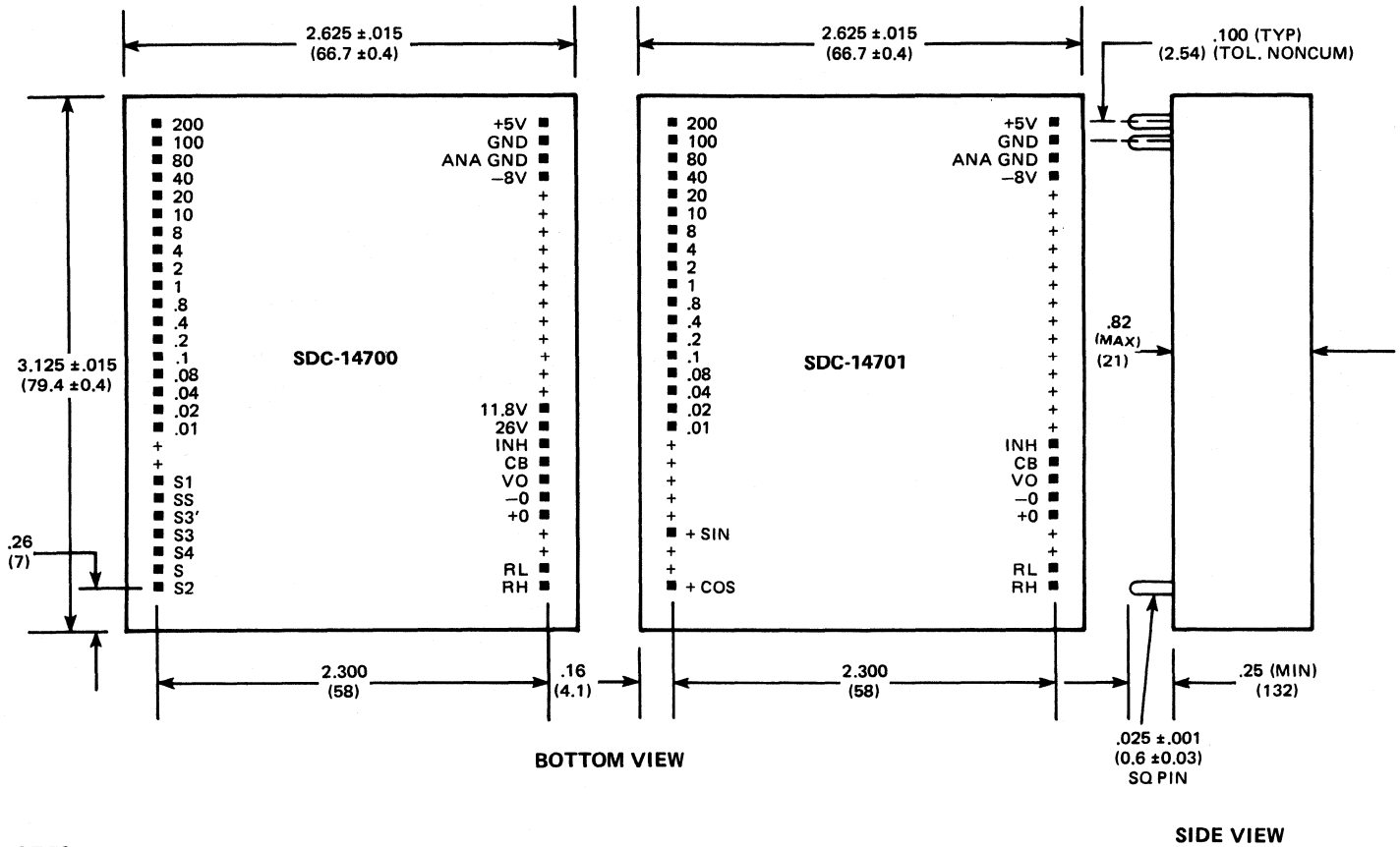


FIGURE 2. TIMING DIAGRAM

MECHANICAL OUTLINE



NOTES:
1. Pin material meets solderability requirements of MIL-STD-202 method 208.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, type SDG-F.
3. Pin callouts on bottom view for reference only.
4. Dimensions in inches (millimeters).

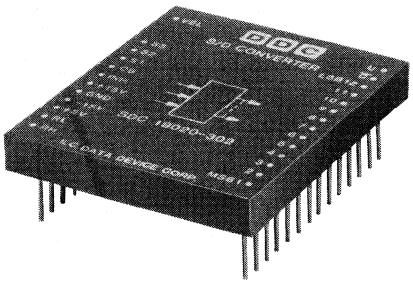
ORDERING INFORMATION

SDC-14700 - 3 9 4

- **4** — Accuracy Grade:
  - 4 = ± 0.05°
  - 5 = ± 0.03°
- **9** — Inputs:*
  - 9 = Standard (pin programmable 11.8 V, 26 V or 90 V)
  - 8 = 2 V (for direct input)
- **3** — Temperature Range:
  - 3 = 0°C to +70°C
- **0** — Type:
  - 0 = Standard
  - 1 = Direct Input
- **SDC-14700** — Family Code

*SDC-14700 available with input option 9 only.
SDC-14701 available with input option 8 only.

10, 12 OR 14 BIT INDUSTRIAL S/D OR R/D CONVERTER



DESCRIPTION

The SDC-19000 Series industrial converters are available in 10, 12 or 14 bit resolution with accuracies of ±21 min, ±8.5 min and ±5.3 min respectively. A ±2.6 min (high accuracy) option is available for the 14 bit unit. Repeatability is 1 LSB for all versions. A velocity output is a standard feature of these converters.

These units are available in low, mid and high frequency ranges, with solid state input options for synchro, resolver or direct inputs. The 12 bit units have carry ($\overline{C}$) and direction (U) outputs for multi-turn and incremental applications.

The SDC-19000 Series converters are a low cost, low profile synchro or resolver to digital tracking devices. Because of a unique control transformer algorithm, these converters provide an inherently higher accuracy and jitter free output. Through the use of a type II tracking loop these converters do not exhibit velocity lag up to the specified tracking rates (Figure 1). In addition, the output data is always fresh and continuously available. Each unit is fully factory trimmed and requires no field adjustments or calibration.

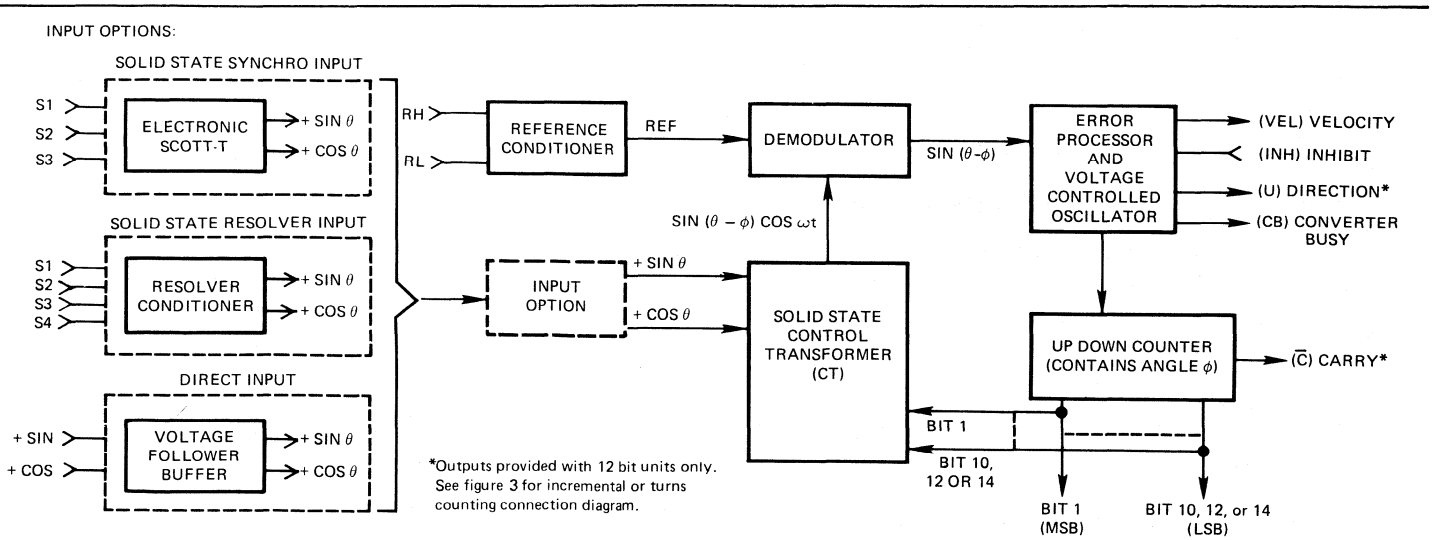
APPLICATIONS

The SDC-19000 Series S/D converters are designed to meet the requirements of the full range of industrial and commercial applications, including control systems, radar antenna position information, automatic machine tooling and robot axis control.

FEATURES

- *LOW COST*
- *FAST TRACKING AT 200 RPS*
- *VELOCITY OUTPUT*
- *ACCURACY:*
  10 BIT ±21 MINUTES
  12 BIT ±8.5 MINUTES
  14 BIT ±5.3 MINUTES
  ±2.6 MINUTES
- *1 LSB REPEATABILITY*
- *CARRY ($\overline{C}$) AND DIRECTION (U) OUTPUT FOR MULTI-TURN AND INCREMENTAL APPLICATIONS (12 BIT UNITS)*
- *2.0V DIRECT INPUT OPTION*

*Patented



NOTE: For military applications DDC's SDC-630 series converter is recommended

FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Apply over temperature range, power supply range, reference frequency and amplitude range, ±10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	UNITS	VALUE		
SDC-19000 SERIES		**1900X**	**1902X**	**1904X**
RESOLUTION	bits	10	12	14
ACCURACY				
Standard	min	±21	±8.5	±5.3
High Accuracy	min	—	—	±2.6
SIGNAL AND REFERENCE INPUT				
Carrier Frequency Range				
Low Range	KHz	.047 to 22	.047 to 22	.047 to 1
Mid Range	KHz	.36 to 22	.36 to 22	.36 to 3
High Range	KHz	2.4 to 22	2.4 to 22	2.4 to 11
REFERENCE INPUT CHARACTERISTICS		**DIRECT INPUTS**	**26V INPUTS**	**115V INPUTS**
Voltage Range	V rms	2 to 10 (4.4 nom)	4 to 50 (26 nom)	20 to 150 (115 nom)
Input Impedance				
Single Ended	Ω	13k min	90k min	380k min
Differential	Ω	26k min	180k min	760k min
Common Mode Range (DC common mode plus recurrent AC peak)	V	18 max	100 max	400 max
SIGNAL INPUT CHARACTERISTICS (Voltage options and minimum input impedance balanced)				
Synchro		90V L-L	11.8V L-L	
Z_{in} (L-L)	kΩ	130	17.5	
Z_{in} Each (L-GND)	kΩ	85	11.5	
Resolver			11.8V L-L	
Z_{in} Single Ended	kΩ		23	
Z_{in} Differential	kΩ		46	
Z_{in} Each (L-GND)	kΩ		23	
Direct (2.0V L-L)				
Z_{in}	MΩ	20		
DIGITAL INPUT/OUTPUT				
Logic Type		TTL		
Input				
Inhibit (INH)		Logic "0" inhibits		
(INH) Loading		0.2 std. TTL loads plus 18 kΩ min pull up to +5V supply		
Output		Low power Schottky		
Parallel Data	bits	10, 12 or 14 parallel lines; natural binary angle, positive logic		
Converter Busy (CB)		0.6 to 1.2 μsec positive pulse; data changes on leading edge		
Carry ($\overline{C}$) 12 Bit Units Only		Logic "0" pulse when internal counter goes through "0" in either direction. For use in turns counting		
Direction (U) 12 Bit Units Only		Logic high when counting up and logic low when counting down		
Drive Capability		2 std TTL loads −55°C to +105°C 4 std TTL loads 0°C to +70°C		
DYNAMIC CHARACTERISTICS		**SEE MODEL SELECTION CHART**		
VELOCITY OUTPUT				
Derived from an op-amp with low impedance output. Positive output for increasing angle.				
Voltage Range	V	±10 min		
		1900X (10 Bit)	1902X (12 Bit)	1904X (14 Bit)
47 Hz to 22 KHz		10V = 12.5 rps	10V = 14 rps	
360 Hz to 22 KHz		10V = 50 rps	10V = 50 rps	
2.4KHz to 22 KHz		10V = 200 rps	10V = 150 rps	
47Hz to 1 KHz				10V = 2.7 rps
360 Hz to 3 KHz				10V = 15 rps
2.4 KHz to 11 KHz				10V = 30 rps
POWER SUPPLY CHARACTERISTICS				
Nominal Voltage		+15V Supply	−15V Supply	+5V Logic Supply
Voltage Range	V	+11 to +16.5	−11 to −16.5	+4.5 to +5.5
Maximum Voltage Without Damage	V	+18	−18	+7
Current				
1900X (10 Bit)	mA	6 typ, 10 max	18 typ, 30 max	80 typ, 120 max
1902X (12 Bit)	mA	6 typ, 10 max	18 typ, 30 max	80 typ, 120 max
1904X (14 Bit)	mA	10 typ, 15 max	20 typ, 30 max	100 typ, 150 max
TEMPERATURE RANGES				
Operating				
−30X	°C	0 to +70		
−10X	°C	−55 to +105		
Storage	°C	−55 to +125		
PHYSICAL CHARACTERISTICS				
Size (Encapsulated Module)	in	3.125 x 2.625 x 0.42 (79.3 x 67 x 11 mm)		
Weight	oz	4 (113g)		

TECHNICAL INFORMATION

TIMING

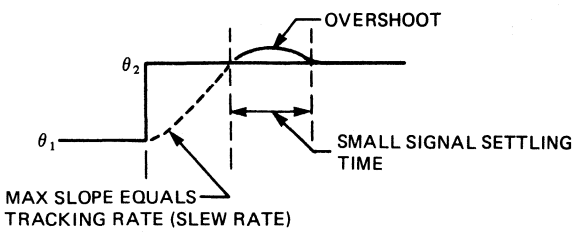
Figure 2 shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy pulse (CB). The CB is a positive pulse 0.6 to 1.2 μsec long. Data changes on the leading edge of the CB pulse, and data can be transferred 0.3 μsec after the leading edge.

The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the Inhibit is applied. The converter will ignore an Inhibit applied during the "busy" interval until the interval is over. Timing is as follows: (a) apply the Inhibit, (b) wait 0.3 μsec (c) transfer the data, and (d) release the Inhibit. Extra CB pulses will not occur if the input angle changes while the counter is locked by the Inhibit.

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltages are not the +15VDC nominal values, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage. The +15V supply voltage will determine the positive maximum velocity, and the −15V supply voltage will determine the negative maximum velocity.

So long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The figure shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT

The nominal open loop transfer function is given by

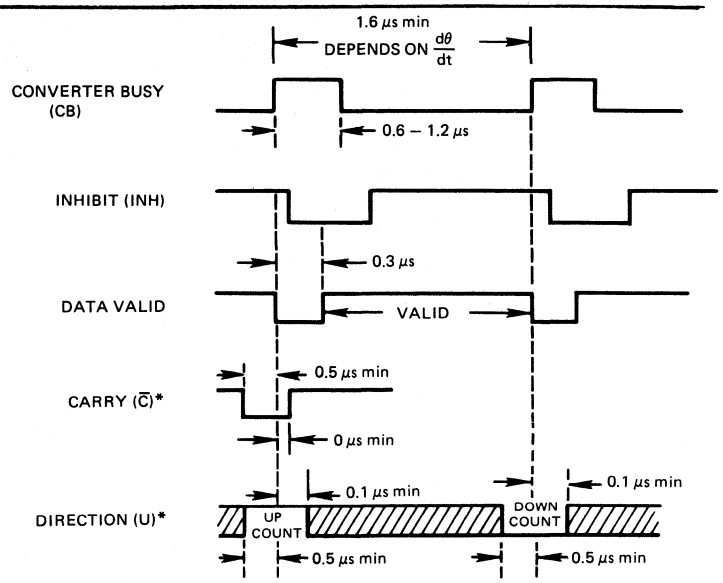
$$G = \frac{A^2\left(\frac{S}{B} + 1\right)}{S^2\left(\frac{S}{10B} + 1\right)}$$

FREQUENCY		10 BIT	12 BIT	14 BIT
HIGH	A	800 sec^{-1}	318 sec^{-1}	264 sec^{-1}
	B	500 sec^{-1}	147 sec^{-1}	89 sec^{-1}
MEDIUM	A	190 sec^{-1}	226 sec^{-1}	167 sec^{-1}
	B	91 sec^{-1}	100 sec^{-1}	56 sec^{-1}
LOW	A	46 sec^{-1}	58 sec^{-1}	30 sec^{-1}
	B	23 sec^{-1}	26 sec^{-1}	10 sec^{-1}

SOLID STATE BUFFER INPUTS

The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection, so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed the following values:

INPUT (L-L)	COMMON MODE (Max)	TRANSIENT PEAK VOLTAGE (Max)
2.0 V	–	15 V
11.8 V	100 V	25 V
90 V	200 V	500 V



*12 bit units only

NOTE: DIRECTION OUTPUT is valid during unshaded area only.

FIGURE 2. TIMING DIAGRAM

CONVERTER BUSY (CB)

The (CB) output is a positive 0.6 to 1.2 μs pulse, and data changes on the leading edge of the pulse. At 150 rps the minimum period between pulses is 1.6 μs, as shown in Figure 2.

DIRECTION (U)

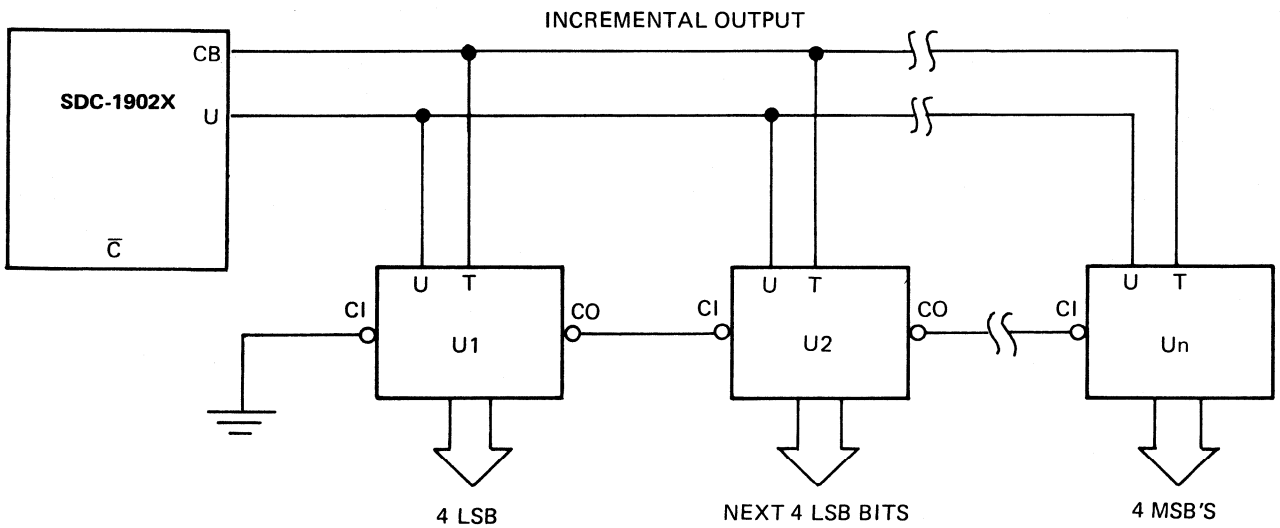
The Direction line is an active low with resistor pull-up. The output is valid as shown in Figure 2. Direction (U) is logic 1 for counting up and logic 0 for counting down. Logic level at the (U) pin is valid up thru 0.5 μs before and 0.1 μs after the leading edge of the (CB) pulse.

CARRY ($\overline{C}$)

The carry output occurs once per revolution. Its purpose is to indicate when the synchro or resolver crosses from one revolution to the next. Carry output is active low and occurs at least 0.5 μs prior to the leading edge of (CB) and ends a minimum of 0 μs after the same leading edge (Figure 2).

VELOCITY OUTPUT (VEL)

Velocity output is a DC voltage proportional to angular velocity $d\theta/dt = d\phi/dt$. The output is derived from an op-amp with low output impedance. The output is positive for an increasing angle.



U1 through Un (4 bit up/down counter)
74LS669 (TTL)
or
4016 (CMOS)

Note: U ≡ Up/down line Logic 1 = Count up
T ≡ Toggle line Counts on positive going edge

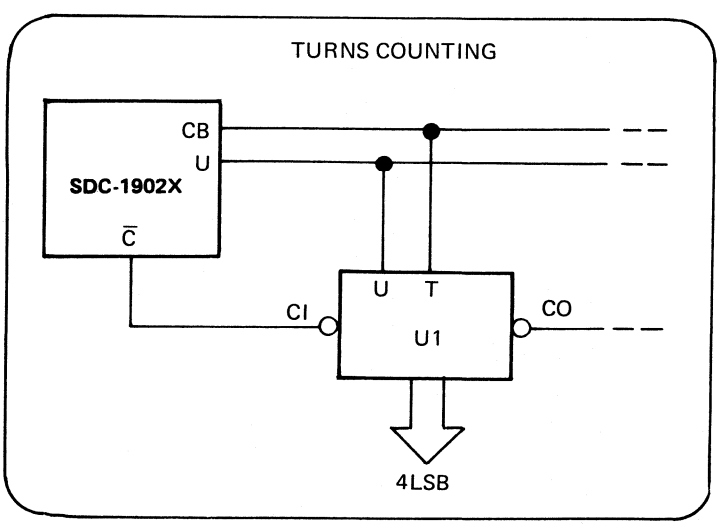


FIGURE 3. INCREMENTAL AND TURNS COUNTING CONNECTION DIAGRAM

MODEL SELECTION/SPECIFICATION CHART

10 BIT SDC-1900X SERIES

Type	Freq. (Hz)	Signal Voltage L-L	Ref. Voltage (V)	Res. (Bits)	Accy. (min)	Tracking Rate (RPS)	Acc. for 1LSB lag error °/sec²	Settling Time for 179° Step to 1 LSB (ms)	Ka (° sec²)	Temp.* (°C)	Part No.
Synchro	47-22K	90	20-150	10	21	12.5	770	300	2200	C	SDC19003-301
Synchro	47-22K	90	20-150	10	21	12.5	770	300	2200	M	SDC19003-101
Synchro	360-22K	90	20-150	10	21	50	12600	80	36000	C	SDC19001-301
Synchro	360-22K	90	20-150	10	21	50	12600	80	36000	M	SDC19001-101
Synchro	360-22K	11.8	4-50	10	21	50	12600	80	36000	C	SDC19000-301
Synchro	360-22K	11.8	4-50	10	21	50	12600	80	36000	M	SDC19000-101
Resolver	360-22K	11.8	4-50	10	21	50	12600	80	36000	C	RDC19005-301
Resolver	360-22K	11.8	4-50	10	21	50	12600	80	36000	M	RDC19005-101
Resolver	2.4K-22K	11.8	4-50	10	21	200	25300	50	72000	C	RDC19006-301
Resolver	2.4K-22K	11.8	4-50	10	21	200	25300	50	72000	M	RDC19006-101
Direct	47-22K	2.0	2-10	10	21	12.5	770	300	2200	C	XDC19008-301
Direct	47-22K	2.0	2-10	10	21	12.5	770	300	2200	M	XDC19008-101
Direct	360-22K	2.0	2-10	10	21	50	12600	80	36000	C	XDC19007-301
Direct	360-22K	2.0	2-10	10	21	50	12600	80	36000	M	XDC19007-101
Direct	2.4K-22K	2.0	2-10	10	21	200	25300	50	72000	C	XDC19009-301
Direct	2.4K-22K	2.0	2-10	10	21	200	25300	50	72000	M	XDC19009-101

12 BIT SDC-1902X SERIES

Synchro	47-22K	90	20-150	12	8.5	14	295	300	3600	C	SDC19023-302
Synchro	47-22K	90	20-150	12	8.5	14	295	300	3600	M	SDC19023-102
Synchro	360-22K	90	20-150	12	8.5	50	4500	90	54000	C	SDC19021-302
Synchro	360-22K	90	20-150	12	8.5	50	4500	90	54000	M	SDC19021-102
Synchro	360-22K	11.8	4-50	12	8.5	50	4500	90	54000	C	SDC19020-302
Synchro	360-22K	11.8	4-50	12	8.5	50	4500	90	54000	M	SDC19020-102
Resolver	360-22K	11.8	4-50	12	8.5	50	4500	90	54000	C	RDC19025-302
Resolver	360-22K	11.8	4-50	12	8.5	50	4500	90	54000	M	RDC19025-102
Resolver	2.4K-22K	11.8	4-50	12	8.5	150	9000	60	108000	C	RDC19026-302
Resolver	2.4K-22K	11.8	4-50	12	8.5	150	9000	60	108000	M	RDC19026-102
Direct	47-22K	2.0	2-10	12	8.5	14	295	300	3600	C	XDC19028-302
Direct	47-22K	2.0	2-10	12	8.5	14	295	300	3600	M	XDC19028-102
Direct	360-22K	2.0	2-10	12	8.5	50	4500	90	54000	C	XDC19027-302
Direct	360-22K	2.0	2-10	12	8.5	50	4500	90	54000	M	XDC19027-102
Direct	2.4K-22K	2.0	2-10	12	8.5	150	9000	60	108000	C	XDC19029-302
Direct	2.4K-22K	2.0	2-10	12	8.5	150	9000	60	108000	M	XDC19029-102

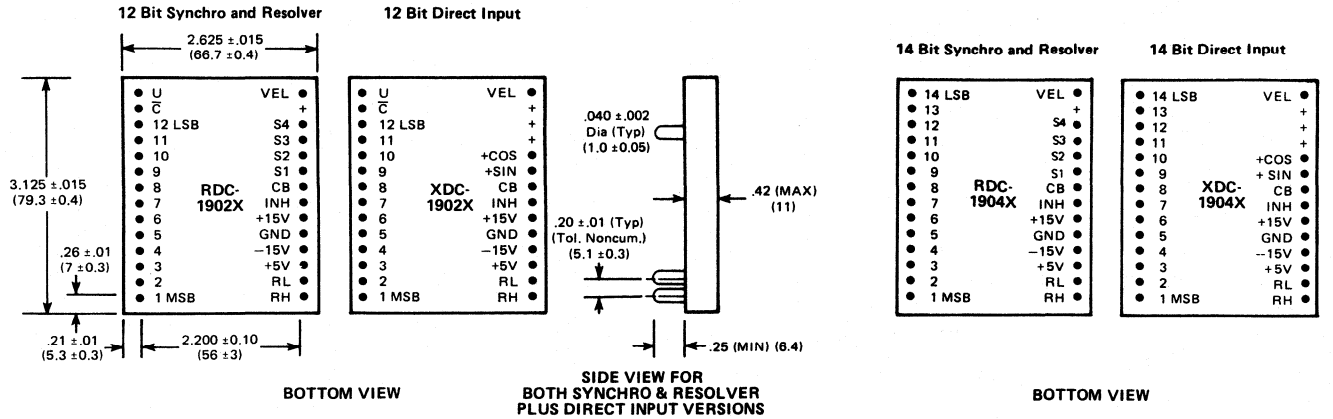
14 BIT SDC-1904X SERIES

Synchro	47-1K	90	20-150	14	5.3	2.7	38	600	1740	C	SDC19043-303
Synchro	47-1K	90	20-150	14	5.3	2.7	38	600	1740	M	SDC19043-103
Synchro	47-1K	90	20-150	14	2.6	2.7	38	600	1740	C	SDC19043-304
Synchro	47-1K	90	20-150	14	2.6	2.7	38	600	1740	M	SDC19043-104
Synchro	360-3K	90	20-150	14	5.3	15	610	150	27800	C	SDC19041-303
Synchro	360-3K	90	20-150	14	5.3	15	610	150	27800	M	SDC19041-103
Synchro	360-3K	90	20-150	14	2.6	15	610	150	27800	C	SDC19041-304
Synchro	360-3K	90	20-150	14	2.6	15	610	150	27800	M	SDC19041-104
Synchro	360-3K	11.8	4-50	14	5.3	15	610	150	27800	C	SDC19040-303
Synchro	360-3K	11.8	4-50	14	5.3	15	610	150	27800	M	SDC19040-103
Synchro	360-3K	11.8	4-50	14	2.6	15	610	150	27800	C	SDC19040-304
Synchro	360-3K	11.8	4-50	14	2.6	15	610	150	27800	M	SDC19040-104
Resolver	360-3K	11.8	4-50	14	5.3	15	610	150	27800	C	RDC19045-303
Resolver	360-3K	11.8	4-50	14	5.3	15	610	150	27800	M	RDC19045-103
Resolver	360-3K	11.8	4-50	14	2.6	15	610	150	27800	C	RDC19045-304
Resolver	360-3K	11.8	4-50	14	2.6	15	610	150	27800	M	RDC19045-104
Resolver	2.4K-11K	11.8	4-50	14	5.3	30	1620	75	73600	C	RDC19046-303
Resolver	2.4K-11K	11.8	4-50	14	5.3	30	1620	75	73600	M	RDC19046-103
Direct	47-1K	2.0	2-10	14	5.3	2.7	38	600	1740	C	XDC19048-303
Direct	47-1K	2.0	2-10	14	5.3	2.7	38	600	1740	M	XDC19048-103
Direct	47-1K	2.0	2-10	14	2.6	2.7	38	600	1740	C	XDC19048-304
Direct	47-1K	2.0	2-10	14	2.6	2.7	38	600	1740	M	XDC19048-104
Direct	360-3K	2.0	2-10	14	5.3	15	610	150	27800	C	XDC19047-303
Direct	360-3K	2.0	2-10	14	5.3	15	610	150	27800	M	XDC19047-103
Direct	360-3K	2.0	2-10	14	2.6	15	610	150	27800	C	XDC19047-304
Direct	360-3K	2.0	2-10	14	2.6	15	610	150	27800	M	XDC19047-104
Direct	2.4K-11K	2.0	2-10	14	5.3	30	1620	75	73600	C	XDC19049-303
Direct	2.4K-11K	2.0	2-10	14	5.3	30	1620	75	73600	M	XDC19049-103

*C = 0°C to + 70°C
M = –55°C to +105°C

MECHANICAL OUTLINE

Dimensions in inches (millimeters)



NOTES:
1. Pin material is electrosoldered brass per MIL-F-14072, M222.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDC-F.
3. Pin S4 is present on Resolver units, and omitted on Synchro units.
4. For the 10 bit version omit pins 11, 12, 13 and 14 from the 14 bit diagram.
5. Pin labels on the bottom view are for reference only.

ORDERING INFORMATION*

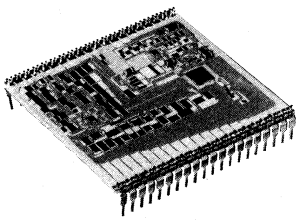
SDC – 19000 – 000

- **Accy:**
  - 1 = ±21 min (10 bit unit only)
  - 2 = ±8.5 min (12 bit unit only)
  - 3 = ±5.3 min (14 bit unit omly)
  - 4 = ±2.6 min (14 bit unit only)
- **Reliability Grade:** 0 = Standard
- **Temp. Range:**
  - 1 = –55°C to +105°C
  - 3 = 0°C to +70°C
- **Input:**
  - 0 = 11.8V, 400Hz, Synchro, 26V Ref
  - 1 = 90V, 400Hz, Synchro, 115V Ref
  - 3 = 90V, 60Hz, Synchro, 115V Ref
  - 5 = 11.8V, 400Hz, Resolver, 26V Ref
  - 6 = 11.8V, 2.4KHz, Resolver, 26V Ref
  - 7 = 2.0V, 400Hz, Direct, 4.4V Ref
  - 8 = 2.0V, 60Hz, Direct, 4.4V Ref
  - 9 = 2.0V, 2.4KHz, Direct, 4.4V Ref
- **Resolution:**
  - 0 = 10 bits
  - 2 = 12 bits
  - 4 = 14 bits
- **Family Code**
- **Signal Input Type:**
  - SDC = Synchro
  - RDC = Resolver
  - XDC = Direct

*See model selection chart for available models

NOTE: Standard size 11 resolver and a heavy duty resolver meeting NEMA 12 standards are available from DDC (consult factory).

SDC-19100 MONOBRID® SERIES*



NOW 16 BITS TOO!

10, 12 ,14 AND 16 BIT INDUSTRIAL S/D AND R/D CONVERTER

DESCRIPTION

The SDC-19100 Series industrial hybrid converters are available in 10, 12, 14 or 16 bit resolution with accuracies of ±21 min, ±8.5 min, ±5.3 min, ±2.6 min and ±1.3 min respectively. Repeatability is 1 LSB for 10 to 14 bit versions and 2 LSB for the 16 bit models. Velocity and direction outputs are standard features of these converters.

These units are available in low, mid and high frequency ranges, with input options for synchro, resolver or direct inputs.

The SDC-19100 Series converters are low cost, low profile synchro or resolver to digital tracking devices. Because of a unique control transformer algorithm, these converters provide an inherently higher accuracy and jitter free output. Through the use of a type II tracking loop these converters do not exhibit velocity lag up to the specified tracking rates (Figure 1). In addition, the output data is always fresh and continuously available. Each unit is fully factory trimmed and requires no field adjustments or calibration.

APPLICATIONS

The SDC-19100 Series converters are designed to meet the requirements of the full range of industrial and commercial applications, including control systems, radar antenna position information, CNC machine tooling and robot axis control.

FEATURES

- *LOW COST*
- *FAST TRACKING*
- *3-STATE LATCHED OUTPUTS*
- *VELOCITY OUTPUT*
- *RESOLUTION/ACCURACY*
  - *10 BIT/±21 MINUTES*
  - *12 BIT/±8.5 MINUTES*
  - *14 BIT/±2.6 OR ±5.3 MINUTES*
  - *16 BIT/±1.3 OR ±2.6 MINUTES*
- *DIRECTION AND COUNT OUTPUTS FOR INCREMENTAL APPLICATIONS*

Note: Monobrid® is a registered trademark of ILC Data Device Corporation.

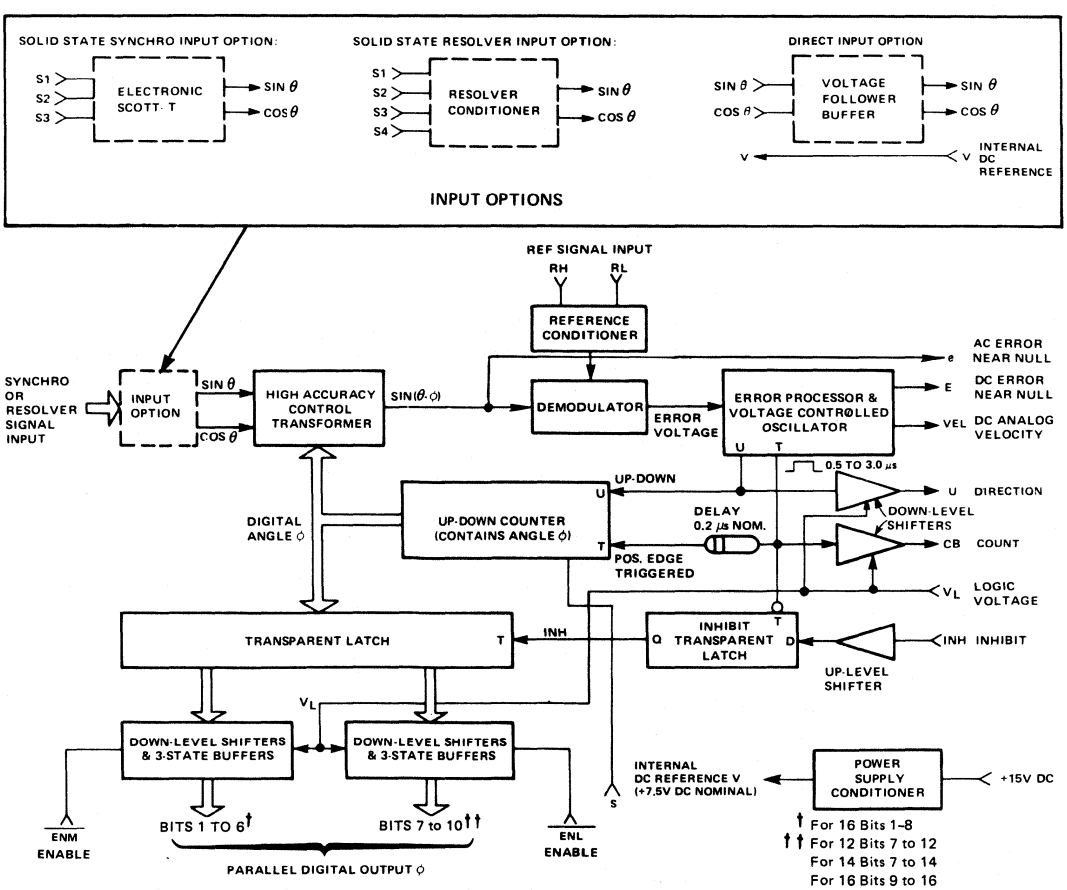


FIGURE 1. BLOCK DIAGRAM

* Patented

SPECIFICATIONS

Apply over temperature range , power supply range, reference frequency and amplitude range, ± 10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	UNITS	VALUE			
SDC-19100 Series		1910X	1912X	1914X	1916X
RESOLUTION	bits	10	12	14	16
ACCURACY	min	±21	±8.5	±2.6 or ±5.3	±1.3 or ±2.6
SIGNAL AND REFERENCE INPUT					
Carrier Frequency Range					
Low Range	kHz	.047 to1	.047 to 1	.047 to 1	.047 to 1
Mid Range	kHz	.36 to 22	.36 to 22	.36 to 22	.36 to 3.5
High Range	kHz	.36 to 22	.36 to 22	.6 to 22	1 to 3.5
REFERENCE INPUT CHARACTERISTICS					
Voltage Range	V rms	4 to 50 (26 nom)	20 to 150 (115 nom)		
Input Impedance					
Single Ended	Ω	50k min	300k min		
Differential	Ω	100k min	600k min		
Common Mode Range (DC common mode plus recurrent AC peak)	V	60 max	300 max		
SIGNAL INPUT CHARACTERISTICS (Voltage options and minimum input impedance balanced)					
Synchro		90V L-L	11.8V L-L		
Z_{in} (L-L)	Ω	160 k	20 k		
Z_{in} Each (L-GND)	Ω	100 k	13 k		
Resolver			11.8V L-L		
Z_{in} Singled Ended	Ω		27 k		
Z_{in} Differential	Ω		54 k		
Z_{in} Each (L-GND)	Ω		27 k		
Direct (2.0V L-L)					
Input Signal Type		Sin and cos resolver signals referenced to converter internal DC reference V			
Sin/Cos Voltage Range		2V nominal, 2.3 max			
Maximum Voltage Without Damage		15V rms continuous; 100V peak transient			
Input Impedance		Z_{in} > 20 MΩ (transient protected voltage follower)			
DIGITAL INPUT/OUTPUT					
Logic type		TTL/CMOS compatible, depending on logic supply voltage			
Inputs		$Z_{in} \geq 25$ kΩ pullup resistor to V_L			
Inhibit (INH)		Logic "0" inhibits			
Enable Bits 1 to 8 $\overline{ENM}$					
Enable Bits 1 to 6 $\overline{ENM}$					
Enable Bits 9 to 16 $\overline{ENL}$		$\overline{ENM}$ and $\overline{ENL}$ { Logic "0" enables			
Enable Bits 7 to 14 $\overline{ENL}$		Logic "1" high impedance			
7 to 12 $\overline{ENL}$					
7 to 10 $\overline{ENL}$					
Enable Time	μs				
S (Control Transformer)		Logic "0" for use as CT			
Logic Type		CMOS Compatible – Logic "0" ≤0.3 V_L, Logic "1" ≥0.7 V_L			
Accuracy	min	±1 (16 bit), ±4 (14 bit), ±5.3 (12 bit), ±10.5 (10 bit)			
Loading		CMOS			
Output					
Parallel Data	bits	10, 12, 14 or 16 parallel lines; natural binary angle, positive logic			
Count (CB)		0.7 to 2.0 μsec positive pulse; leading edge initiates counter update			
Direction (U)		Logic high when counting up and logic low when counting down			
Drive Capability		1 std TTL load, 1.6 mA at 0.4 V max (logic "0"); 10 std TTL loads, 0.4 mA at 2.8 V min (logic "1") 10μA max (high impedance)			
ANALOG OUTPUTS					
Internal DC reference (V)		+15 VDC/2 ≃7.5V nom			
AC Error (e)	mV	5 rms per LSB of error (16 bits)			
	mV	10 rms per LSB of error (14 bits)			
	mV	12.5 rms per LSB of error (10 and 12 bits)			
Filtered DC Error Voltage (E)	V	–0.5 per +1 LSB of error (±3 LSB range) 16 bit unit.			
	V	–1 per +1 LSB of error (±3 LSB range) 14-bit unit.			
	V	–1.25 per +1 LSB of error (±3 LSB range) 10 and 12-bit units.			
POWER SUPPLY CHARACTERISTICS					
Nominal Voltage		+15V Supply	Logic Supply		
Voltage Range	V	+11 to +16.5	+4.5 to +15		
Maximum Voltage Without Damage	V	+18	+18		
Current or Impedance		15 mA max	Z_{in} = 5 kΩ min		
TEMPERATURE RANGES					
Operating					
–30X	°C	0 to +70			
–10X	°C	–30 to +105			
Storage	°C	–30 to +105			
PHYSICAL CHARACTERISTICS					
Size	in	2.1 x 2.1 x 0.2 (53 x 53 x 5 mm) see mechanical outline			
Weight	oz	0.7 (20g)			

TECHNICAL INFORMATION

INTRODUCTION

The circuit shown in the SDC-19100 block diagram, Figure 1, consists of three main parts: the signal input option; a feedback loop whose elements are the control transformer, demodulator error processor, and up-down counter; and digital interface circuitry including various latches and buffers.

The input options accept a synchro or resolver input and produce a resolver type output for the control transformer. The first two options, called solid state synchro and resolver input, accept synchro and resolver signal inputs directly, and provide signal isolation internally. The third option is a direct input designed to operate with a 2V L-L input, which allows for the use of a lower reference voltage. Since it does not have an input scaling network it is inherently more accurate.

All input options are DC coupled with broadband characteristics up to the specified frequencies.

In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The internal converter operates with signals in resolver format, $\sin\theta \cos\omega t$ and $\cos\theta \cos\omega t$. Synchro signals are of the form $\sin\theta \cos\omega t$, $\sin(\theta + 120^\circ)\cos\omega t$, and $\sin(\theta + 240^\circ)\cos\omega t$. The diagrams below show synchro and resolver signals as a function of the angle θ.

The feedback loop produces a digital angle Φ which tracks the analog input angle θ to within the specified accuracy of the converter. The control transformer performs the following trigonometric computation:

$$\sin(\theta - \Phi) = \sin\theta \cos\Phi - \cos\theta \sin\Phi$$

where θ is the angle representing the synchro or resolver shaft position, and Φ is the digital angle contained in the up-down counter in the converter. The tracking process consists of continually adjusting Φ to make $(\theta - \Phi) \rightarrow 0$, so that Φ will represent the shaft position θ.

The output of the demodulator is an analog DC level proportional to $\sin(\theta - \Phi)$. The error processor integrates this $\sin(\theta - \Phi)$ error signal, and the output of the integrator is used to control the frequency of a voltage controlled oscillator "clock" pulses which are accumulated by the up-down counter. The up-down counter is functionally an incremental integrator. Therefore there are two stages of integration, making the converter a Type II tracking servo. In a Type II servo, the voltage controlled oscillator always settles to a counting rate which makes $d\Phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The digital interface circuitry has three main functions: to latch the output bits during an Inhibit command so that stable data can be read out, to furnish both parallel and 3-state data formats, and to act as a buffer between the internal CMOS logic and the external logic level.

Applying an Inhibit command will lock the data in the transparent latch without interfering with the continuous tracking of the feedback loop. This is a new feature, since S/D and R/D converters usually lock the up-down counter while an Inhibit is applied. In the SDC-19100 Series Monobrids, therefore, the digital angle Φ is always updated and the Inhibit can be applied for an abitrary amount of time. The Inhibit transparent latch and the 0.2 μs delay are also parts of the Inhibit circuitry, whose detailed operation is described in the Logic Output/Input Section.

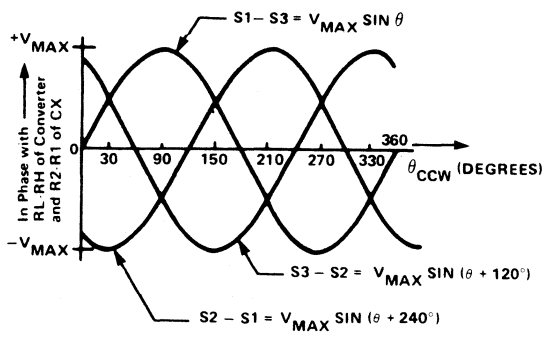
When testing or evaluating the converter, it is advisable to limit the power supply currents as follows:

+15V Supply Limit at 20 mA.
Logic Supply V_L at 2 mA + Digital Load at Logic 1.

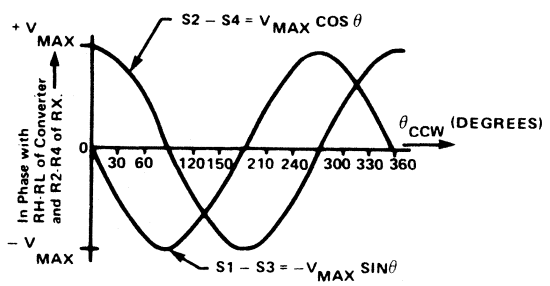
Analog circuits inside the SDC-19100 module are referenced to an internal DC reference level V which rides at +7.5 nominal with respect to the external ground (GND). V should not be connected to the external ground.

SOLID STATE BUFFER INPUTS

The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection,



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

SYNCHRO AND RESOLVER SIGNALS

so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed the following values:

Input	Common Mode Maximum	Max Transient Peak Voltage
11.8V L-L	30V Peak	150V
26 V L-L	60V Peak	150V
90 V L-L	220V Peak	500V
115 V Ref	300V Peak	1000V
26 V Ref	60V Peak	200V

90V line-to-line systems may have voltage transients which exceed the 500V specification listed above.

Voltage transients are likely to occur whenever synchro voltages are switched on or off. For instance, a 1000V transient can be generated when the primary of a CX or TX driving a synchro or resolver input is opened.

DIRECT INPUT

Direct input units require a signal conditioner that provides a 2.0V rms nominal resolver type signal referenced to the internal DC reference V. This input option may be preferred in applications where the signal conditioner can be integrated with other components, as in many multiplexed systems.

LOGIC INPUT/OUTPUT

Logic outputs consist of parallel data bits and count (CB). All logic outputs are short-circuit proof to ground and to positive voltages as high as V_L. The CB output is a positive 0.7–2.0 μs pulse, and data changes about 0.2 μs after the leading edge of the pulse because of an internal delay (see Figure 1). Data is valid 0.5 μs after the leading edge of a CB. Angle is determined by adding bits in the 1 state.

The parallel digital outputs are gated to provide 6 and 8 bit bytes when the MSB byte is enabled ($\overline{\text{ENM}}$). The 8 bit byte is reserved for 16 bit resolution converters only. The LSB byte ($\overline{\text{ENL}}$) is gated to provide 4, 6 and 8 bit bytes dependent upon converter resolution (4 and 6 bit bytes are reserved for 10 and 12 bit converters while the LSB byte is 8 bits for both 14 and 16 bit resolutions). When the Enables for the gates are at logic 0, the gate outputs are at normal logic 1 or 0, depending on the bit state. When the Enables are at logic 1, the gate outputs are high impedance and the microprocessor sees an essentially open line. Outputs are valid 0.5 μs after an Enable is driven to logic 0. For 10, 12, 14, or 16 bit parallel output operation when the 3-state feature is not used, the Enable lines should be tied to logic 0.

The Inhibit (INH) logic input locks the transparent latch so that the bits will remain stable while data is being transferred (see Figure 1). The output is stable 0.5 μs after the Inhibit is driven to logic 0. A logic 0 at the T input locks the latch, and a logic 1 allows the bits to change. The purpose of the INH transparent latch is to prevent the transmission of invalid data when there is an overlap between the CB and INH. While the counter is not being updated the CB is at logic 0 and the INH latch is transparent. When the CB goes to logic 1 the INH latch is locked. If a CB occurs after an INH has been applied, the latch will remain locked and its data cannot change until the CB returns to logic 0. If an INH is applied during a CB pulse, the latch will not lock until the CB pulse is over. The purpose of the 0.2 μs delay is to prevent a race condition between the CB and the INH in which the up-down counter begins to change just as an INH is applied.

The Direction Output (U) is valid as shown in Figure 2. It is logic 1 for counting up and logic 0 for counting down. Logic level at the (U) pin is valid up thru 0.5 μs before and 0.1 μs after the leading edge of the (CB) pulse.

Since the SDC-19100 converters contain a CMOS device, standard CMOS handling procedures should be followed.

TIMING

Figure 2 shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. The output data change is initiated by the leading edge of the CB pulse, delayed by the 0.2μs (nominal) delay. The output becomes stable in less than 0.5μs even though the CB pulse may last longer. Data transfer can be made synchronous with the leading edge of CB, delayed by 0.5μs. (See Timing Diagram.)

An Inhibit input, regardless of its duration, does not affect converter update. A simple method of interfacing to a computer, asynchronous to CB pulse, is to (a) apply the inhibit, (b) wait 1.5 μs min., (c) transfer the data and (d) release the inhibit.

DYNAMIC PERFORMANCE

A Type II servo loop ($K_v = \infty$) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltages are not the +15VDC nominal values, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage.

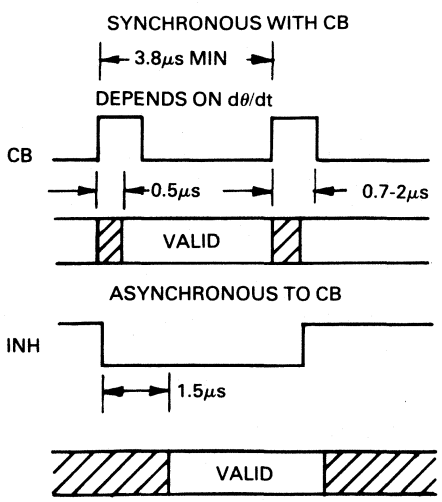
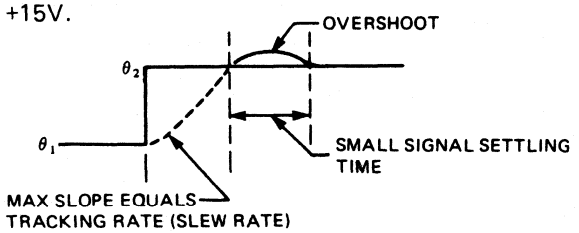


FIGURE 2. TIMING DIAGRAM

As long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The figure shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to a final value is a function of the small signal settling time.

ANALOG OUTPUTS

The analog outputs are V, e, E and VEL. V is an internal DC reference, +7.5 VDC nominal. The outputs e, E and VEL ride on the internal DC reference voltage V, and should be measured with respect to V. Outputs can swing ±5V when the voltage level of the +15V power supply is +15V. The output swing changes proportionally if the level is not a +15V.



RESPONSE TO A STEP INPUT

$$G = \frac{A^2\left(\frac{S}{B} + 1\right)}{S^2\left(\frac{S}{10B} + 1\right)}$$

NOTE: Values for A and B are found in the Model Selection/Specification Chart.

CONVERTER LOOP DYNAMICS

AC error (e) is proportional to the error $(\theta - \phi)$ with 5 mV/LSB nominal for the 16 bit unit, 10 mV/LSB nominal for the 14 bit unit and 12.5 mV/LSB nominal for the 12 and 10 bit units.

E is a filtered DC voltage proportional to the error $(\theta - \phi)$ near the null point, with −0.5 VDC/+LSB of error for the 16 bit unit, −1 VDC/+LSB of error for the 14 bit unit and −1.25 VDC/+LSB of error for the 12 and 10 bit units.

Velocity output (VEL) is a DC voltage proportional to angular velocity $d\theta/dt = d\phi/dt$. The output is positive for an increasing angle.

Maximum loading for each analog output is 1.0 mA. Outputs e, E, and VEL are not required for normal operation of the converter; V is used as internal DC reference with the direct input option.

The outputs e, E and VEL are not closely controlled or characterized. Consult factory for further information.

USE AS A CT

The SDC-19100 Series S/D can be used as a "Solid State CT". This is analagous to the function of a rotary control transformer except here the *rotary* shaft input is replaced by a *digital* angle. Referring to the equation below, the output is an AC voltage (e) which varies as the sine of the difference between the analog input angle and the digital angle.

$$e = \sin(\theta - \phi)\cos\omega t$$

where θ is the analog angle and ϕ is the digital angle.

Control transformers are frequently used as error signal generators in closed servo loops. They are useful when digital remote control of a position servo must be accomplished.

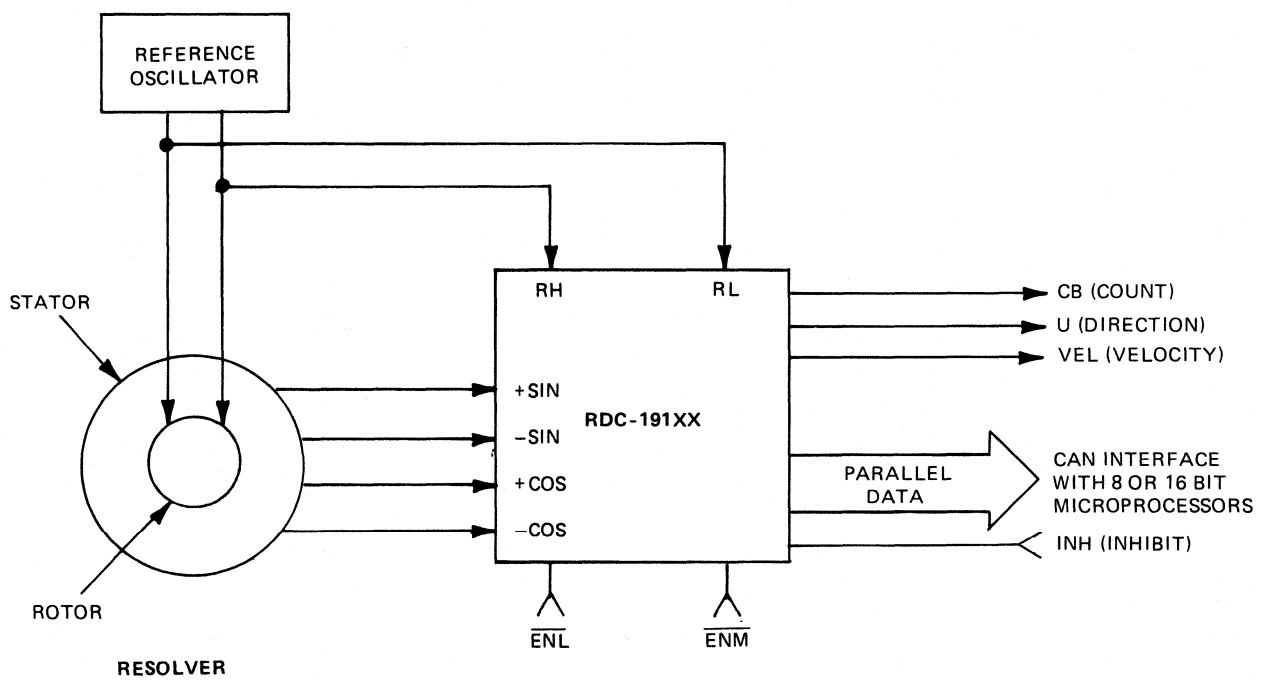


FIGURE 3. TYPICAL RESOLVER CONNECTION.

MODEL SELECTION/SPECIFICATION CHART

	Freq. (Hz)	Signal Voltage (L-L)	Ref Voltage (V)	Tracking Rate (RPS)	Acc. for 1 LSB lag error °/sec²	Settling Time for 179° Step to 1 LSB (ms)	Ka	Trans. Func. Breaks A	B	Velocity ± RPS = ± Volts nom	Temp. (°C)	Part No.
10 BIT RESOLUTION/±21 MINUTE ACCURACY SDC-1910X SERIES												
Synchro	47-1K	90	20-150	48	1400	350	4000	62	25	56=5	0°C to +70°C	SDC 19103-301
Synchro	47-1K	90	20-150	48	1400	350	4000	62	25	56=5	−30°C to +105°C	SDC 19103-101
Synchro	360-22K	90	20-150	192	22000	90	62000	250	100	220=5	0°C to +70°C	SDC 19101-301
Synchro	360-22K	90	20-150	192	22000	90	62000	250	100	220=5	−30°C to +105°C	SDC 19101-101
Synchro	360-22K	11.8	4-50	192	22000	90	62000	250	100	220=5	0°C to +70°C	SDC 19100-301
Synchro	360-22K	11.8	4-50	192	22000	90	62000	250	100	220=5	−30°C to +105°C	SDC 19100-101
Resolver	360-22K	11.8	4-50	192	22000	90	62000	250	100	220=5	0°C to +70°C	RDC 19105-301
Resolver	360-22K	11.8	4-50	192	22000	90	62000	250	100	220=5	−30°C to +105°C	RDC 19105-101
Resolver	360-22K	11.8	4-50	400	160000	30	460000	680	300	400=3.4	0°C to +70°C	RDC 19106-301
Resolver	360-22K	11.8	4-50	400	160000	30	460000	680	300	400=3.4	−30°C to +105°C	RDC 19106-101
Direct	47-1K	2	4-50	48	1400	350	4000	62	25	56=5	0°C to +70°C	XDC 19108-301
Direct	47-1K	2	4-50	48	1400	350	4000	62	25	56=5	−30°C to +105°C	XDC 19108-101
Direct	360-22K	2	4-50	192	22000	90	62000	250	100	220=5	0°C to +70°C	XDC 19107-301
Direct	360-22K	2	4-50	192	22000	90	62000	250	100	220=5	−30°C to +105°C	XDC 19107-101
Direct	360-22K	2	4-50	400	160000	30	460000	680	300	400=3.4	0°C to +70°C	XDC 19109-301
Direct	360-22K	2	4-50	400	160000	30	460000	680	300	400=3.4	−30°C to +105°C	XDC 19109-101
12 BIT RESOLUTION/±8.5 MINUTE ACCURACY SDC-1912X SERIES												
Synchro	47-1K	90	20-150	12	350	360	4000	62	25	14=5	0°C to +70°C	SDC 19123-302
Synchro	47-1K	90	20-150	12	350	360	4000	62	25	14=5	−30°C to +105°C	SDC 19123-102
Synchro	360-22K	90	20-150	48	5500	90	62000	250	100	56=5	0°C to +70°C	SDC 19121-302
Synchro	360-22K	90	20-150	48	5500	90	62000	250	100	56=5	−30°C to +105°C	SDC 19121-102
Synchro	360-22K	11.8	4-50	48	5500	90	62000	250	100	56=5	0°C to +70°C	SDC 19120-302
Synchro	360-22K	11.8	4-50	48	5500	90	62000	250	100	56=5	−30°C to +105°C	SDC 19120-102
Resolver	360-22K	11.8	4-50	48	5500	90	62000	250	100	56=5	0°C to +70°C	RDC 19125-302
Resolver	360-22K	11.8	4-50	48	5500	90	62000	250	100	56=5	−30°C to +105°C	RDC 19125-102
Resolver	360-22K	11.8	4-50	100	40000	60	460000	680	300	100=3.4	0°C to +70°C	RDC 19126-302
Resolver	360-22K	11.8	4-50	100	40000	60	460000	680	300	100=3.4	−30°C to +105°C	RDC 19126-102
Direct	47-1K	2	4-50	12	350	360	4000	62	25	14=5	0°C to +70°C	XDC 19128-302
Direct	47-1K	2	4-50	12	350	360	4000	62	25	14=5	−30°C to +105°C	XDC 19128-102
Direct	360-22K	2	4-50	48	5500	90	62000	250	100	56=5	0°C to +70°C	XDC 19127-302
Direct	360-22K	2	4-50	48	5500	90	62000	250	100	56=5	−30°C to +105°C	XDC 19127-102
Direct	360-22K	2	4-50	100	40000	60	460000	680	300	100=3.4	0°C to +70°C	XDC 19129-302
Direct	360-22K	2	4-50	100	40000	60	460000	680	300	100=3.4	−30°C to +105°C	XDC 19129-102
14 BIT RESOLUTION/±5.3 MINUTE ACCURACY SDC-1914X SERIES *												
Synchro	47-1K	90	20-150	3	70	600	3000	56	25	3.2=5	0°C to +70°C	SDC 19143-303
Synchro	47-1K	90	20-150	3	70	600	3000	56	25	3.2=5	−30°C to +105°C	SDC 19143-103
Synchro	360-22K	90	20-150	12	1100	150	50000	224	100	14=5	0°C to +70°C	SDC 19141-303
Synchro	360-22K	90	20-150	12	1100	150	50000	224	100	14=5	−30°C to +105°C	SDC 19141-103
Synchro	360-22K	11.8	4-50	12	1100	150	50000	224	100	14=5	0°C to +70°C	SDC 19140-303
Synchro	360-22K	11.8	4-50	12	1100	150	50000	224	100	14=5	−30°C to +105°C	SDC 19140-103
Resolver	360-22K	11.8	4-50	12	1100	150	50000	224	100	14=5	0°C to +70°C	RDC 19145-303
Resolver	360-22K	11.8	4-50	12	1100	150	50000	224	100	14=5	−30°C to +105°C	RDC 19145-103
Resolver	600-22K	11.8	4-50	25	8100	90	370000	610	300	25=3.4	0°C to +70°C	RDC 19146-303
Resolver	600-22K	11.8	4-50	25	8100	90	370000	610	300	25=3.4	−30°C to +105°C	RDC 19146-103
Direct	47-1K	2	4-50	3	70	600	3000	56	25	3.2=5	0°C to +70°C	XDC 19148-303
Direct	47-1K	2	4-50	3	70	600	3000	56	25	3.2=5	−30°C to +105°C	XDC 19148-103
Direct	360-22K	2	4-50	12	1100	150	50000	224	100	14=5	0°C to +70°C	XDC 19147-303
Direct	360-22K	2	4-50	12	1100	150	50000	224	100	14=5	−30°C to +105°C	XDC 19147-103
Direct	600-22K	2	4-50	25	8100	90	370000	610	300	25=3.4	0°C to +70°C	XDC 19149-303
Direct	600-22K	2	4-50	25	8100	90	370000	610	300	25=3.4	−30°C to +105°C	XDC 19149-103
16 BIT RESOLUTION/±2.6 AND ±1.3 MINUTE ACCURACY SDC-1916X SERIES *												
Synchro	47-1K	90	20-150	.75	12	1000	2120	56	46	0.8=5	0°C to +70°C	SDC 19163-305
Synchro	47-1K	90	20-150	.75	12	1000	2120	56	46	0.8=5	−30°C to +105°C	SDC 19163-105
Synchro	360-3.5K	90	20-150	3	190	250	35000	224	187	3.5=5	0°C to +70°C	SDC 19161-305
Synchro	360-3.5K	90	20-150	3	190	250	35000	224	187	3.5=5	−30°C to +105°C	SDC 19161-105
Synchro	360-3.5K	11.8	4-50	3	190	250	35000	224	187	3.5=5	0°C to +70°C	SDC 19160-305
Synchro	360-3.5K	11.8	4-50	3	190	250	35000	224	187	3.5=5	−30°C to +105°C	SDC 19160-105
Resolver	360-3.5K	11.8	4-50	3	190	250	35000	224	187	3.5=5	0°C to +70°C	RDC 19165-305
Resolver	360-3.5K	11.8	4-50	3	190	250	35000	224	187	3.5=5	−30°C to +105°C	RDC 19165-105
Resolver	1K-3.5K	11.8	4-50	6.3	1430	150	260000	610	510	6.3=3.4	0°C to +70°C	RDC 19166-305
Resolver	1K-3.5K	11.8	4-50	6.3	1430	150	260000	610	510	6.3=3.4	−30°C to +105°C	RDC 19166-105
Direct	360-3.5K	2	4-50	3	194	250	35000	224	187	3.5=5	0°C to +70°C	XDC 19167-305
Direct	360-3.5K	2	4-50	3	194	250	35000	224	187	3.5=5	−30°C to +105°C	XDC 19167-105
Direct	1K-3.5K	2	4-50	6.3	1430	150	260000	610	510	6.3=3.4	0°C to +70°C	XDC 19169-305
Direct	1K-3.5K	2	4-50	6.3	1430	150	260000	610	510	6.3=3.4	−30°C to +105°C	XDC 19169-105

*** For ±2.6 minute accuracy, the last digit of P/N becomes "4". (See Ordering Information.)**

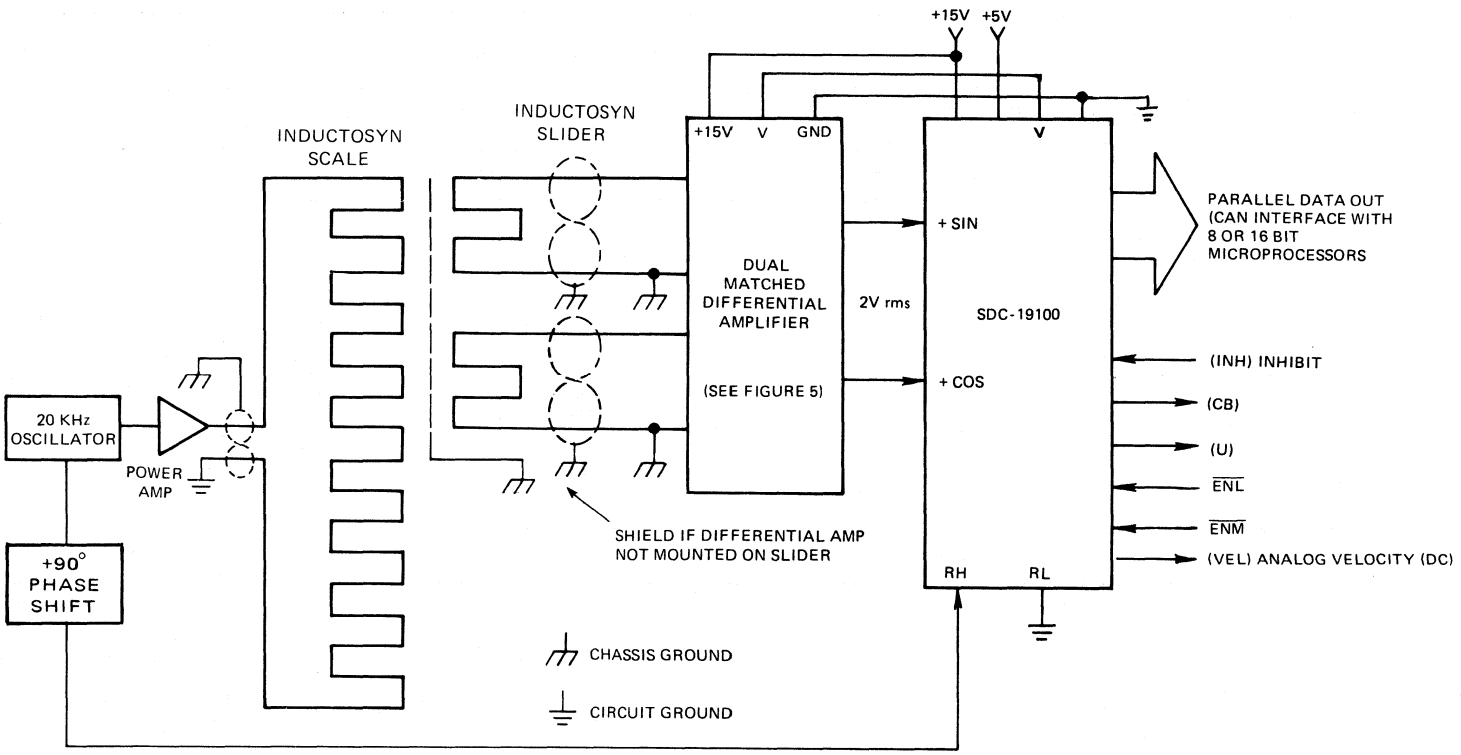


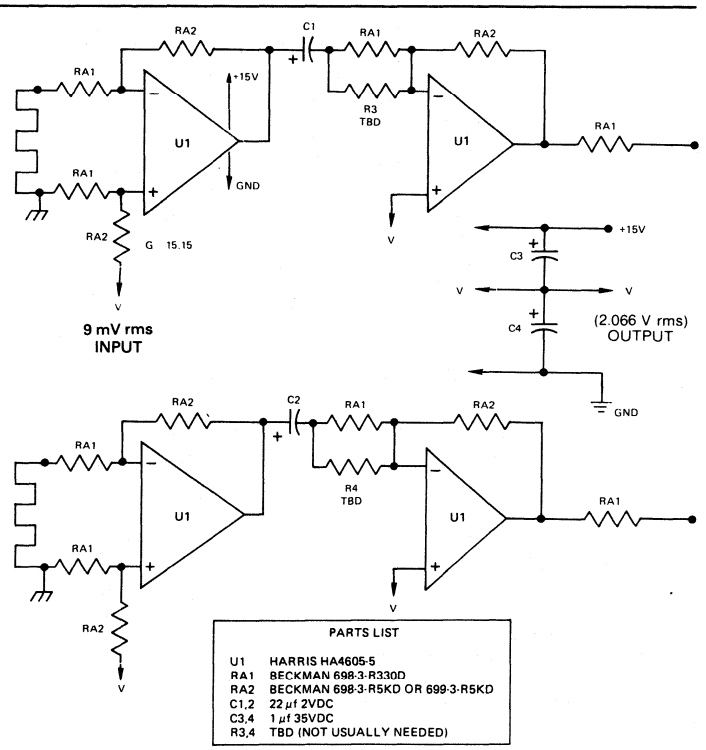
FIGURE 4. TYPICAL INDUCTOSYN CONNECTION

The procedure to enable this function is to disable the up-down counter by setting pin 30 (S) to logic "0" and using the digital output lines (which are bidirectional) as digital inputs. Note that "e" rides on the internal DC reference voltage "V" (approximately 7.5V) and a differential amplifier should be used to reference this signal to real (circuit) ground as shown in the diagram under analog outputs.

The gain control function (Ge) is still operative in CT mode and the effect is the same as when used as an S/D. If you adjust the gain for a lower than nominal line-to-line signal, the error magnitude will remain the same, i.e., 16mV/LSB. If you adjust the gain for a lower signal level but come in with the "nominal" signal level, the error amplitude will be correspondingly gained-up (by the factor $V_{nominal}/V_{lower}$), however the usable error range (dynamic range) is correspondingly reduced.

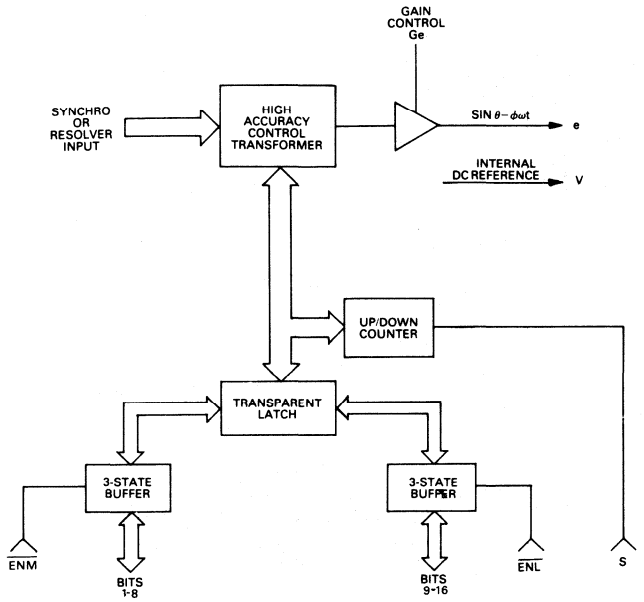
Figure 5 suggests a method for amplifying the output of an Inductosyn to meet the required signal input level of the SDC-19100 (2Vrms, ±10%). The use of this circuit will sufficiently condition the input so resistors R3 and R4 are not needed for most applications.

Trimming should be done by measuring the differential voltage at the input of the op amp closest to the slider (+sin). The output voltage is then measured to determine the gain. The same procedure is performed on the +cos amplifier. A high accuracy digital voltmeter is recommended for the final output readings. Capacitors C1 and C2 are used to create a DC voltage block.



NOTES: 1. For other input levels select RA1 and RA2 as required. Standard values are: 100, 200, 330, 470, 500, 1K, 2K, 2.2K, 4.7K, 5K, 10K, 15K, and 20KΩ.
2. For lower input levels use Harris HA-4625-5

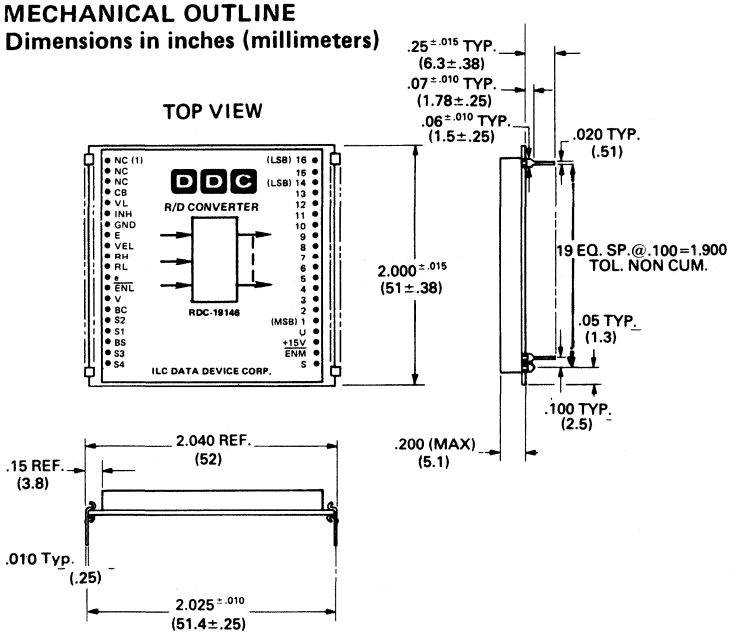
FIGURE 5. DUAL MATCHED DIFFERENTIAL AMPLIFIER



CT BLOCK DIAGRAM

MECHANICAL OUTLINE

Dimensions in inches (millimeters)



NOTES:

1. Pin material is bronze phosphor with solder plating.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, type SDC-F.
3. Pin S4 is present on resolver units, and omitted on synchro units.
4. Omit pins 11, 12, 13, 14, 15 and 16 (10 bit); 13, 14, 15 and 16 (12 bit); 15 and 16 (14 bit) units.
5. For the direct input option, pins S1 and S4 will be replaced by NC, S2 and S3 will be replaced by COS and SIN respectively.
6. BC and BS are used as test points.

IN GENERAL

For applications where a square wave is more convenient than the conventional sine wave, the SDC-19100 Series converters are capable of operating with square waves.

When brushless resolvers are used as position transducers, it is recommended that the transmitter type be used because if a receiver resolver is used a decrease in accuracy will occur.

For users who desire a built-in-test (BIT) function to detect position error between the input and output, a simple detection circuit can be implemented with the AC error signal provided by the SDC-19100 converter. The schematic diagram for the BIT circuit is available from DDC.

ORDERING INFORMATION *

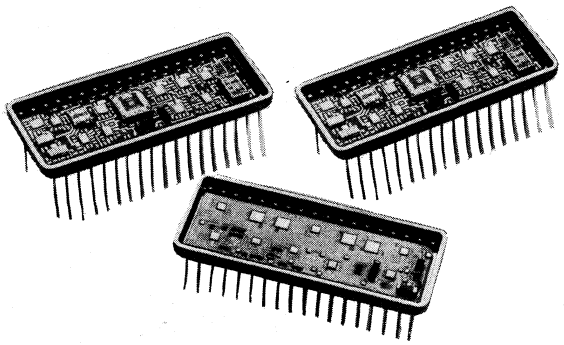
SDC – 19100 –000

- Accy: 1 = ±21 min (10 bit unit only); 2 = ±8.5 min (12 bit unit only); 3 = ±5.3 min (14 bit unit only); 4 = ±2.6 min (14 and 16 bit unit only); 5 = ±1.3 min (16 bit unit only)
- Reliability Grade: 0 = Standard
- Temp. Range: 1 = –30°C to +105°C; 3 = 0°C to +70°C
- Input: 0 = 11.8V, 400 Hz, Synchro, 26V Ref; 1 = 90V, 400 Hz, Synchro, 115V Ref; 3 = 90V, 60 Hz, Synchro, 115V Ref; 5 = 11.8V, 400 Hz, Resolver, 26V Ref; 6 = 11.8V, 2.4 KHz, Resolver, 26V Ref; 7 = 2.0V, 400 Hz, Direct, 26V Ref; 8 = 2.0V, 60 Hz, Direct, 26V Ref; 9 = 2.0V, 2.4 KHz, Direct, 26V Ref
- Resolution: 0 = 10 bits; 2 = 12 bits; 4 = 14 bits; 6 = 16 bits
- Family Code
- Signal Input Type: SDC = Synchro; RDC = Resolver; XDC = Direct

*See model selection chart for available models.

HSDC-360*

HYBRID TWO-SPEED TRACKING CONVERTER
Resolution to 20 Bits; Any Speed Ratio



DESCRIPTION

The HSDC-360 is an application of the hybrid control transformer and data processor modules in the HSDC-14 to form a two-speed tracking converter. A circuit diagram with a list of discrete components is provided so that a crossover detector and other required circuit elements can be added to two standard hybrid control transformer modules and one standard data processor module. The additional components and their interconnections determine the speed ratio and resolution of the converter. The circuit for a 1 and 36 speed converter with 16 bit output is described in the data sheet; circuit diagrams for other speed ratios and resolutions will be supplied on request.

The HSDC-360 has most of the characteristics listed in the description of the HSDC-14, including ratiometric conversion, phase sensitive detection, broadband inputs, and DC analog velocity output. The power supply voltage ranges are the same, and the −15V power supply can also be eliminated with a trade-off reduction in the maximum tracking rate.

The accuracy of the HSDC-360 depends on the speed ratio and resolution, and on whether standard or high-accuracy control transformers are used. For a 16 bit, 1 and 36 speed converter the accuracy can be as high as ±1.2 LSB, including the ±1 LSB quantizing error.

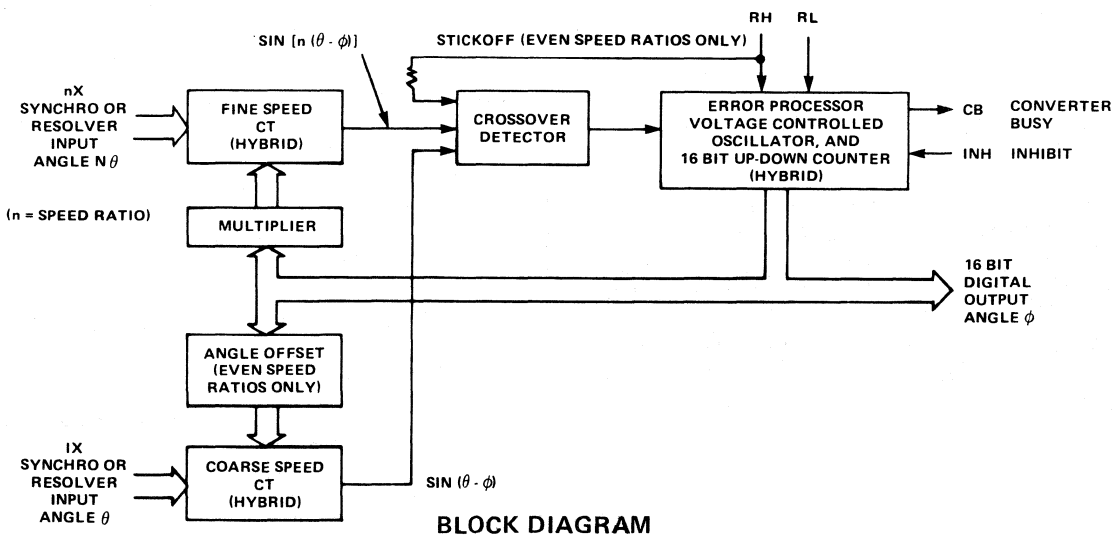
APPLICATIONS

The HSDC-360 may be used wherever analog angle data from a two-speed synchro or resolver system must be converted rapidly and accurately to digital form for transmission, storage, or analysis. Because of the small size, low weight, low power requirement, and high MTBF of its hybrid components, the HSDC-360 is well suited for remotely located and hard to access equipment. All hybrid modules are processed to MIL-STD-883 (burn-in is optional), and can be used in the most stringent industrial and military ground or avionics applications. Designed for printed circuit board mounting by standard techniques, the HSDC-14 can be readily incorporated into other equipment for computer control.

FEATURES

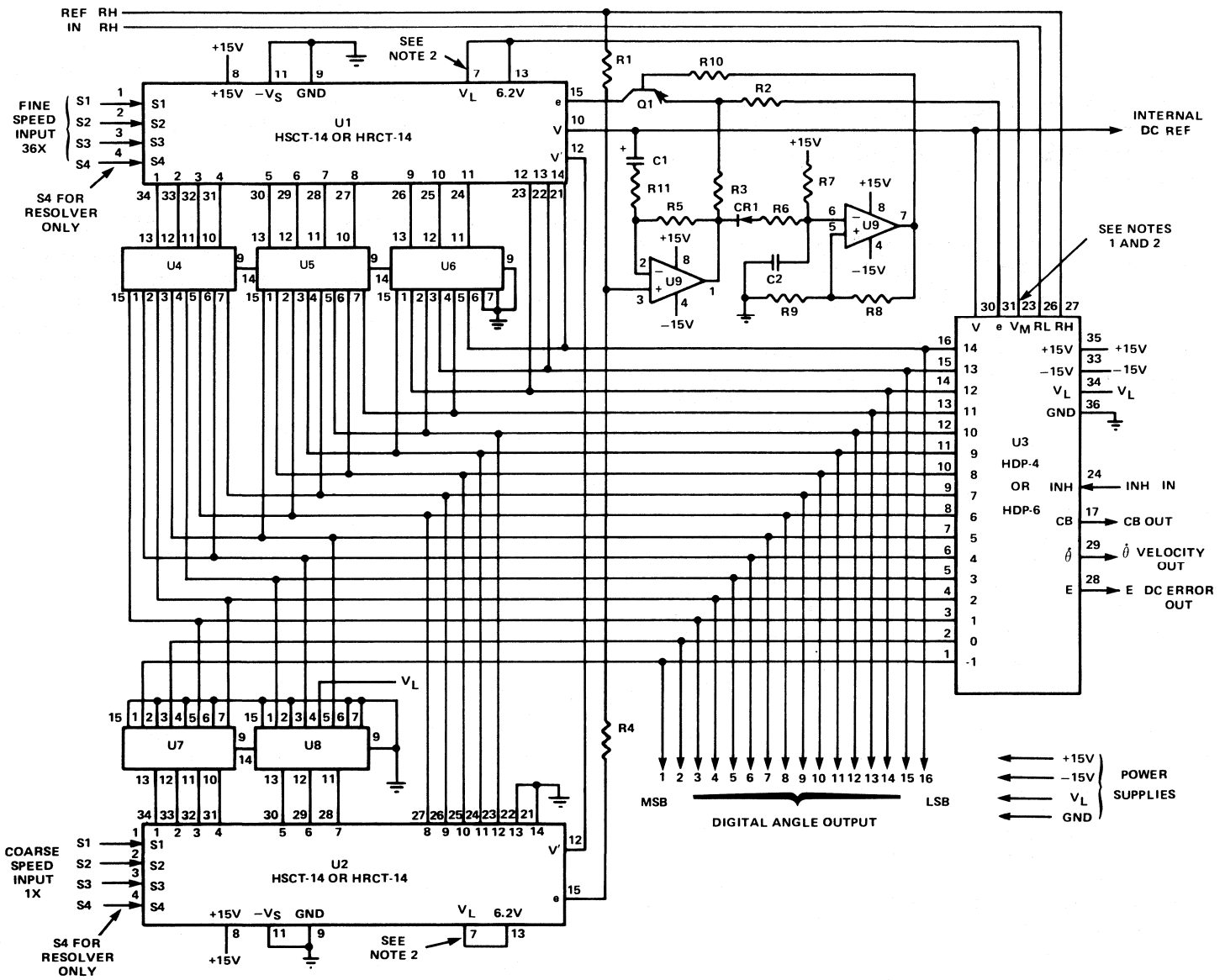
- *THREE STANDARD HYBRID MODULES PLUS DISCRETE COMPONENTS WIRED BY CUSTOMER TO DETERMINE SPEED RATIO AND RESOLUTION*
- *SIGNAL AND REF. INPUTS:*
  Internal solid state isolation or external isolation transformers
  All common synchro and resolver L-L voltage levels and frequencies
- *LOGIC:*
  TTL and CMOS compatible
  Up to 20 bit parallel binary angle output
  Converter Busy and Inhibit
- *POWER REQUIRED:*
  ±15V DC and logic voltage supply

*Patented



BLOCK DIAGRAM

CIRCUIT DIAGRAM FOR 16 BIT, 1:36 SPEED CONVERTER



NOTES:

1. Digital output drive capability is normally 2 standard TTL loads. If logic supply V_L = +5V for TTL interface and 4 unit load capability is desired, disconnect pin 23 (V_M) on U3 from 6.2V and connect it to +15V. Note that the Inhibit logic 1 is referred to V_M.

2. If the external logic supply voltage V_L is greater than 6.2V, do not connect pins 7 (V_L) on U1, U2 and pin 23 (V_M) on U3 to 6.2V. Instead, connect these three pins to the external logic supply V_L.

3. If signal isolation transformers are required, use HXCT-14 for U1, U2. See Interconnection Diagram in HSDC-14 data sheet for signal and reference transformer connections.

PARTS LIST:

U1, U2 = DDC hybrid control Transformers } See ordering
U3 = DDC hybrid data processor } information
U9 = 4558, dual op-amp
R1 = Coarse speed stickoff. Value depends on reference voltage level. R1 = 22 MΩ, 5% for 115V rms ref and R1 = 5.1 MΩ, 5% for 26V ref.
U4 – U8 = 4008, CMOS 4-bit adders.
U4, U5, U6 form 36X multiplier
U7, U8 form 1X angle offset
Coarse and fine speed loop gain
1% Resistors: R2 = 80.6 KΩ; R3 = 100 KΩ, R4 = 10 KΩ; R5 = 750 KΩ; R11 = 10 KΩ
C1 = 10μF, 6V DC
Crossover Detector
5% Resistors: R6 = 1 KΩ; R7, R8 = 1 MΩ, R9 = 200 KΩ, R10 = 30 KΩ
C2 = 0.1μF ceramic; CR1 - 1N4148
Crossover Switch
Q1 = 2N2946

TECHNICAL INFORMATION

INTRODUCTION

The applications information for the HSDC-360 has much in common with that for the HSDC-14, since the same control transformer and data processor modules are used. The HSDC-14 data sheet will be referenced frequently to avoid repeating information and diagrams.

The block diagram shows the main components of the HSDC-360. The multiplier, angle offset, stickoff resistor, and crossover detector are composed of discrete components.

The operation of a two-speed S/D is essentially the same as a single speed except there are two control transformers (CT) which generate two error voltages. These two CTs are fed by a common up-down counter with the counter data multiplied by the speed ratio for the fine speed CT.

Assuming an off-null condition, as when the system is first energized, the crossover detector feeds the coarse (1X) CT error signal output to the demodulator and error processor. The converter seeks a null as it would for a single speed S/D. As null is approached (to within 2.5° nominally) the coarse CT output drops below a preset threshold and the crossover detector then switches the fine speed CT error signal into the demodulator and error processor. Since the counter angle θ is multiplied by the speed ratio, the gradient of the fine speed CT is n times the coarse (1X) CT output. The servo loop then is able to seek an even finer null, using the fine speed CT error signal. The converter will continue to use the fine error signal for continuous tracking, swtiching back to the coarse signal only when the coarse error exceeds the crossover threshold. An angle offset and stickoff voltage are introduced in the coarse channel for even speed ratios in order to eliminate the false stable nulls which can occur when the fine and coarse speed angles are simultaneously at 180°.

MODULE INTERCONNECTIONS

A circuit diagram and list of components for a 16 bit 1:36 speed converter are given to illustrate the most common resolution and speed ratio. Interconnection layout is not critical. The analog outputs are derived from op-amps, have low output impedance, and are short circuit proof.

The output drive capability can be either 2 or 4 standard TTL loads as indicated in the Notes. The penalty for 4 TTL load capability is that the Inhibit input, which is internally connected to V_M by an 80 KΩ pull-up resistor, will be referenced to the +15V supply rather than to the logic supply voltage.

SIGNAL AND REFERENCE INPUTS AND TRANSFORMERS

All information listed under this section heading in the HSDC-14 data applies. Note especially the protective voltage suppressors that must be installed on all 90V L-L solid state input modules to prevent voltage transients from destroying the input resistor networks.

LOGIC INPUTS AND OUTPUTS

Logic outputs consist of 16 to 20 parallel data bits and a Converter Busy (CB). These outputs are short circuit proof to ground or to positive voltages as high as V_L.

Information about the Inhibit (INH) is given in the corresponding section of the HSDC-14 data.

ANALOG OUTPUTS

The analog outputs are V, e, E, and θ. V is an internal D.C. ground, +3.9V DC nominal, and is used as reference ground with the voltage follower buffer input option (HXDC). The other analog outputs, which ride on the D.C. reference V, are not used externally in normal operation.

The HSDC-14 data sheet describes the characteristics of the analog outputs e, E, and $\dot{\theta}$. The only difference for the HSDC-360 is the scaling for the velocity output $\dot{\theta}$. This scaling is given in the HSDC-360 specifications table.

TIMING AND DYNAMIC PERFORMANCE

The discussion and diagrams in the HSDC-14 data sheet concerning timing and dynamic performance apply to the HSDC-360 without modification.

SPECIFICATIONS

Apply over reference amplitude, temperature, and power supply ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	16 to 20 bits
ACCURACY	
Depends on Speed Ratio, Resolution and Whether Option "a" (±2 min) Is Used	$\frac{\pm 4 \text{ min (or 2 min)}}{\text{speed ratio}}$ ±0.9 LSB
Accuracy For 1:36 Speed Ratio and 16 Bit Resolution	±0.45 min with standard CT ±0.39 min with high accuracy CT
SPEED RATIO	Any speed ratio can be accommodated by an appropriate multiplier and angle offset made with discrete components. Consult factory for circuit diagram.
SIGNAL AND REFERENCE INPUT	
SOLID STATE BUFFER INPUT (HSCT AND HRCT UNITS)	
Carrier Frequency Range	47 – 1000 Hz
Synchro and Resolver Input Characteristics	
Voltage Options and Minimum Input Impedance (Balanced)	

Synchro (HSCT)	Z_{IN} Line to Line	Z_{IN} Each Line to Gnd
90V L-L (Option H)	130 KΩ	85 KΩ
11.8V L-L (Option L)	17.5 KΩ	11.5 KΩ

Resolver (HRCT)	Z_{IN} Single Ended	Z_{IN} Differential	Z_{IN} Each Line to Gnd
90V L-L (Option H)	175 KΩ	350 KΩ	175 KΩ
26V L-L Option M)	50 KΩ	100 KΩ	50 KΩ
11.8V L-L (Option L)	23 KΩ	46 KΩ	23 KΩ

Common Mode Range (DC Common Mode Plus Recurrent AC Peak)

	$-V_S = 0V$	$V_L = +6.2V$ and $-V_S = -7V$
90V L-L (Option H)	150V max	300V max
26V L-L (Option M)	45V max	90V max
11.8V L-L (Option L)	20V max	60V max

VOLTAGE FOLLOWER INPUT (FOR HXCT UNITS)	
Carrier Frequency Range	47 – 1000 Hz
Voltage Range	
$-V_S = 0V$	1V rms nominal; 1.15V max; 0.1V min
$V_L = +6.2$ and $-V_S = -7V$	3V rms nominal; 3.5V max; 0.1V min
Max Voltage Without Damage	15V rms continuous 100V peak transient
Input Impedance	$Z_{IN} > 10$ MΩ (transient protected voltage follower)
TRANSFORMER CHARACTERISTICS (FOR HXCT UNITS)	
400 Hz TRANSFORMERS	
Reference Transformer (Optional for Both Solid State and Transformer Input Options)	
Carrier Frequency Range	Option 4 = 360 – 1000 Hz
Voltage Range	18 – 130V
Input Impedance	40 KΩ min
Breakdown Voltage to GND	1200V peak
Signal Transformer	
Carrier Frequency Range	Option 4 = 360 – 1000 Hz
Minimum Input Impedances (Balanced)	

	Synchro Z_{IN} (Z_{SO})	Resolver Z_{IN}
90V L-L (Option 4H)	180 KΩ	100 KΩ
26V L-L (Option 4M)	–	30 KΩ
11.8V L-L (Option 4L)	20 KΩ	30 KΩ
Breakdown Voltage to GND	700V peak	

PARAMETER	VALUE
60 Hz TRANSFORMERS	
Reference Transformer (Optional for Both Solid State and Voltage Follower Input Options)	
Carrier Frequency Range	47 – 440 Hz
Input Voltage Range	80 – 138V rms; 115V rms nominal
Input Impedance	600 KΩ min, resistive
Input Common Mode Voltage	±500V rms, transformer isolated
Output Description	+R (in phase with RH-RL) and -R (in phase with RL-RH) derived from op-amps. Short circuit proof.
Output Voltage	3.0V nominal riding on DC reference V. Output voltage level tracks input level.
Power Required	4 mA typ, 7 mA max from +15V supplies.
Signal Transformer	
Carrier Frequency Range	47 – 440 Hz
Input Voltage Range	10 – 100V rms; L-L 90V rms L-L nominal
Input Impedance	148 KΩ min L-L balanced resistive
Input Common Mode Voltage	±500V rms, transformer isolated
Output Description	Resolver output ±sine (±S) and ±cosine (–C) derived from op-amps. Short circuit proof
Output Voltage	1.0V rms nominal riding on DC reference V. Output voltage level tracks input level.
Power Required	4 mA type 7 mA max from +15V supply
DIGITAL INPUT/OUTPUT	
Logic Type	TTL/DTL/CMOS compatible, depending on logic supply voltage
Outputs	
14 Parallel Data Bits	Natural binary angle positive logic
Converter Busy (CB)	1.5 – 3μs positive pulse, leading edge initiates counter update
Drive Capability	2 or 4 standard TTL loads
Inhibit Input (INH)	$Z_{IN} > 80$ KΩ pull-up resistor to V_M (V_M = logic supply voltage or ±15 supply voltage. See Interconnection Diagrams.)
ANALOG OUTPUTS	
Internal D.C. Ref. (V)	+3.9 VDC nominal
AC Error Voltage (θ)	0.38 mV rms per LSB of error
DC Error Voltage (E)	–1 VDC per ± LSB of error
DC Velocity Voltage (θ)	
For 16 Bit Resolution	+1.0V DC per +112°/sec at 400 Hz +1.0V DC per +28°/sec at 60 Hz
For Higher Resolutions	Scales according to number of bits. At 400 HZ for instance, a 1.0V DC θ output corresponds to 28°/sec at 16 bits and 7°/sec at 20 bits.
DYNAMIC CHARACTERISTICS	
Input Rate For Full Accuracy	
For 16 Bit Resolution	
At 400 Hz	0 to ±2.5 rps min
At 60 Hz	0 to ±0.625 rps min
For Higher Resolutions	Maximum input rate scales according to number of bits: 1/4 at 18 bits, and 1/16 at 20 bits.
Velocity Constant	$K_V = \infty$ (No limitation with Type II servo loop)
Acceleration Constant	
At 400 Hz	$K_a = 58{,}000$ sec^{-2} nominal
At 60 Hz	$K_a = 3{,}600$ sec^{-2} nominal
Settling Time	
For Normal Tracking	No lag error up to specified input rates
For 179° Step Change with 1:36 Speed Ratio	
At 400 Hz	270 msec typ to 1 LSB 350 msec max to final value
At 60 Hz	1080 msec typ to 1 LSB 1400 msec max to final value
For 179° Step Change With Other Speed Ratio	Consult factory. Depends on slew rate and small signal settling time.

SPECIFICATIONS

PARAMETER	VALUE
TEMPERATURE RANGES	
Operating	
–1 option	–55°C to +125°C
–3 option	0°C to +70°C
Storage	–55°C to +135 °C
POWER SUPPLIES	
Nominal Voltage	+15 VDC / –15 VDC / Logic Supply
Voltage Range	+11 to +16.5V / 0 to –16.5V / +4.5V to +15 supply
Absolute Max Voltage	+18V / –18V / +18V
Current or Impedance	70 mA max* / 20 mA max* / Z_{IN} – 10 KΩ min

*Does not include current required by 60 Hz active transformers.

PARAMETER	VALUE
PHYSICAL CHARACTERISTICS	
Converter Module and Data Processor Module	
Type	36 pin double DIP
Size	0.78 x 1.9 x 0.21 inch (2.0 x 4.8 x 0.53 cm)
Weight	1 oz max (28 g)
400 Hz Transformer Modules	
Type	Encapsulated module. Signal input uses 2 modules (T1A and T2B) Ref uses 1 module (T2)
Size	0.8 x 0.6 x 0.3 inch (2 x 1.5 x 0.8 cm)
Weight	0.4 oz max (11 g)
60 Hz Transformer Modules	
Type	Encapsulated module.Signal transformer and reference transformer each consist of one such module
Size	1.125 x 1.125 x 0.42 inch (2.86 x 2.86 x 1.07 cm)
Weight	0.7 oz max (20 g)

ORDERING INFORMATION

Order two hybrid control transformers and one hybrid data processor. DDC does not supply the discrete components for the angle multiplier, angle offset, and stickoff.

1. Order two control transformers as follows. These units operate over the full 47–1000 Hz frequency range. Transformers for HXCT-14 units must be ordered separately as described below.

HSCT–14–H–1–a–883B

- 883B: MIL-STD-883 Processing: 883B = Conforms to MIL-STD-883 DDC procedures; Blank = Same, except pre burn in test and burn in are omitted.
- a: Accuracy: Blank = ±4 minutes; a = ±2 minutes
- 1: Temperature Range (Operating): 1 = –55°C to +125°C; 3 = 0°C to +70°C
- H: Voltage Levels: 1. Synchro solid state input (HSCT): H = 90V L-L; L = 11.8V L-L. 2. Resolver solid state input (HRCT): H = 90V L-L; M = 26V L-L; L = 11.8V L-L. 3. Voltage follower input (HXCT): Omit voltage level specification. One HXCT model accepts all normal voltage levels.
- 14: Resolution = 14 Bits
- HSCT: Input Type: HSCT = Solid state synchro; HRCT = Solid state resolver; HXCT = Voltage follower buffer. Requires external signal conditioner such as an isolation transformer.

2. Order one data processor as follows:

HDP - 4 - 1 - 883B

- 883B: MIL-STD-883 Processing: 883B = Conforms to MIL-STD-883 DDC procedures; Blank = Same, except pre burn in test and burn in are omitted.
- 1: Temperature Range: 1 = –55°C to +125°C; 3 = 0°C to +70°C
- 4: Carrier Frequency Range: 4 = 360–1000 Hz; 6 = 47–1000 Hz

3. Isolation transformers for CT modules with voltage follower buffer inputs (HXCT-14) must be ordered separately by part number.

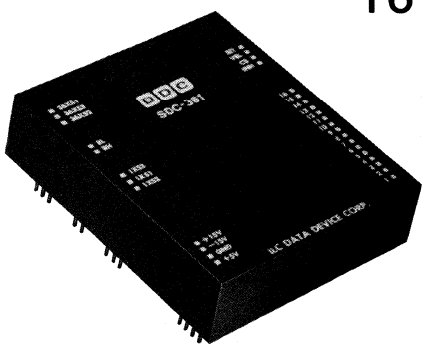
Type	Frequency	Ref. Voltage	L-L Voltage	Part Numbers Ref. Xfmr.	Part Numbers Signal Xfmr.
Synchro	400 Hz	115V	90V	21049	21045*
Synchro	400 Hz	26V	11.8V	21049	21044*
Resolver	400 Hz	115V	90V	21049	21048*
Resolver	400 Hz	26V	26V	21049	21047*
Resolver	400 Hz	26V	11.8V	21049	21046*
Synchro	60 Hz	115V	90V	24133	24126*

*The part number for each 400 Hz synchro or resolver isolation transformer includes two separate modules as shown in the outline drawings.

MECHANICAL OUTLINES

Mechanical outlines, pin assignments, and schematic diagrams for the control transformer and error processor modules and for all transformers can be found on the HSDC-14 data sheet.

16 BIT TWO-SPEED S/D AND R/D CONVERTER
Single Module with Internal Transformers



DESCRIPTION

The SDC-361 is a low-cost, single module synchro to digital and resolver to digital tracking converter. A unique control transformer algorithm is used that provides inherently higher accuracy and jitter-free output. Other features include a BIT logic signal to indicate proper tracking and an analog velocity output. Utilizing a type II servo loop, these converters have no velocity lag up to the specified tracking rate, and output data is always fresh and continuously available. Each unit is fully trimmed and requires no adjustments.

APPLICATIONS

The SDC-361 may be used wherever analog angle data from 1 and 36 speed† synchros or resolvers must be converted rapidly and accurately to digital form for transmission, storage or analysis. Because these units are extremely rugged and stable, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial, commercial and military applications. Military ground support and avionics uses include ordnance control, radar tracking systems, navigation and collision avoidance systems.

FEATURES

- *ACCURACY: ±1 LSB = 20 seconds*
- *SIGNAL AND REF INPUTS:*
  Internal transformer isolation
  Broadband input: 350–3000 Hz or 47–3000 Hz
  All common L-L voltage levels
- *LOGIC:*
  TTL compatible
  16 bit parallel binary angle output
  Converter Busy, Inhibit and BIT
- *POWER REQUIRED:*
  ±15V DC and +5V DC

† All references to 1 and 36 speed apply to SDC-361. SDC-362 is 1 and 18 speed.

SPECIFICATIONS

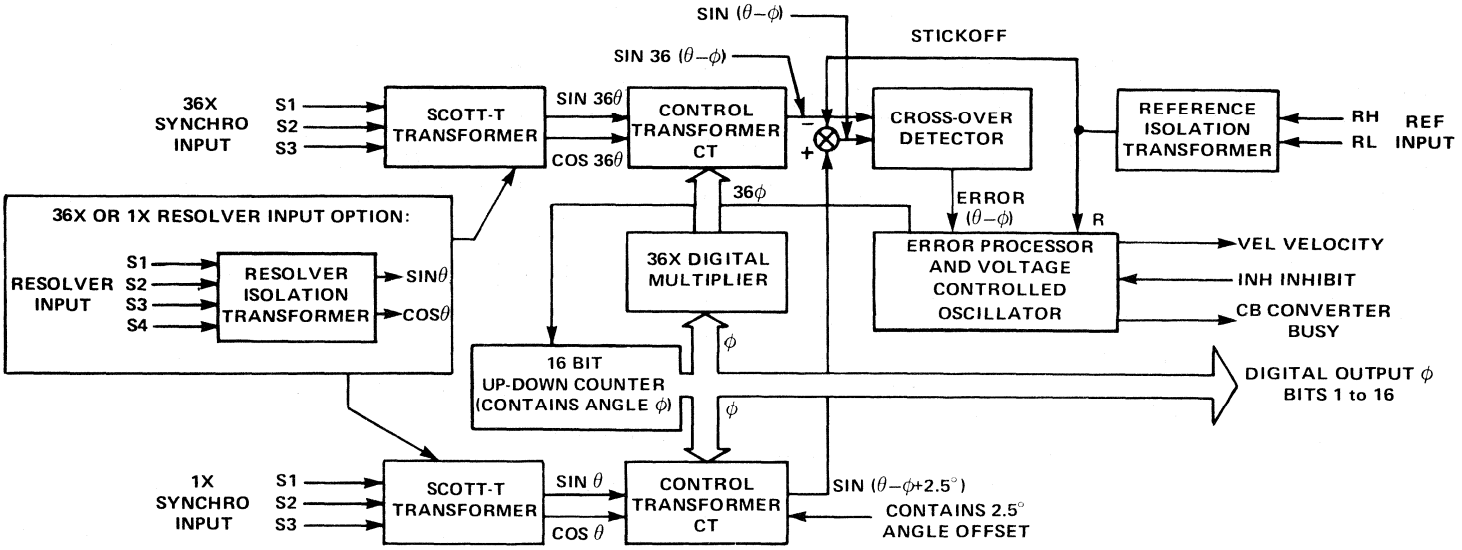
Apply over temperature range, power supply range, reference frequency range, ±10% signal & reference amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	16 bits
ACCURACY	
SDC-361	±1 LSB (20 sec)
SDC-362	±2 LSB (40 sec)
SIGNAL AND REFERENCE INPUT	
Synchro Input*	Signal Frequency Range / Signal Input Impedance (L-L Balanced, Resistive)
90V L-L, 400 Hz (Option H)	350–3000 Hz / 148 KΩ min
90V L-L, 60 Hz (Option I)	47–3000 Hz / 148 KΩ min
11.8V L-L, 400 Hz (Option L)	350–3000 Hz / 19 KΩ min
Resolver Input*	
90V L-L, 400 Hz (Option H)	350–3000 Hz / 148 KΩ min
26V L-L, 400 Hz (Option M)	350–3000 Hz / 42 KΩ min
11.8V L-L, 400 Hz (Option L)	350–3000 Hz / 19 KΩ min
Reference Input*:	Reference Voltage Range / Ref. Input Impedance (Resistive)
Options H, I	40–150V rms / 300 KΩ min
Options M, L	10–50V rms / 80 KΩ min
*Transformer isolated. Other voltages and frequencies available on special order.	
DIGITAL INPUT/OUTPUT	
Logic Type	TTL
Inhibit Input (INH)	Logic "0" inhibits
Loading	0.2 Std. TTL loads plus 18 KΩ min pull-up resistor to +5V supply
Outputs	
16 Parallel Data Bits	Natural binary angle; positive logic
Converter Busy (CB)	1–2.5μsec positive pulse data changes on leading edge
Drive Capability	2 Std. TTL loads (5 Std. load capability available on special order – consult factory)
Bit (Built In Test)	Logic 0 = normal tracking Logic 1 = not tracking within fine speed range
ANALOG VELOCITY OUTPUT	
Scale Factor	±1.0V DC ±30% for 100°/sec at 400 Hz ±1.0V DC ±30% for 25°/sec at 60 Hz
Range	±10V DC min
Loading	±10 KΩ max

PARAMETER	VALUE
DYNAMIC CHARACTERISTICS	
Input Rate for Full Accuracy	
Options H, M, L (400 Hz)	0–1000°/sec minimum
Option I (60 Hz)	0–250°/sec minimum
Acceleration for 1 LSB Lag	
Options H, M, L (400 Hz)	384°/sec² typ
Option I (60 Hz)	23°/sec² typ
Settling Time	
For Normal Tracking (Up to Specified Input Rate)	No lag error
For 179° Step Change (Typical Values)	
Options H, M, L (400 Hz)	
Settling to 1 LSB	400 msec
Settling to Final Value	480 msec
Option I (60 Hz)	
Settling to 1 LSB	1400 msec
Settling to Final Value	1800 msec
Velocity Constant (Type II Servo Loop)	$K_V = \infty$
Acceleration Constant	–
Options H, M, L (400 Hz)	K_A = 70,000 nominal
Option I (60 Hz)	K_A = 4,300 nominal

POWER SUPPLIES			
Nominal Voltage	+15V Supply	–15V Supply	+5V Logic Supply
Voltage Range	+11 to +16.5V	–11 to –16.5V	+4.5 to +5.5V
Max. Voltage Without Damage	+18V	–18V	7V
Current			
Typical	10 mA	35 mA	110 mA
Maximum	15 mA	50 mA	150 mA

PARAMETER	VALUE
TEMPERATURE RANGES	
Operating	
–1 Option	–55°C to +105°C
–3 Option	0°C to +70°C
Storage	–55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size (Encapsulated Module)	3.125 x 2.625 x 0.82 inch (79.4 x 66.7 x 20.8mm)
Weight	7 oz (200 g)



NOTE: Block Diagram Illustrates SDC-361. All References to "36x" are "18x" for SDC-362.

BLOCK DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION

The operation of a two-speed S/D is essentially the same as a single speed except there are two control transformers (CT) which generate two error voltages. These two CTs are fed by a common up-down counter with the counter data multiplied by 36 for the fine speed CT.

Assuming an off-null condition, as when the system is first energized, the crossover detector feeds the coarse (1X) CT error signal output to the demodulator and error processor. The converter seeks a null as it would for a single speed S/D. As null is approached (to within 2.5° nominally) the coarse CT output drops below a preset threshold and the crossover detector then switches the fine (36X) CT error signal into the demodulator and error processor.* Since the counter angle θ is multiplied by 36, the gradient of the fine speed CT is 36X the coarse (1X) CT output. The servo loop then is able to seek an even finer null, using the fine speed CT error signal. The converter will continue to use the fine error signal for continuous tracking, switching back to the coarse signal only when the coarse error exceeds the crossover threshold. In order to eliminate false stable nulls of 180° an angle offset and stickoff voltage are introduced in the coarse channel.

The ±15V power supplies can vary over their specified ranges with no change in the converter specifications except for a proportional change in the maximum ± tracking rates. When testing or evaluating the converters, it is advisable to limit the current to each of the three power supplies. Set each limit to 50% greater than the maximum current listed for that supply in the specifications table.

To prevent damage to the input transformers, the maximum voltage should not exceed the specified input voltage by more than 30%. The maximum common mode voltage (DC plus recurrent AC peak) should not exceed 500V.

***SDC-362 is (18x) where all references to (36x) occurs in text and diagrams.**

DIGITAL OUTPUTS

Logic outputs are low power Schottky and they can drive remote loads.

The BIT logic output is a built in test derived from the crossover detector. It goes to logic 1 whenever the digital output is not tracking the input signal within the range of the fine speed synchro or resolver.

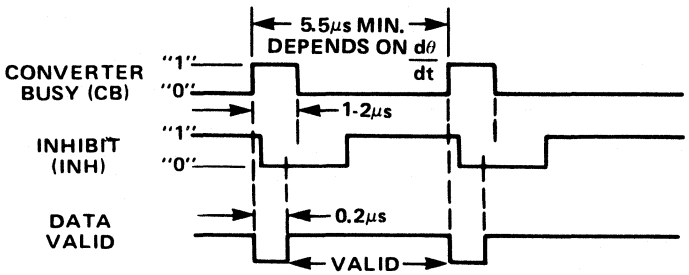
Bit	Deg/Bit	Min/Bit
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	108.75
8	1.405	84.38
9	0.7081	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0379	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	.66
16	0.0055	.33

BIT WEIGHT TABLE

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a converter busy pulse (CB). The output data change is initiated at the leading edge of the CB pulse, and the output is stable within 0.2μsec after the leading edge. Extra CB pulses will not occur if the input angle changes while the counter is locked by the INH.

The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the inhibit is applied. The converter will ignore an inhibit applied during the "busy" interval until that interval is over. Timing is as follows: (a) apply the inhibit, (b) wait 0.2μsec, (c) transfer the data, and (d) release the inhibit.



TIMING DIAGRAM

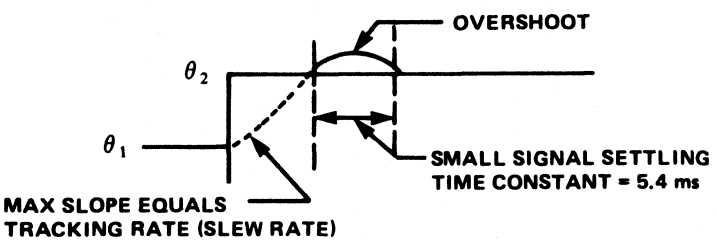
ANALOG VELOCITY OUTPUT

VEL is a DC voltage proportional to the angular velocity $d\theta/dt = d\phi/dt$. The output is derived from an op-amp with low output impedance and is short circuit proof. Other characteristics are listed in the specifications table.

DYNAMIC PERFORMANCE

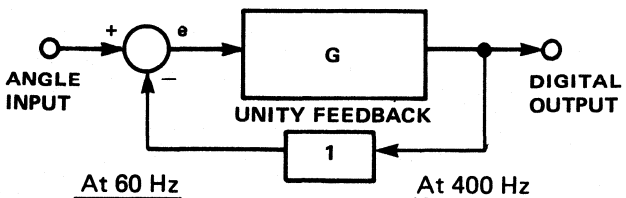
A Type II servo loop ($K_V = \infty$) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltages are not the ±15 VDC nominal values, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage. The +15V supply voltage will determine the positive maximum velocity, and the −15V supply voltage will determine the negative maximum velocity.

So long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal setting time.



RESPONSE TO A STEP INPUT

The loop dynamics of DDC's tracking S/D converters are described by the unity feedback configuration shown. The closed-loop transient response is nominally critically damped, and all loop dynamics can be determined from the diagram and formulas given.



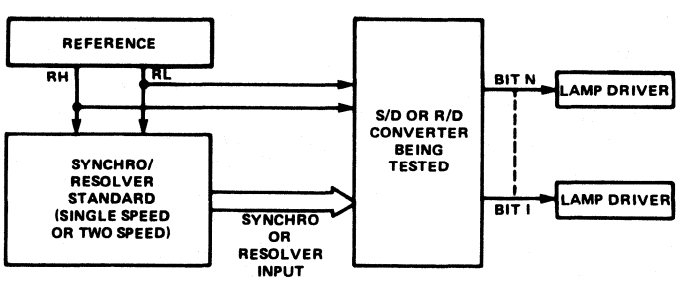
$$\text{At 60 Hz}\quad G = \frac{66^2\left(\frac{S}{33}+1\right)}{S^2\left(\frac{S}{330}+1\right)} \qquad \text{At 400 Hz}\quad G = \frac{266^2\left(\frac{S}{133}+1\right)}{S^2\left(\frac{S}{1330}+1\right)}$$

S/D CONVERTER LOOP DYNAMICS

ACCURACY TESTS

Because of the high accuracy of DDC's S/D converters, only laboratory-grade synchro or resolver substitution boxes or standards should be used. If synchro standards are not available, arrangements may be made to witness the final source inspection at the DDC factory.

The figure below shows how to arrange test equipment for measuring the accuracy of S/D converters. A separate lamp driver or suitable readout is required for each of the output data lines. The synchro standard is set to any desired test angle, and the lamps which are on are added according to their bit weights and compared with the test angle.



ACCURACY TEST CIRCUIT

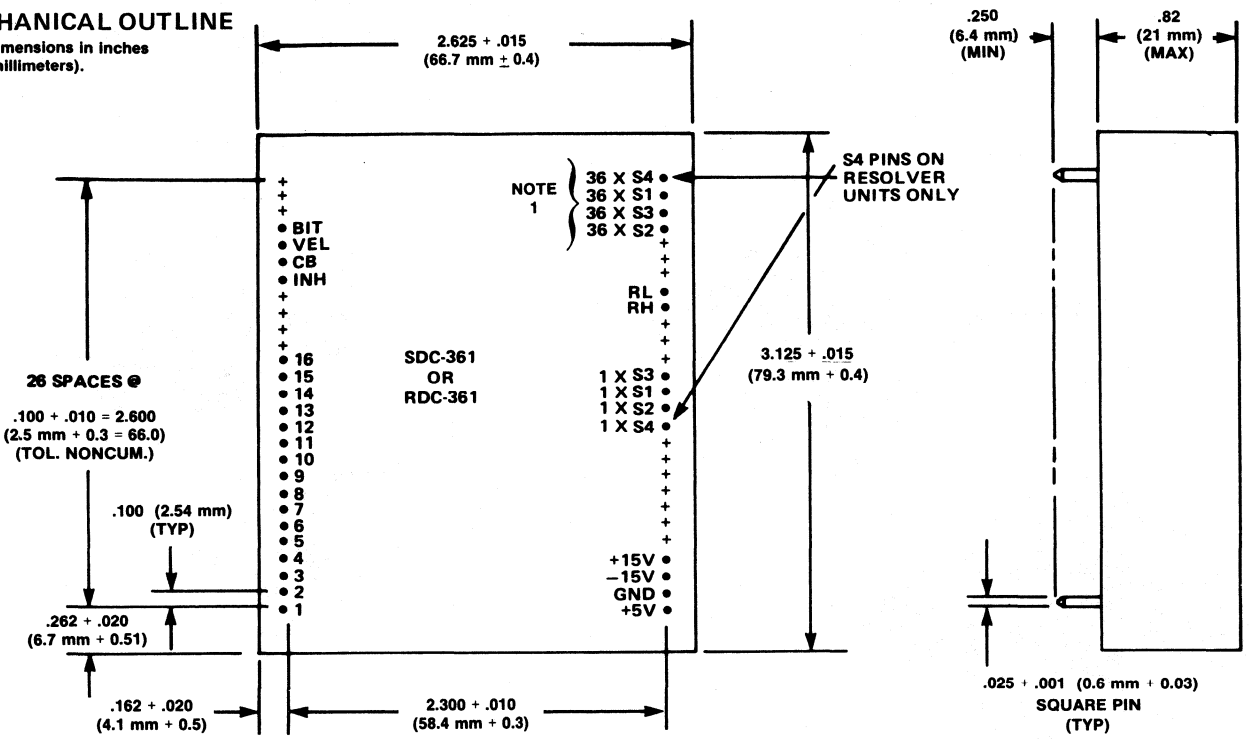
PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc.

It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a pin connection by ripping out the plated through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.

MECHANICAL OUTLINE

Dimensions in inches
(millimeters).



BOTTOM VIEW

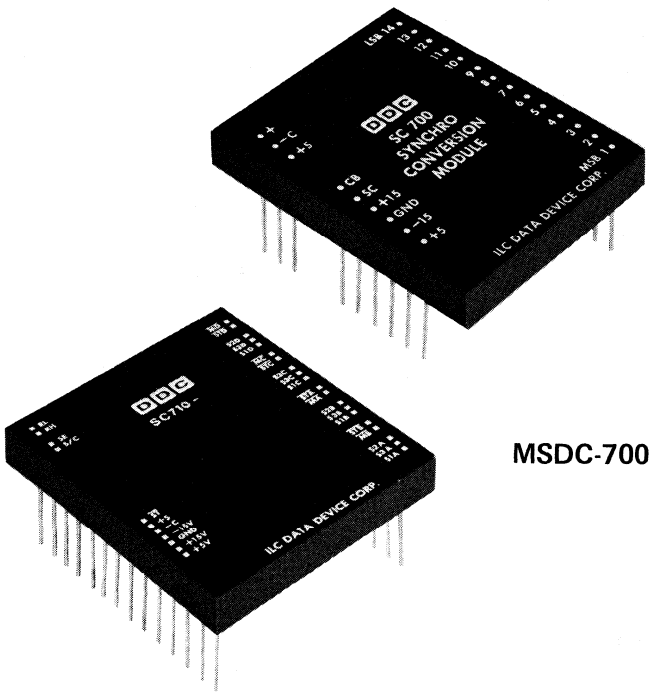
NOTES:
1. All reference to 36x become 18x on model SDC-362
2. Pin labels on bottom view are for reference only.
3. All dimensions shown are in inches.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type sdg-F.
6. Pins S4 are present on resolver units only.

ORDERING INFORMATION

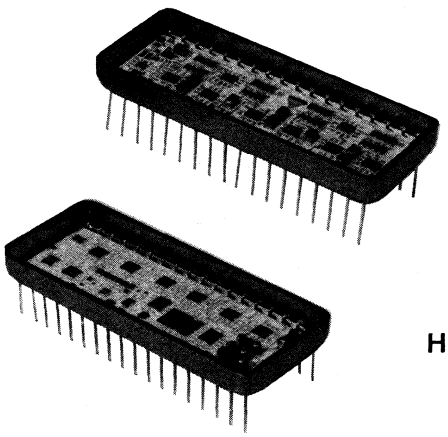
SDC – 361 – H – 1

- Temperature Range:
  1 = –55° C to +105° C
  3 = 0° C to +70° C
- Signal Input Voltage and Frequency:
  H = 90 V L-L, 400 Hz (Synchro or Resolver)
  I = 90 V L-L, 60 Hz (Synchro only)
  M = 26 V L-L, 400 Hz (Resolver only)
  L = 11.8 V L-L, 400 Hz (Synchro or Resolver)
- Speed:
  361 = 1 x 36 Speed
  362 = 1 x 18 Speed
- Input Type:
  SDC = Synchro
  RDC = Resolver

MULTIPLEXED 14 BIT S/D AND R/D CONVERTERS
New Design Requires Fewer Modules



MSDC-700



HMSDC-8700

FEATURES

- *SIMULTANEOUS SAMPLING AND RANDOM ACCESS*
- *SUPERIOR ALGORITHM GIVES INHERENTLY HIGH ACCURACY*
- *ONLY TWO TYPES OF MODULES 4 channel input module and central converter*
- *MODULES AVAILABLE IN DISCRETE OR HYBRID FORM*

DESCRIPTION

These two new series of multiplexed S/D and R/D converters are cost effective because they require fewer components and interconnections. Since each input module contains four signal channels, and the central converter is complete in one module, a 4 channel system can be made with only two modules. All common synchro and resolver line-to-line voltages and frequencies are available, and signal and reference input channels can be interconnected in any combination.

Discrete and hybrid modules can be used together because they are electrically interchangeable. Modules in the discrete MSDC-700 series are low profile (0.43 inch high) and low cost. They feature internal isolation transformers at both 60 Hz and 400 Hz. Modules in the hybrid HMSDC-8700 series have the small size, low weight, and high reliability of thick-film hybrids. They feature differential solid-state signal and reference inputs with substantial common mode rejection so that transformer isolation is not usually required.

APPLICATIONS

Multiplexed S/D and R/D converters can be used when multiple synchro or resolver inputs are sampled for digital computation or display, and real time tracking is not required. Multiplexing is found in data logging systems, process monitors, ordnance aiming controls, navigation systems, numerical control, and range instrumentation. The synchro and resolver inputs often represent variables which are analyzed by a computer for monitoring or control.

*Patented

SPECIFICATIONS

Apply over reference frequency, reference amplitude, temperature and power supply ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY	±4.6 minutes ± 1/2 LSB
DYNAMIC CHARACTERISTICS	
Signal Sample Rate at Each Signal Input Channel	Once per cycle of the reference processor controlling that input channel.
Conversion Time, Per Channel	120-150 μsec
Number of Conversions per Carrier Cycle	
At 400 Hz	15 max
At 60 Hz	100 max
Channel Access	Random, one address per line per channel

ANALOG INPUT CHARACTERISTICS FOR DISCRETE UNITS, MSDC-700

Input Type	Transformer isolation, both reference and signal inputs. Input impedance is maintained with power off.		
Breakdown Voltage	500V min to ground		
Reference and Signal Characteristics	Min Z_{IN} L-L (Balanced, Resistive)	Ref Input Voltage (±20%)	Min Ref Z_{IN} (Resistive)
Synchro Input			
11.8V L-L, 360–440 Hz (SC-710)	19 KΩ	26V rms	40 KΩ
90V L-L, 360–440 Hz (SC-711)	148 KΩ	115V rms	160 KΩ
90V L-L 47-440 Hz (SC-715) Reference 47-66 Hz	148 KΩ	115V rms	160 KΩ
Resolver Input			
11.8V L-L, 360-440 Hz (SC-712)	26 KΩ	26V rms	40 KΩ
26V L-L, 360-440 Hz (SC-713)	57 KΩ	26V rms	40 KΩ
90V L-L, 360-440 Hz (SC-714)	198 KΩ	115V rms	160 KΩ

ANALOG INPUT CHARACTERISTICS FOR HYBRID UNITS, HMSDC-8700

Input Type	Differential solid state. Input impedance is maintained with power off.
Frequency Range*	47–440 Hz
Reference Voltage Range	10–150V RMS
Reference Input Impedance	Single ended: 1.5 MΩ min Differential: 3 MΩ min.
Reference Common Mode Range	DC common mode plus recurrent AC peak: 210V max

Signal Input Minimum Impedance (Balanced, Resistive)

	Z_{in} Line-to-Line	Z_{in} Each Line to GND
Synchro*		
11.8V L-L (SC-8710)	17.5 KΩ	11.5 KΩ
90V L-L (SC-8711)	130 KΩ	85 KΩ

	Z_{in} Single Ended	Z_{in} Differential	Z_{in} Each Line to GND
Resolver*			
11.8V L-L (SC-8712)	23 KΩ	46 KΩ	23 KΩ
26V L-L (SC-8713)	50 KΩ	100 KΩ	50 KΩ
90V L-L (SC-8714)	175 KΩ	350 KΩ	175 KΩ

Signal Common Mode Ranges	
For 90V L-L Input	150V max } DC common mode plus recurrent AC peak
For 26V L-L Input	50V max }
For 11.8V L-L Input	25V max }

*Other voltages and frequencies available – consult factory.

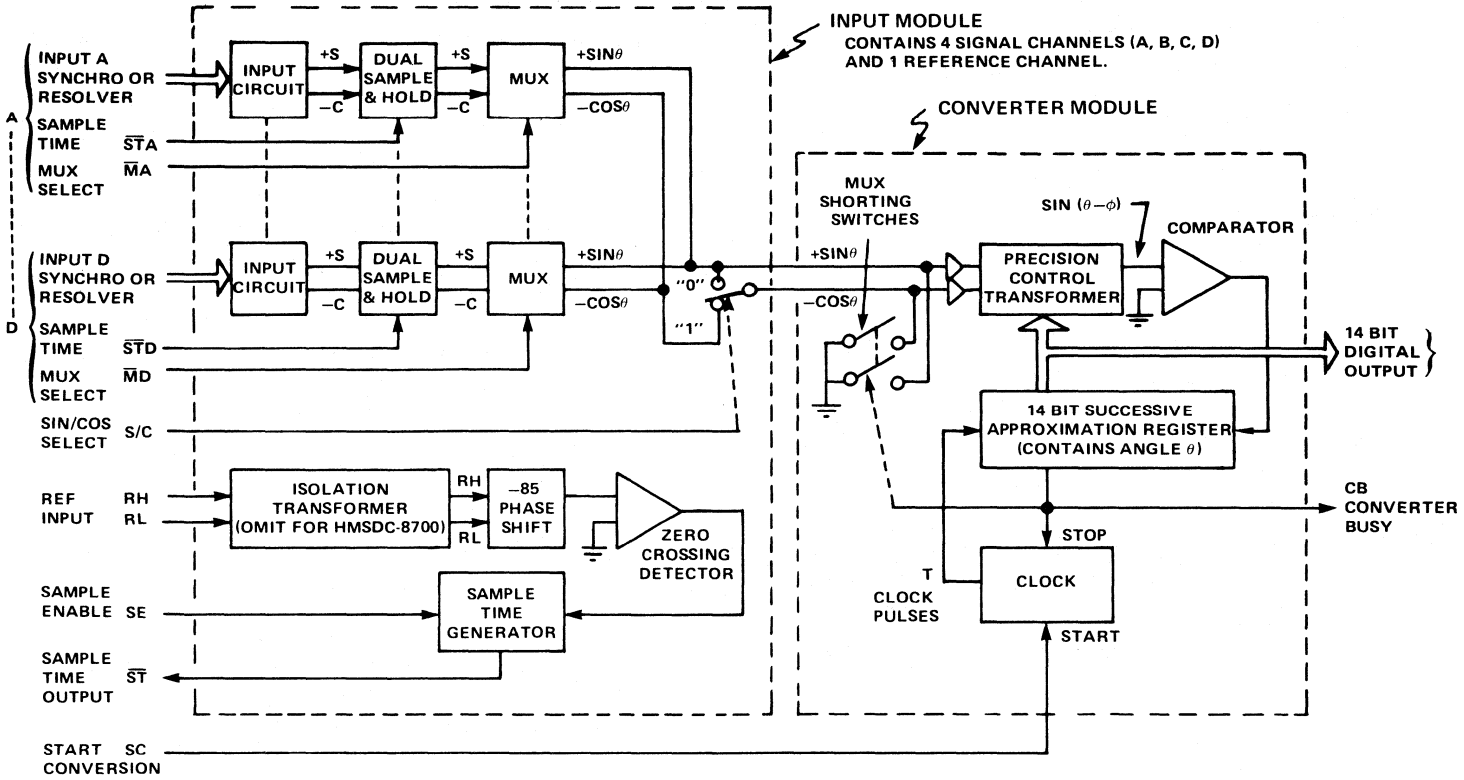
PARAMETER	VALUE			
DIGITAL INPUTS	Input Type	Internal Pullup to +5V (min)	Std TTL Load (Includes Pullup)	Description
System Inputs				
Start Convert (SC)				1–4μsec positive pulse; leading edge initiates conversion
Discrete (SC 700)	LS TTL	–	0.2	
Hybrid (SC 8700)	LS TTL	27 KΩ	0.4	
Mux Select ($\overline{MA}$, $\overline{MB}$, $\overline{MC}$, $\overline{MD}$)	CMOS	40 KΩ	0.08	Logic 0 selects channel; must start within 1 μsec of SC and remain until conversion is complete (CB=0)
Sample Enable (SE)	CMOS	40 KΩ	0.08	Logic 0 inhibits sample time pulse (ST) from ref channel; ST resumes when SE returns to logic 1.
Sin/Cos Select (S/C)	CMOS	40 KΩ	0.08	Switches cos output line on input module between cos output (logic 1) and sin output (logic 0); for interfaces not using central converter.
Interconnection Inputs				
Sample Time Input ($\overline{STA}$, $\overline{STB}$, $\overline{STC}$, $\overline{STD}$)	CMOS	40 KΩ	0.08	Gate control for sample/hold; connected by user to ST output from any ref channel.
+ Input	LS TTL	27 KΩ	0.3	Normally tied to +5V

DIGITAL OUTPUT	Output Type	Drive capab. STD TTL Loads	Description
System Outputs			
14 Parallel Data Bits	LP TTL	2	Natural binary angle; positive logic
Converter Busy (CB)	CMOS	2	150 μsec max; logic 1 during conversion
Interconnection Outputs			
Sample Time Output ($\overline{ST}$)	CMOS	0.2	Drives up to 8 sample/hold gates; connnected by user to ST inputs in any signal channel. Negative pulse, 50 μsec nominal, 40 μsec min, 70 μsec max. $\overline{ST}$ pulse is automatically initiated close to the positive peak in each ref cycle.

TEMPERATURE RANGES	
Operating	
–1 Option	–55°C to +105°C
–3 Option	0°C to +70°C
Storage	
Discrete (MSDC-700)	–55°C to +125°C
Hybrid (HMSDC-8700)	–55°C to +135°C

POWER SUPPLIES			
Nominal Voltage (±5%)	+5 VDC	+15 VDC	–15 VDC
Max Voltage Without Damage	+7 VDC	+18 VDC	–18 VDC
Current in mA			
Central Converter (SC700, SC8700)	58 nom 83 max	9 nom 15 max	8 nom 14 max
Input Modules (SC710-715, SC8710-8714)	3 nom 5 max	15 nom 24 max	14 nom 23 max

PHYSICAL CHARACTERISTICS	
Discrete Units	
Type	Encapsulated module; each contains either a central converter or 1 ref plus 4 signal input channels.
Size, Each Module	3.125 x 2.625 x 0.43 inch (7.94 x 6.67 x 1.09 cm)
Weight, Each Module	4 oz. (114 g)
Hybrid Units	
Type	36 pin double DIP; each module contains either a central converter or 1 ref plus 4 signal input channels.
Size, Each Module	1.9 x 0.78 x 0.21 inch (4.83 x 1.98 x 0.53 cm)
Weight, Each Module	1 oz. max (28 g)



BLOCK DIAGRAM
MSDC-700 AND HMSDC-8700

TECHNICAL INFORMATION

INTRODUCTION AND BLOCK DIAGRAM

Each multiplexed system consists of one converter module and one or more signal input modules. The block diagram shows one input module connected to one converter module. The input module contains four signal input channels A, B, C, D and one reference input channel.

Each synchro or resolver is connected to a separate input channel, and each reference to a reference channel. In the discrete MSDC-700 series the input circuit is either a resolver isolation transformer or a Scott-T transformer. In the hybrid HMSDC-8700 series the input circuit is either a solid state buffer or a solid state Scott-T.

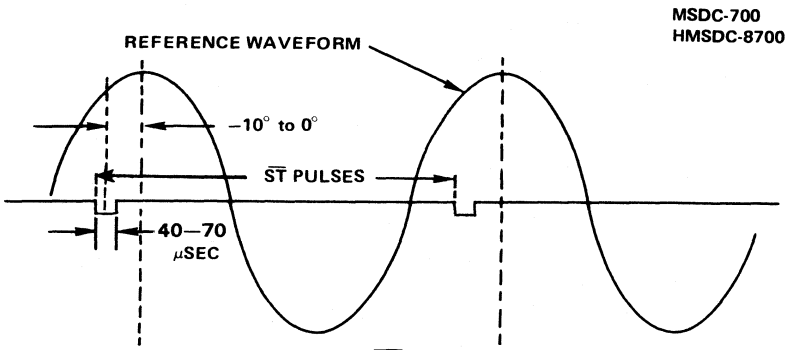
If several synchro or resolvers share a reference, they will also share a reference input channel. The purpose of the reference input channel is to produce the sample time pulse $\overline{ST}$. The $\overline{ST}$ output from each reference channel can be connected to the sample time inputs $\overline{STA}$. . . $\overline{STD}$ in up to 8 input channels. Each $\overline{ST}$ pulse causes the dual sample/holds to which it is connected to sample the synchro or resolver input in that channel.

The sample enable, SE, inhibits the sample time generator. If the SE is at logic 1, the sample time generator automatically produces an $\overline{ST}$ pulse near each positive peak of the reference waveform, as shown in the sample time pulse diagram. The synchro and resolver inputs connected to each reference are therefore sampled simultaneously once during each cycle, unless an SE pulse is applied. The $\overline{ST}$ pulse is inhibited only if the SE is at logic 0 at the moment the $\overline{ST}$ is initiated; once the $\overline{ST}$ begins, a subsequent SE drop to logic 0 will not affect the $\overline{ST}$ pulse completion.

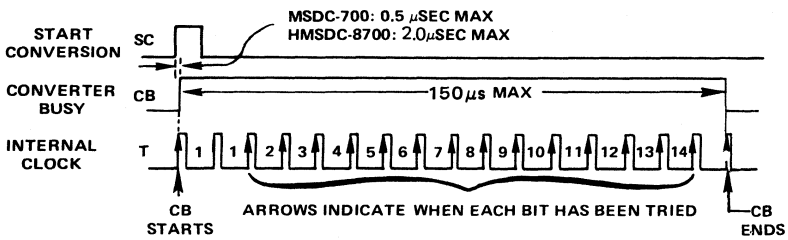
The outputs from each signal input circuit are nominally +4.1 sin θ sin ωt and –4.1 cos θ sin ωt. These signals are sampled by the dual sample/hold at a time close to the positive peaks of the reference waveform. The dual sample/hold outputs are nominally +4.1 sinθ and –4.1 cosθ. These outputs are muxed together to the central converter input. The MUX select lines $\overline{MA}$, $\overline{MB}$,...determine which of these outputs will be processed. The MUX shorting switches are operated automatically by the converter busy pulse to discharge the central converter muxed input lines between conversions.

The sin/cos select S/C was designed for situations in which the output from a signal module is processed not by a converter module, but by some other means such as a computer. By operating the S/C control, the sinθ and cosθ information can be muxed into one output line.

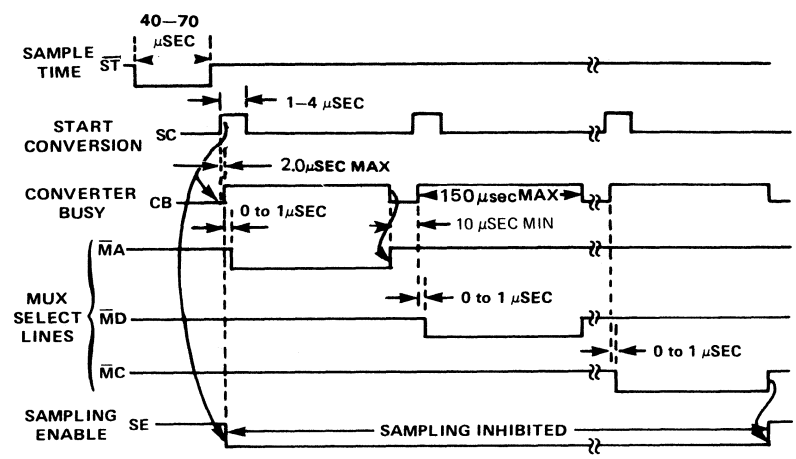
The –85° nominal phase shifter and the zero crossing detector in the reference channel detect the peak of the reference waveform. The 5° shift away from 90° compensates for a lead of approximately this amount which normally occurs between the signal output and reference input of a synchro or resolver.



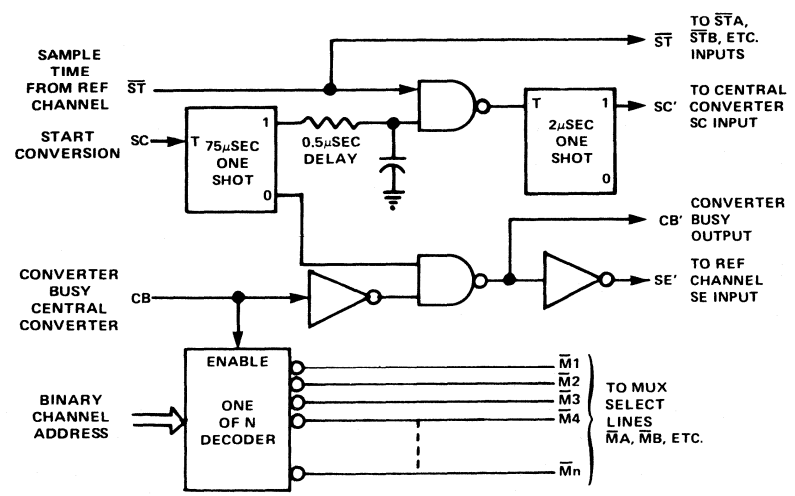
SAMPLE TIME ($\overline{ST}$) PULSE DIAGRAM



CENTRAL CONVERTER CLOCK TIMING



TIMING DIAGRAM



TIMING INTERLOCK CIRCUIT

SYSTEM TIMING

Timing and control for the MSDC-700 and the HMSDC-8700 are depicted in the timing diagram. An SC pulse for converting data from any channel can be initiated at any time. The basic timing sequence is as follows:

1. Start conversion with an SC pulse. The leading edge of the SC pulse will cause a converter busy (CB) pulse to be generated, and the MUX shorting switches will open automatically during the CB pulse interval. 10 μsec min must elapse between trailing edge of CB and the leading edge of channel select.
2. Select the channel to be converted by driving any of the MUX select lines $\overline{MA}$, $\overline{MB}$,... to logic 0 within 1 μsec of the CB leading edge.
3. Drive the MUX select line back to logic 1 after the CB returns to logic 0.

This sequence is repeated for each conversion, with a minimum time interval of 10 μsec between the end of one CB and the start of the next SC.

Errors of a few LSBs can occur if a signal input is sampled while it is being converted. The following methods can be used to prevent simultaneous sampling and conversion:

1. Conversions can be timed to occur only between $\overline{ST}$ pulses. This is accomplished by interlocking the SC and the $\overline{ST}$ pulse with logic circuitry.
2. New $\overline{ST}$ pulses can be inhibited during conversions by keeping the SE at logic 0 until all conversions have been completed, as shown in the timing diagram. However, it is still necessary to avoid starting a conversion while sampling is in progress.

The timing interlock circuit shown will prevent simultaneous sampling and conversion. An SC input pulse first produces an SE to inhibit $\overline{ST}$ pulses. Then after a 0.5 μsec delay the SC input produces a start conversion pulse SC' only if there is no $\overline{ST}$ in progress. The SE pulse will remain low during the conversion process because of the interlock with the central converter CB. The one-of-N decoder is used to gate the MUX channel addresses with the CB. An SE input may be combined with the SE' to inhibit sampling between conversions.

The maximum number of conversions per carrier cycle may be calculated as follows:

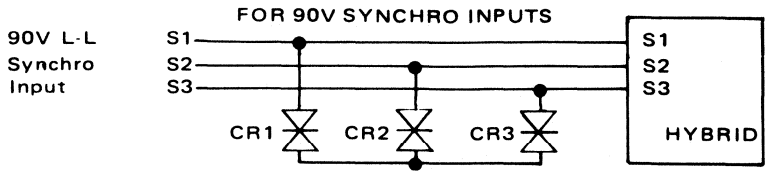
$$\text{Max no. of conversions/cycle} = \frac{\text{minimum period} - \text{max } \overline{ST} \text{ pulse time}}{\text{max CB pulse time} + 10\ \mu\text{sec}}$$

SOLID STATE BUFFER INPUT PROTECTION (HMSDC-8700 ONLY)

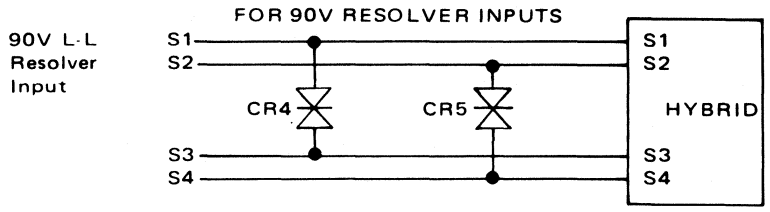
The solid state signal and reference inputs in the HMSDC-8700 input modules are true differential inputs with high AC and DC common mode rejection. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage range should not exceed the following values:.

INPUT	COMMON MODE MAXIMUM	MAX TRANSIENT PEAK VOLTAGE
11.8V L-L	25V Peak	150V
26V L-L	50V Peak	150V
90V L-L	150V Peak	350V
Reference	210V Peak	1000V

90V line-to-line systems generally have voltage transients which exceed the 350V specification listed above. These transients can destroy the thin film input resistor network in the hybrid. Therefore, 90V L-L solid state input modules should always be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro or resolver voltages are switched on or off.



CR1, CR2 and CR3 are 1N6130, 100V bi-polarity transient voltage suppressors or equivalent.

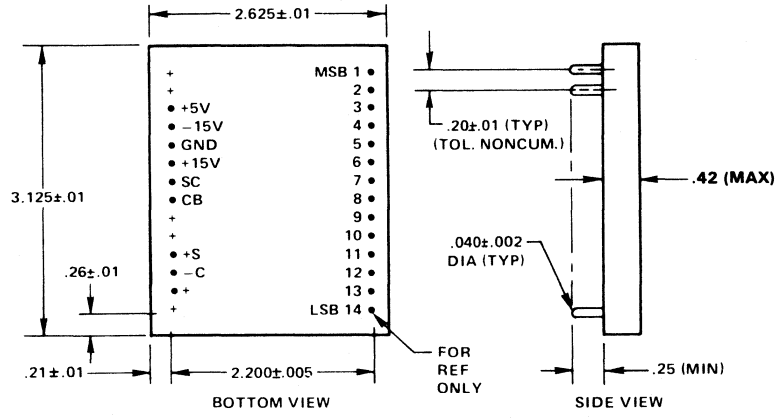


CR 4 and CR5 are 1N6137, 200V bi-polarity transient voltage suppressors or equivalent.

CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

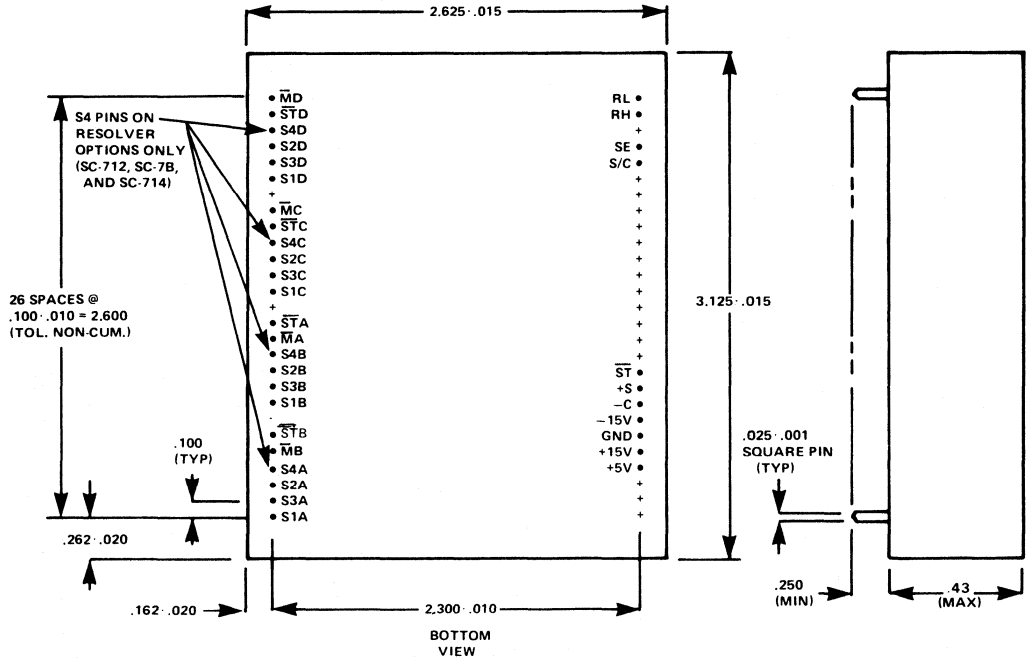
MECHANICAL OUTLINES FOR DISCRETE MODULES

1. CENTRAL CONVERTER: SC-700



Notes:
1. Pin material is electrosoldered brass per MIL-F-14072, M222.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14.

2. SIGNAL INPUT MODULES: SC-710 TO SC-715



Notes:
1. Case in glass filled Diallyl Phthalate per MIL-M-14
2. Pin material is 3/4 hard phosphor bronze per ASTM Type 1 B159-606
3. Pin plating is .00015 min acid tin per MIL-T-10727A

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All HMSDC-8700's are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5004/5008 except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) is 530,000 hours, at 25°C, for a 4 channel system consisting of one hybrid central converter module and one hybrid signal input module.

PIN CONNECTION TABLES FOR HYBRID MODULES

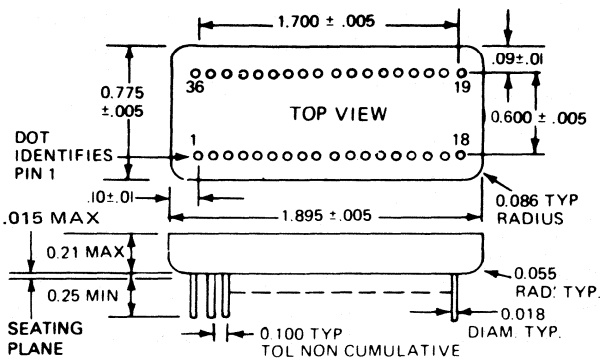
1. PIN CONNECTION TABLE FOR CENTRAL CONVERTER: SC-8700

Pin	Name	Description	Pin	Name	Description
1	B1	14 Bit Outputs	20	-C	-COS input. Connect to -C outputs on all input modules.
2	B2				
3	B3				
4	B4		21	+S	+SIN input. Connect to +S outputs on all input modules.
5	B5				
6	B6				
7	B7		22	CB	Converter busy output
8	B8		23	SC	Start conversion input
9	B9		24	TP4	(+5.6) Factory test point
10	B10		25	TP6	(e) Factory test point
11	B11		26	NC	No connection
12	B12		27	+	No connection if unused
13	B13		28	NC	No connection
14	B14		29	TP8	Factory test point
15	NC	No connection	30	TP9	(T) Factory test point
16	TP1	(+BC) Factory test points	31	+5V	Power supply connections
17	TP3	(-BS) Factory test points	32	-15V	Power supply connections
18	TP2	(-BC) Factory test points	33	TP7	(E) Factory test point
19	AG	Analog GND (Must be connected to pin 34)	34	GND	Power supply and logic GND
			35	TP5	(-8.2) Factory test point
			36	+15V	Power supply connection

2. PIN CONNECTION TABLE FOR INPUT MODULES: SC-8710 TO SC-8714

Pin	Name	Description	Pin	Name	Description
1	S1A	Synchro or resolver input A. S4 for Resolver only.	21	NC	No connection
2	S3A		22	+5V	Power supply connections
3	S4A		23	-15V	
4	S2A		24	GND	
5	S1B	Synchro or resolver input B. S4 for resolver only.	25	+15V	
6	S3B		26	$\overline{STD}$	Sample time inputs and MUX select lines for inputs A, B, C, and D. Connect sample time inputs to any appropriate ST output.
7	S4B		27	$\overline{MD}$	
8	S2B		28	$\overline{STC}$	
9	S1C	Synchro or resolver input C. S4 for resolver only.	29	$\overline{MC}$	
10	S3C		30	$\overline{MB}$	
11	S4C		31	$\overline{STB}$	
12	S2C		32	$\overline{STA}$	
13	S1D	Synchro or resolver input D. S4 for resolver only.	33	$\overline{MA}$	
14	S3D		34	+S	+SIN output. Connect to +S input on central converter module.
15	S4D				
16	S2D				
17	RH	Ref input high	35	-C	-COS output. Connect to -C input on central converter module.
18	RL	Ref input low			
19	SE	Sample enable input. No connection if unused.	36	S/C	SIN/COS select input. No connection if unused.
20	$\overline{ST}$	Sample time output. Connect to sample time inputs on any module.			

MECHANICAL DIAGRAM FOR ALL HYBRID MODULES (SC 8700, SC 8710 – SC 8714)



PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING
PINS ARE KOVAR WITH GOLD PLATING (50 μINCH MIN)
CASE IS ELECTRICALLY FLOATING

ORDERING INFORMATION

Each module required is specified separately. Modules are called out with temperature range as follows:

SC 8710 – 1 – 883B

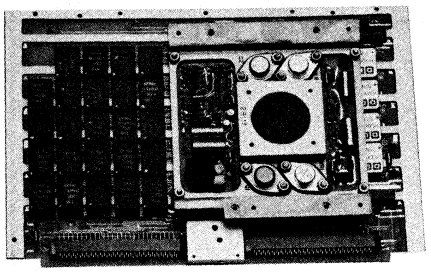
- 883B: MIL-STD-883 Processing: (Applies to hybrid modules only):
  - 883B = Conforms to MIL-STD-883B, DDC procedures.
  - Blank = Same, except pre burn in test and burn in are omitted
- 1: Temperature Range (Operating):
  - 1 = –55°C to +105 C
  - 3 = 0°C to +70°C
- SC 8710: Module Number:
  - 700 Series = Discrete encapsulated modules
  - 8700 Series = Hybrid modules

Each system requires the following:

1. Central Converter. Order one of the following:
   Discrete: SC 700.
   Hybrid: SC-8700
2. Signal Input Module. Order one or more of the following:

Input Type	L-L Voltage	Discrete Module No.	Discrete Frequency	Hybrid Module No.	Hybrid Frequency
Synchro	11.8V	SC 710	360-440 Hz	SC 8710	47-440 Hz
Synchro	90V	SC 711	360-440 Hz	SC 8711	47-440 Hz
Synchro	90V	SC-715*	47-440 Hz	–	–
Resolver	11.8V	SC 712	360-440 Hz	SC 8712	47-440 Hz
Resolver	26V	SC 713	360-440 Hz	SC 8713	47-440 Hz
Resolver	90V	SC 714	360-440 Hz	SC 8714	47-440 Hz

*The SC-715 module may be used at 400 Hz by interconnecting the SC-711 sample time outputs ($\overline{ST}$) to the desired SC-715 sample time inputs ($\overline{STA}$, $\overline{STB}$, $\overline{STC}$ and $\overline{STD}$).



ROLM 1602B PROCESSOR (AN/UYK-19) COMPATIBLE, 8 CHANNEL, S/D CONVERTER MODULE

DESCRIPTION

The DDC-6509 S/D Converter module is designed to interface with a Rolm 1602B Processor and provide 8 channels of synchro-to-digital conversion. It is mechanically configured to mount in two adjacent PC card slots of a Rolm 2150 I/O expander chassis. Functionally, the DDC-6509 provides all required hardware, device and channel-select logic and user programmable address-select capability to process instruction commands generated by the Rolm Processor. All synchro signal and reference inputs are independently transformer isolated. All connections are made with in-line-plug assemblies mounted to the internal circuit board.

Signal and reference inputs are respectively 90V rms (L-L) and 115V rms (L-L), 400 Hz. The DDC-6509 is capable of tracking up to a maximum of 3600°/second with accuracy of ±5.3 arc minutes on each of its eight input channels.

Because the module houses a DC to DC converter for internal power, the only power required from the Rolm chassis is +5 volts at 3 amps.

Output data is 14-bit negative-true TTL, presented in left-justified format on the 16-line Rolm I/O data bus. The module is interrogated by the Rolm processor, via programmed Data Input (DATIA) and Data Output (DATOA) instruction control signals.

The eight channels of S/D conversion are performed by DDC model HSDC-8915 Monobrid® tracking converters. The HSDC-8915 is a 14-bit hybrid S/D converter with 3-state outputs.

APPLICATIONS

The DDC-6509 is used when multiple synchro position information must be interfaced with a Rolm 1602B Processor. Specific applications include ordnance aiming controls, navigation systems and range instrumentation.

FEATURES

- *ROLM 1602B PROCESSOR COMPATIBLE*
- *FITS INTO TWO STANDARD CARD SLOTS OF ROLM EXPANDER CHASSIS*
- *+5V SUPPLY ONLY*
- *8 CHANNELS OF 14 BIT S/D CONVERSION*
- *±5.3 MINUTES ACCURACY*
- *TRANSFORMER ISOLATED*

Monobrid® is a registered trademark of ILC Data Device Corporation.

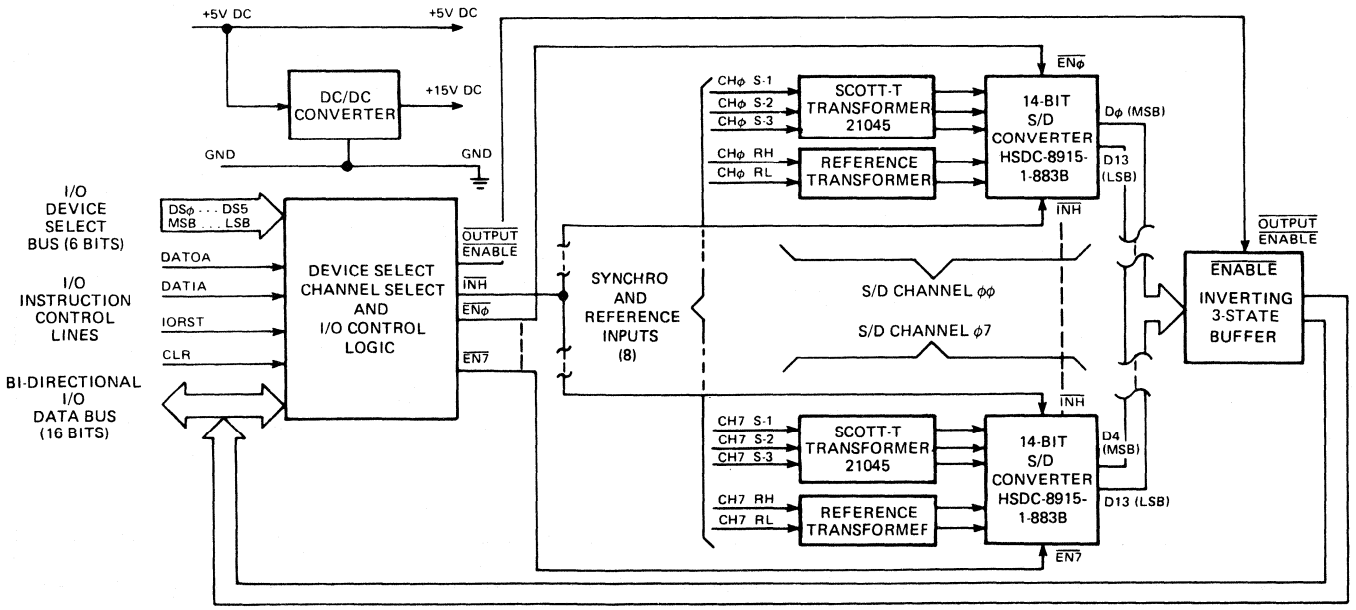


FIGURE 1. BLOCK DIAGRAM

SECTION F

DIGITAL TO SYNCHRO AND RESOLVER CONVERTERS

PRODUCT SUMMARY TABLE

Name	Form Factor	Features	Page
DRC-10500	32 pin TDIP hybrid	14 bit high power (1.5VA) hybrid D/R converter. 8 bit byte input latches are standard. Optional BITE capability available.	208
DSC-544	Encap. Module 3.1 x 2.6 x 0.8"	14 bit D/S converter that dissipates half the power of previous designs. Parallel CMOS and TTL digital input compatible and output is transformer isolated 90V synchro @ 400 Hz and 60 Hz. Requires only +5V power supply.	212
DSC-644	Encap. Module 3.1 x 2.6 x 0.5"	14 bit D/S and D/R, with fully protected output, very low scale factor variation of 0.05% typical and parallel CMOS or TTL digital input. Conservative thermal design includes metal heatsink at top of its low profile case.	216
EDSC	Encap. Module 3.1 x 2.6 x 0.8"	14 bit D/S or D/R Converter with ±4 minute accuracy. Synchro or resolver type output capable of driving many typical control transformers.	222
HDSC-14	36 pin DDIP hybrid	14 bit D/S or D/R Converter with ±4 minute accuracy. Pin programmable low level resolver or synchro output at 2 mA.	225
MDRC	Encap. Module 3.1 x 2.6 x 0.4"	14 bit D/R converter in a low profile module. Scale factor typically is 0.05%. The input is compatible with CMOS and TTL inputs.	228
TD-100/ 101	P.C. card mounted with buffer on card or on remote heat sink	12 bit D/S Converter with an accuracy of ±10 minutes for control transformer loads and ±21 minutes for torque receiver loads. A heavy duty extrenally mounted heat sink unit can drive the heaviest synchro loads.	232

BACKGROUND INFORMATION

INTRODUCTION

DDC's Digital-to-Synchro and Digital-to-Resolver converters are intended to satisfy a broad category of interface applications where digital angle data with binary bit weights must be converted accurately to either three-wire synchro or four-wire resolver signals.

From a systems engineer's standpoint, outstanding performance features have been incorporated into these units. They are designed for printed circuit board mounting by hand soldering and flow soldering techniques. Each unit is fully trimmed and tested before leaving the factory. DDC builds hundreds of converters each month, making shipments from stock a common occurence.

THEORY OF OPERATION

The input to a Digital-to-Synchro (D/S) or Digital-to-Resolver (D/R) converter is a set of binary weighted "logic levels", (ones & zeros), representing the shaft angle, θ, to some number of bits of resolution (Figure 1). The first two most significant bits (MSBs) of any pure binary coded word are the quadrant designating bits (the first three, by similar reasoning, are the octant designating bits). The remaining bits of the digital word determine the angle precisely by adding some value between 0 degrees and 90 degrees. Converting these bits into analog levels corresponding to the sin and cos of that angle (between 0 degrees and 90 degrees) will enable us to use the quadrant-designating bits to establish the appropriate polarity for these analog levels, in accordance with the following identities:

$$\text{Sin } \theta \text{ (2nd quad.)} = + \cos(\theta - 90^\circ)$$
$$\text{Sin } \theta \text{ (3rd quad.)} = - \sin(\theta - 180^\circ)$$
$$\text{Sin } \theta \text{ (4th quad.)} = - \cos(\theta - 270^\circ)$$
$$\text{Cos } \theta \text{ (2nd quad.)} = - \sin(\theta - 90^\circ)$$
$$\text{Cos } \theta \text{ (3rd quad.)} = - \cos(\theta - 180^\circ)$$
$$\text{Cos } \theta \text{ (4th quad.)} = + \sin(\theta - 270^\circ)$$

Quadrant	1st 2 MSBs	Polarity Sin θ	Polarity Cos θ
4	11	Neg	Pos
3	10	Neg	Neg
2	01	Pos	Neg
1	00	Pos	Pos

By routing the first two MSBs to a set of polarity/signal selection logic circuits, we may reduce our problem to trigonometric D/A conversion in only one quadrant (see Figure 1). The first two MSBs are diverted to a quadrant selector circuit and the remaining bits are used to program 0 degrees to 90 degrees sin and cos function generators. These generators may be described as non-linear, bipolar, multiplying D/A converters in which the reference input signal is the reference (E ref), and the transfer function is either EA = E ref Sin θ or EB = E ref cos θ, where θ is the angle represented by the digital input.

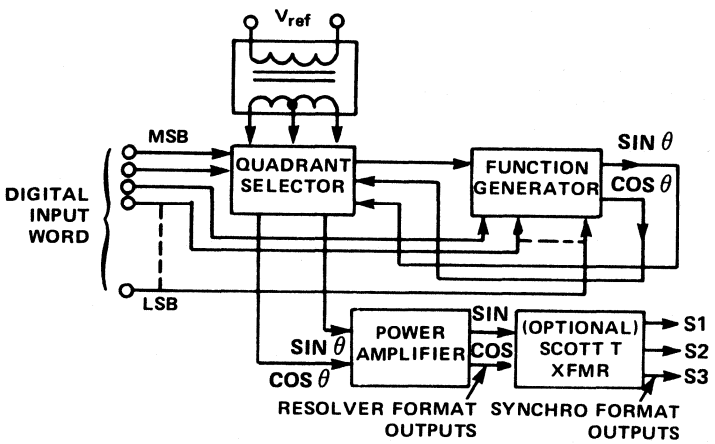


FIGURE 1 BASIC DIGITAL-TO-SYNCHRO RESOLVER CONVERTER

The reference voltage supplied to the D/S converter is transformer or resistor isolated and converted (with the use of a centertap) into two equal reference frequency sin waves of opposite phase. After quadrant selection, they are fed to the inputs of the function generators. The outputs of the function generators are now accurate resolver-format signals. For resolver to synchro conversion, the use of a "reversed" Scott-T transformer is required in order to convert from 4-wire resolver to 3-wire synchro. The outputs produced by these converters are low-energy, low-voltage signals and may require the use of an external high power buffer amplifier (DDC's HPB or SBA series of amplifiers).

The conventions for output phasing and for RH, RL for each of DDC's synchro or resolver to digital converters and torque receivers are described individually for each product. If the output of an S/D or R/D converter is used to provide input for a D/S or D/R converter, the relative phasing of RH, RL on both units should be compared.

APPLICATIONS

In all of DDC's D/S or D/R converters, careful attention must be given to making the proper electrical connections. Reversal or misapplication of power supplies can result in damage to the converter. When preparing the P.C. artwork, keep all AC signals apart from both the digital and power leads. This will make it less likely that meter or scope probes will induce potentially destructive shorts.

Care must be taken when handling units which have CMOS inputs since they are extremely sensitive to static. Avoid handling the units by their leads, keeping them plugged into the conductive foam supplied with the unit until they are ready for use in a circuit.

The synchro or resolver system reference must be connected to the REF HI and REF LO terminals. It is very important that extreme caution be used in handling the reference since sometimes it is a high AC voltage, usually from a low source impedance. If it makes contact with either a digital input or a power terminal, damage will result. The output AC signals are derived from (and proportional to) the applied reference. Any distortion present on the reference will appear in the output signals. The input power to the reference terminals is a negligible load for almost any reference source. The typical load for a D/S is a CT (control transformer) which is a highly inductive load with a reasonable Q. It is possible to "tune" this load by placing three capacitors of the proper value across the synchro output in a delta configuration (Figure 2). The same holds true for the resolver output, except that only two capacitors are

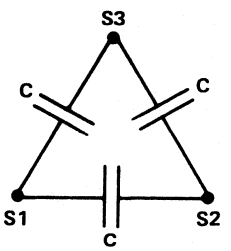


FIGURE 2 DELTA CONFIGURATION FOR TUNING LOADS

required. The formula for determining the size of the capacitor is given in Figure 3. Note that good grade capacitors are necessary and that they must be able to withstand the full AC output voltage. By tuning the load, you can raise the effective impedance and thereby drive many more loads simultaneously.

Do not exceed the converter's output load ratings since it will cause waveform distortion leading to inaccuracies. A false null may occur 180 degrees away from the true null due to the fact that the converter can alter the angle so fast that the servo (load) cannot respond. To avoid this problem, the software which determines how the digital data is generated should never allow 180 degrees changes to take place in one step.

Transients may occur when the data angle changes. This usually does not cause any error since the low bandwidth of the synchro filters out these transients. If your application includes a high speed S/D, be sure that you give the D/S enough time to settle before reading the output angle. To test these converters you will need the equipment shown in Figure 4. We suggest that DDC's new synchro angle indicator (the SR-103) be used to test the D/S. As an alternative, use the bit switches to program any angle, and adjust the synchro bridge for a null as read by the phase angle voltmeter. The error is equal to the angle read by the bridge subtracted from the theoretical angle. If it would seem beneficial to avoid the high cost of test equipment, we invite you to use DDC's facilities for "source inspection" at no extra charge.

$$C = \frac{X'_{LSO}}{6\pi f\,[(R'_{so})^2 + (X'_{LSO})^2]}$$

Where:

C = Tuning capacitor in farads in delta connection.

X'_{LSO} = Reactive component of impedance of one stator winding leg with rotor open circuit.

f = Frequency in Hz

R'_{so} = Resistive component of impedance of one stator winding leg with rotor open circuit.

Note:

$$Z'_{so} = \frac{2}{3}(Z_{so})$$

Z_{so} = Stator winding impedance with rotor open circuit.

Z'_{so} = per leg winding impedance with rotor open circuit.

FIGURE 3 CAPACITOR FOR TUNING SYNCHRO STATOR WINDINGS

SOME COMMON CONTROL TRANSFORMERS AND THEIR LOAD IMPEDANCES

Military Type Number	Size	Z_{so}	Use DDC Converter Number	Comments
26 V 08CT4c	08	100+j490	EDSC-L	
26 V 11CT4d	11	21+j132	EDSC-L	
11CT4e	11	838+j4955	EDSC-H	
15CT4c	15	1600+j9300	EDSC-H	
15CT6b	15	1170+j6780	EDSC-6	60 Hz
18CT4c	18	1420+j3260	EDSC-H	
18CT6b	18	1680+j5040	EDSC-6	60 Hz
23CT4a	23	1460+j11050	EDSC-H	
23CT6a	23	1250+j3980	EDSC-6	60 Hz

Please obtain complete data from the synchro manufacturer or other sources to determine the impedances. There are many variations in synchros and you should not assume that a 15 CT 4 and a 15 CT 4d are the same. They are not.

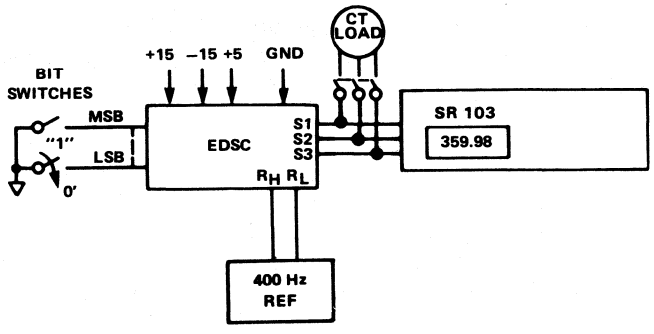
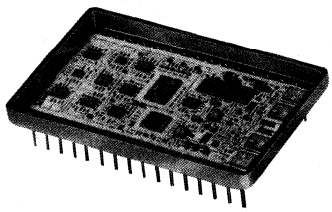


FIGURE 4 EDSC TEST CONFIGURATION

HIGH POWER 14 BIT HYBRID D/R CONVERTER



DESCRIPTION

The DRC-10500 is a 14 bit, 32 pin triple DIP D/R Converter with 1.5 VA drive capability. Featuring a power amplifier that may be driven by a standard ±15V DC power supply, or by the reference source when used with the optional power transformer DDC/PN 29306, the DRC-10500 provides compatibility with microprocessors through its 8 bit 2 byte transparent input latch. Data input is natural binary angle in CMOS parallel positive logic format. The DRC-10500 is comprised of a high accuracy D/R converter and a dual power amplifier stage and has high accuracy and low scale factor variation. An optional BITE circuit provides a digital over-current signal output. A logic "0" pulse once per carrier cycle is used for detection of overcurrent condition in the sine or cosine outputs. Reference inputs are scalable with external resistors. Loss of power or reference signal will not damage the converter.

APPLICATION

The DRC-10500 can be used where digitized shaft angle data must be converted to an analog format for driving control transformers. With its built-in input latches, the DRC-10500 is especially compatible with a microprocessor based system including flight simulators, flight instrumentation, fire control systems, radar and navigation systems, and air data computers.

FEATURES

- *HYBRID CONSTRUCTION*
- *1.5 VA DRIVE CAPABILITY*
- *8 BIT/2 BYTE TRANSPARENT INPUT LATCH*
- *RESOLUTION: 14 BITS ACCURACY: ±4 MINUTES*
- *POWER AMPLIFIER USES AC REFERENCE OR DC SUPPLIES*
- *OPTIONAL BITE CIRCUIT*

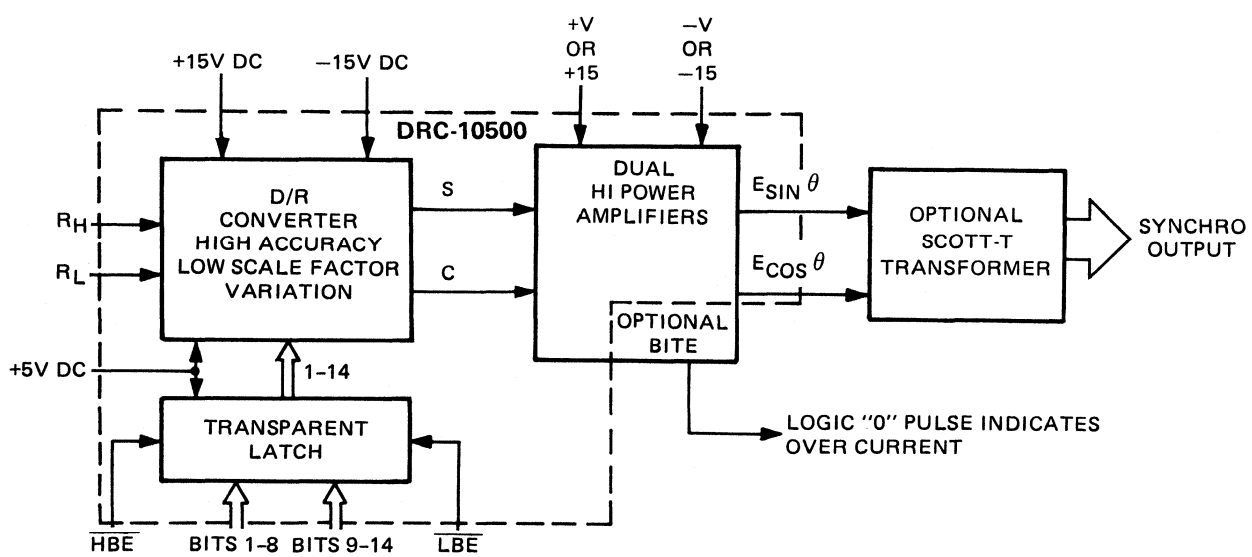


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Apply over temperature range, power supply ranges, reference voltage and frequency range and 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY AND DYNAMICS	
Output Accuracy	
Without Scott-T	±4 minutes
With Scott-T P/N29305	±10 minutes(1.5 VA min for CT load) ±16 minutes (2VA min for CT load)
Differential Linearity	±1 LSB
Output Settling Time	Less than 40 μsec for any digital input step change
DIGITAL INPUT	
Logic Type	Natural binary angle, parallel positive logic, CMOS. V_{DD} = 5 VDC Buffered by transparent latches Logic "0" = 1.5V max Logic "1" = 3.5V min
$\overline{HBE}$	Controls bits 1-8 (8 MSBs) ("0" = latch
$\overline{LBE}$	Controls bits 9-14 (6 LSBs) "1" = transparent
Loading	1 CMOS (10 μA max)
REFERENCE INPUT	
Type	Differential 3.4V rms
Voltage	Higher voltages are scaled by adding series resistors
Frequency	DC 1 kHz
Input Impedance	
Single Ended	13 kΩ ±0.5%
Differential	26 kΩ ±0.5%

PARAMETER	VALUE
ANALOG OUTPUT	
Type	Resolver
Output Current	220 mA rms, min (1.5VA, min)
Max Output Voltage /tracks reference input voltage)	6.8V rms max line-to-line ±1% Simultaneous amplitude variation in all output lines as function of digital angle is ±0.2% max.
Scale Factor Variation	
DC Offset (each line to ground)	±30 mV max varies with input angle.
Protection	Output is protected from over current, short circuits and voltage feedback transients.
POWER SUPPLIES	
Voltage	+15V | −15V | +5V | +V | −V
Voltage Limits	±5% | ±5% | ±10% | 20V peak max 3V above output voltage min.
Max Voltage Without Damage	+18V | −18V | +7V | +25V | −25V
Current	30mA max | 30mA max | 2mA max | load dependent
Peak Current At Power Turn On or Short Circuit (when using Transformer)	700 mA max
TEMPERATURE RANGES	
Operating (−3xx)	0°C to +70°C case
(−1xx)	−55°C to +125°C case
Storage	−55°C to +135°C
PHYSICAL CHARACTERISTICS	
Package Type	32 pin triple DIP
Size	1.14 x 1.74 x 0.28 inch (28 x 44 x 7.0mm)
Weight	1.15 oz (33g)

TECHNICAL INFORMATION

INTRODUCTION

The DRC-10500 is a digital to resolver (D/R) converter which has an inherently high accuracy and low scale factor variation. The circuit is based on an algorithm whose theoretical math error is only ±3.5 arc-seconds (less than 5% of 1 LSB), and whose theoretical scale factor variation with angle is less than ±0.015%. Therefore accuracy and scale factor are limited only by the physical components, not by the algorithm.

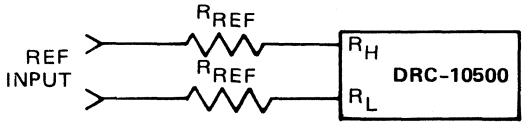
The digital inputs are CMOS transparent latches (Figure 1). Bit weights for the 14 binary inputs are given in the bit weight table. Angle is determined by adding bits in the logic 1 state.

REFERENCE LEVEL ADJUSTMENT

The input is specified for operation at a reference level of 3.4V rms, however reference levels other than 3.4V rms may be scaled by calculating the value of the scaling resistor with the following equation:

$$R_{REF} = \frac{(V_{REF} - 3.4)}{3.4} \times 13k$$

eg., if V_{REF} = 26V rms, then $R_{REF} = \frac{(26-3.4)}{3.4} \times 13k = 86.4\ k\Omega$



The output is a 6.8V rms line-to-line resolver format signal which may be converted into a synchro format of 11.8V line-to-line with the companion Scott-T transformer module available as DDC P/N29305.

DRIVING THE POWER AMPLIFIER WITH THE REFERENCE

The high power amplifier stage can be driven by a standard ±15V DC supply or with a high efficiency pulsating power supply derived from the reference voltage source. A companion power transformer DDC P/N29306, designed to implement the pulsating power source for the DRC-10500 is also available (Figure 2). The DRC-10500 will not be damaged by sequencing order or interruptions in either the ±15V, +5V supplies or the reference input.

OUTPUT PROTECTION

The output is protected from over current, short circuits and voltage feedback transients. The optional BITE circuit available with the DRC-10501 detects over current conditions in the sine or cosine resolver output. A logic "0" pulse, once per carrier cycle is used for over current detection. Normal operation is logic "1". Pull-up to logic "1" is 10k ohms.

BITE OPERATION

The BITE line is normally at logic "1". An overload resulting from in-phase load current will cause the BITE line to drop when the output current exceeds a peak level of approximately 300 ma. This will occur once per carrier cycle when both sine and cosine are of the same relationship. When they are of opposite phase, BITE output will occur twice per carrier cycle.

A phase-shifted load current will produce identical results but the pulses will be time-phase shifted accordingly.

A short circuit condition will cause the BITE line to go low immediately and to remain low for either one-half or a full carrier cycle, depending on the instantaneous relation polarities of the sine/cosine signals.

Since the BITE output is a pulsating event rather than a continuous level during an overload condition the use of an external one-shot with suitable time constant is advised if continuous level flag is required.

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing:

$$\sin = (R_H - R_L)\, A_O\, (1 + A(\theta))\, \sin\theta$$
$$\cos = (R_H - R_L)\, A_O\, (1 + A(\theta))\, \cos\theta$$

The output amplifiers simultaneously track reference voltage fluctuations because they are proportional to (RH-RL). The amplitude factor A_O is 2 for 6.8V rms L-L output. The maximum variation in A_O from all causes is 0.8%. The term $A(\theta)$ represents the variation of the amplitude with the digital input angle. $A(\theta)$, which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.2% for all values of θ. The total maximum variation in $A_O\,(1 + A(\theta))$ is therefore ±1%.

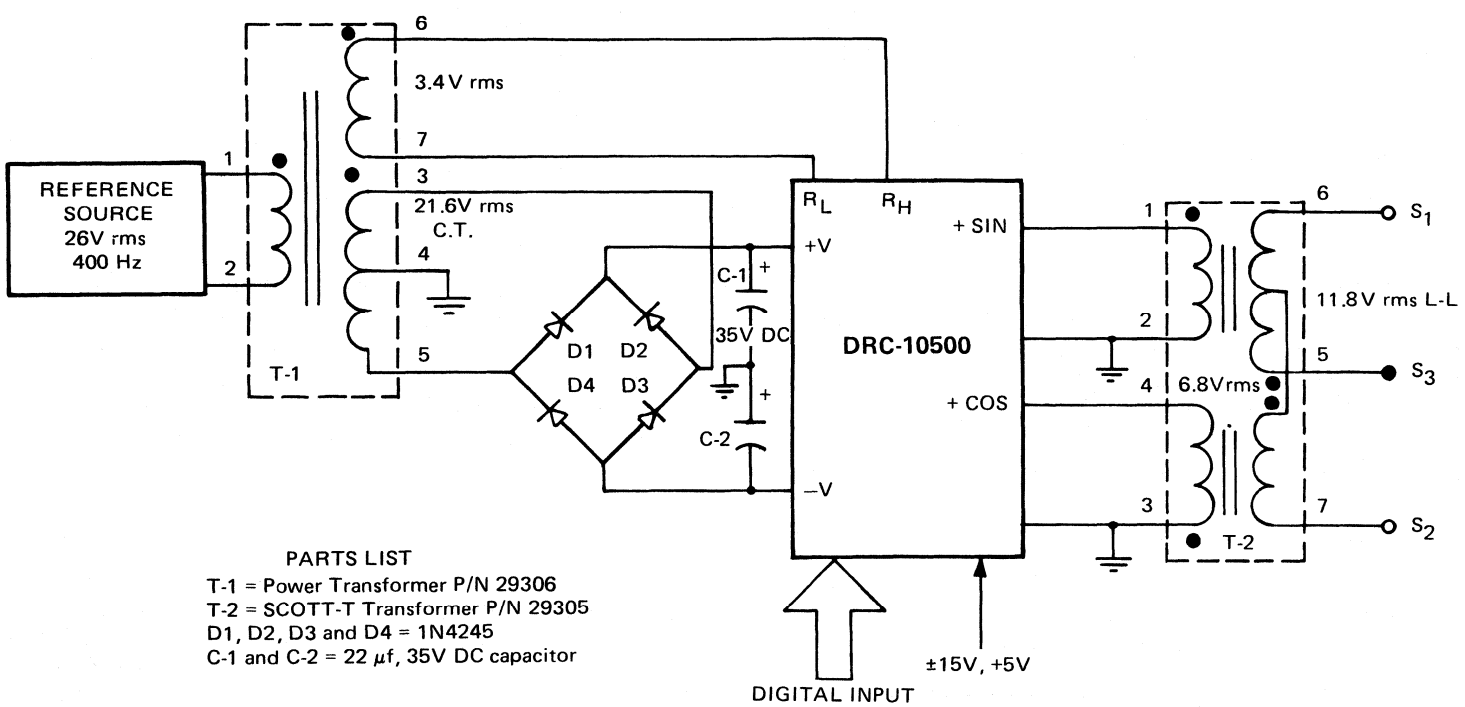
Because the amplitude factor $(R_H - R_L)\, A_O\, (1 + A(\theta))$ varies simultaneously on all output lines, it will not be a source of error when the DRC-10500 is to drive a ratiometric system such as a resolver or synchro. However, if the outputs are used independently, as in x-y plotters, the amplitude variations must be taken into account.

RELIABILITY

The use of MSI circuits and thin film resistor networks, as well as careful thermal design, results in high MTBF values. Summaries of MTBF calculations are available on request. All DDC hybrids are built in accordance with the requirements of MIL-STD-883. The screening is based on the requirements of Method 5008, except for burn-in which is optional.

PIN CONNECTION TABLE

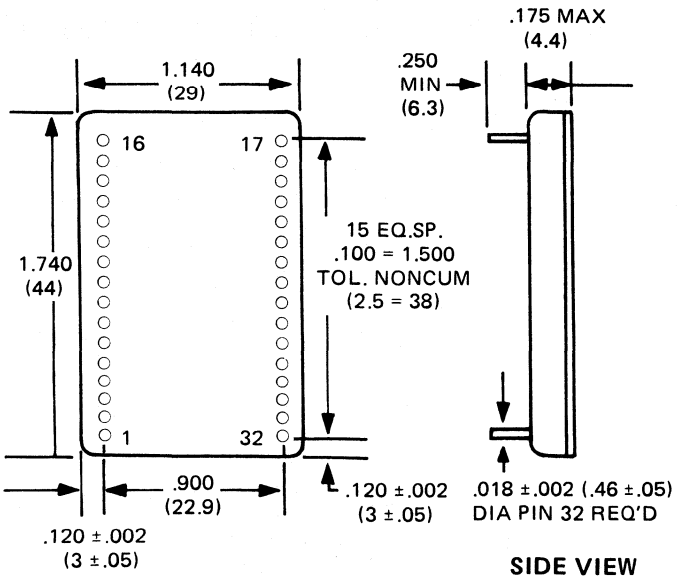
PIN	FUNCTION	PIN	FUNCTION
1	NC	17	$\overline{LBE}$
2	NC	18	9
3	NC	19	10
4	COS	20	11
5	SIN	21	12
6	+V	22	13
7	–V	23	14
8	1	24	R_L
9	2	25	R_H
10	3	26	+5V
11	4	27	–15V
12	5	28	GND
13	6	29	NC
14	7	30	+15V
15	8	31	BITE OUT (Optional)
16	$\overline{HBE}$	32	NC



PARTS LIST
T-1 = Power Transformer P/N 29306
T-2 = SCOTT-T Transformer P/N 29305
D1, D2, D3 and D4 = 1N4245
C-1 and C-2 = 22 μf, 35V DC capacitor

FIGURE 2. TYPICAL CONNECTION DIAGRAM UTILIZING PULSATING POWER SOURCE FOR SYNCHRO OUTPUT.

MECHANICAL OUTLINE
32 Pin Triple DIP



NOTES:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be cnetered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-883, Method 2003.

ORDERING INFORMATION
CONVERTER:

DRC-1050 X-X X 3

- Accuracy:
  - 3 = ±4 minutes
- Reliability Grade:
  - 0 = Standard
  - 1 = 883
- Operating Temperature Range:
  - 1 = –55°C to +125°C (case)
  - 3 = 0°C to +70°C (case)
- BITE Option:
  - 0 = No BITE
  - 1 = With BITE
- Family Code

TRANSFORMER:

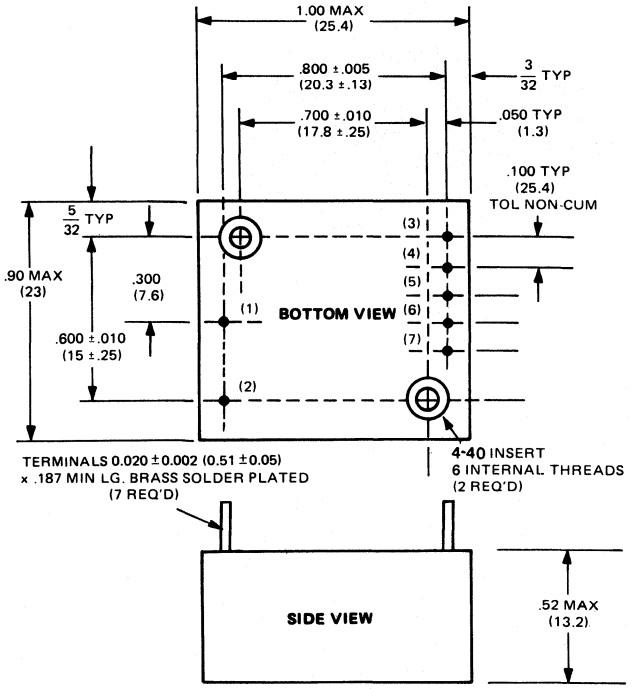
29305 Scott-T Transformer for 11.8V synchro output.

29306 Power Transformer used for driving amplifier stage with reference source.

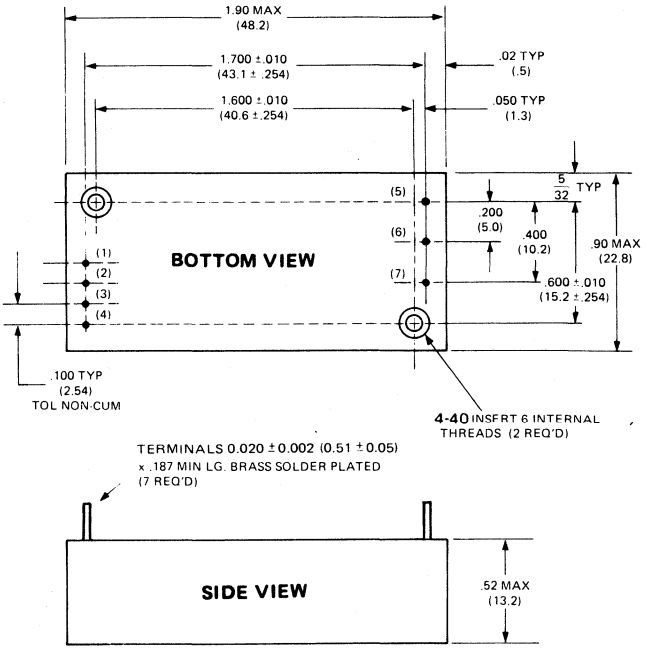
NOTE: The transformers listed above are representative of many available models. For alternative size and line to line levels contact the factory.

MECHANICAL OUTLINE
POWER TRANSFORMER (29306)

Dimensions in inches (millimeters)

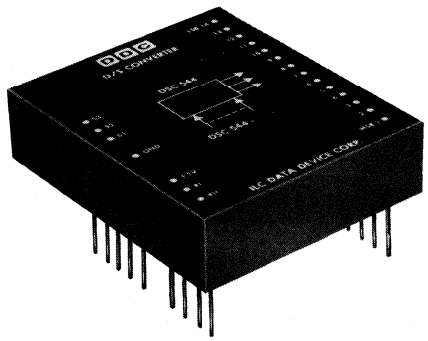


MECHANICAL OUTLINE
OUTPUT SCOTT-T TRANSFORMER(29305)



DDC
ILC DATA DEVICE CORPORATION

14 BIT D/S CONVERTER
4.5VA; Powered From Ref Input



FEATURES

- *POWER DISSIPATION CUT IN HALF:*
  AT 400 Hz, DRIVING 4.5 VA, DISSIPATES 6W
  AT 60 Hz, DRIVING 1.5 VA, DISSIPATES 3W
- *DOES NOT REQUIRE +15V OR −15V SUPPLIES*
- *NO EXTERNAL TRANSFORMER AT 60 Hz*
- *VIRTUALLY INDESTRUCTABLE:*
  RUGGED POWER AMPLIFIERS WITH CURRENT LIMITING
  COMPLETELY SHORT-CIRCUIT PROOF
  OVERVOLTAGE TRANSIENT PROTECTION
  THERMAL CUTOFF
- *OUTPUT*
  TRANSFORMER ISOLATED OUTPUT
  90V SYNCHRO OUTPUT AT 400 Hz AND 60 Hz
- *DIGITAL INPUT*
  CMOS AND TTL COMPATIBLE
  PARALLEL BINARY ANGLE INPUT
- *POWER SUPPLIES REQUIRED:*
  +5 V ONLY

DESCRIPTION

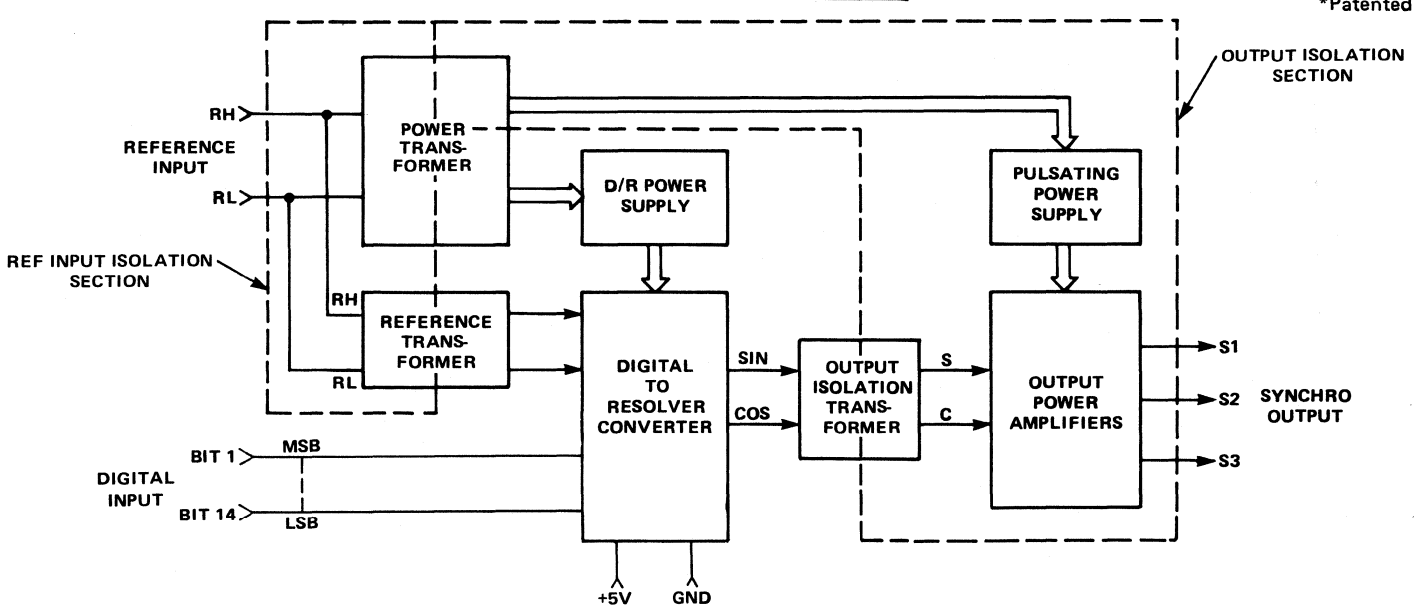
The DSC-544 digital to synchro (D/S) converter complements the low profile DSC-644 industry standard by providing additional features. The DSC-544 has a 0.82" high profile and standard pinouts except that the need for +15V and -15V power supplies has been eliminated. Because the unit is powered from the reference input with an internal pulsating power supply it is much more efficient. The reduced heat dissipation has made it possible to increase the load at 400 Hz by a factor of three, and the power output at 60 Hz is limited only by the size of the internal power transformer.

The DSC-544 also retains the many improved features of the DSC-644. The output is fully protected against overloads, transients from load kickbacks, short circuits and overheating. An aluminum top plate in the module improves thermal dissipation. And a new circuit design provides a smoother, more accurate output with improved transient response and a negligible scale factor variation.

APPLICATIONS

The DSC-544 may be preferred when its special features are required: elimination of the ±15V power supplies, elimination of an external transformer at 60 Hz, greater drive capability at 400 Hz, and less heat dissipation. The converter is used in many applications where digitized shaft angle data must be converted to synchro form to drive control transformers, control differential transmitters, and angle indicators. Because these converters are very rugged, and meet the requirements of MIL-STD-202, they are suitable for the most severe industrial and military applications, including military ground support and avionics. They are used especially in computer based systems in which digital information is processed, such as simulators, flight trainers, flight instrumentation, and fire control systems.

*Patented



DSC-544 BLOCK DIAGRAM

DSC-544 SPECIFICATIONS

Apply over operating temperature and frequency ranges, ±5% variation of power supply, ±10% reference amplitude variation, up to 10% reference harmonic distortion, and for any load up to full load.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY (TO FULL LOAD)	
Output Accuracy	±4 minutes
Differential Linearity	±1 LSB max
ANALOG OUTPUT (TRANSFORMER ISOLATED)	
Drive Capability (L-L Balanced)	
Synchro Output	
90V rms L-L, 360 – 440 Hz (Option H)	1.33 KΩ min
90V rms L-L, 57 – 63 Hz (Option I)	4.0 KΩ min
Output Scale Factor	
Absolute (All Causes)	±2%max simultaneous amplitude variation on all output lines, including variation with digital angle. Output amplitude tracks reference input amplitude.
Variation With Digital Angle	±0.1% max
Output Quadrature	±0.2% max
DIGITAL INPUT	
Logic Type	Natural binary angle; parallel positive logic TTL compatible Transient protected CMOS 33 KΩ pull-up to +5V
Loading	0.13 Std. TTL load

*The output amplifiers will drive loads with any phase angle from –90° to +90°.

PARAMETER	VALUE
REFERENCE INPUT (TRANSFORMER ISOLATED)	
Ref Voltage Level	115V rms ±10%
Max Voltage Without Damage	138V rms
Current	
No Load	
Option H	40 mA max
Option I	50 mA max
Additional With Load	1 mA per mA of load
POWER SUPPLY	
Voltage	+5V
Max Voltage Without Damage	+7V
Current	20 mA max
TEMPERATURE RANGES	
Operating (Temperature of Metal Plate on Top of Case)	
–1 Option	–55°C to +85°C
–3 Option	0°C to +70°C
Storage	–55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size (Encapsulated Module)	3.125 x 2.625 x 0.82 inch (7.94 x 6.67 x 2.08 cm)
Weight	8 oz. max (227 g)

TECHNICAL INFORMATION

INTRODUCTION

The DSC-544 circuit is divided onto 3 parts which are transformer isolated from each other (see Block Diagram). The first part contains the reference input, the second part contains the digital input and an internal digital to resolver converter, and the third part contains output power amplifiers and an associated pulsating power supply.

Reference input isolation is provided both by the reference transformer and by the power transformer. The converter output signals are proportional to the applied reference, and any distortion in the reference input will appear in the output signals. The power transformer output has a voltage clamp which protects the power amplifiers against transients in the reference input.

The internal digital to resolver (D/R) converter in the DSC-544 operates from an internal power supply connected to the reference input. The circuit in the internal D/R converter is based on an alogorithm whose theoretical math error is only ±3.5 arc-seconds (less than 5% of 1 LSB), and whose theoretical scale factor variation with angle is less than ±0.015%. The output is well behaved, with negligible glitches at major transition points. The accuracy and scale factor error are not limited by the physical components, not by the algorithm.

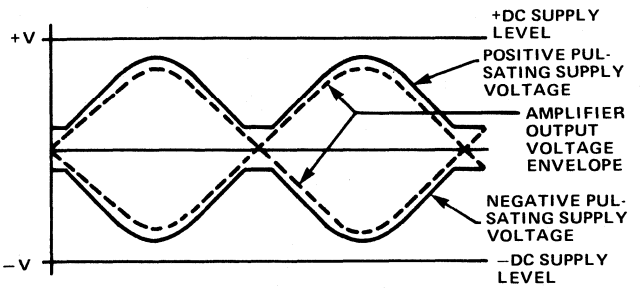
The digital inputs are transient protected CMOS switches with 33 KΩ pull-up resistors to the +5V supply, and can be driven by all standard TTL gates. If the TTL gates drive other loads as well, the circuit must allow the 33 KΩ resistors to pull up the logic 1 level to within 1.0V of the +5V supply. Bit weights for the 14 binary inputs are given in the bit weight table. Angle is determined by adding bits in the logic 1 state.

Bit	Deg/Bit	Min/Bit	Bit	Deg/Bit	Min/Bit
1MSB	180	10,800	8	1.406	84.38
2	90	5,400	9	0.7031	42.19
3	45	2,700	10	0.3516	21.09
4	22.5	1,350	11	0.1758	10.55
5	11.25	675	12	0.0879	5.27
6	5.625	337.5	13	0.0439	2.64
7	2.813	168.75	14LSB	0.0220	1.32

BIT WEIGHT TABLE

The most novel features of the DSC-544 converter are in the output section. The pulsating power supply produces two unfiltered, full-wave-rectified positive and negative voltages as shown in the diagram. These voltages are in the phase with the amplifier output voltage because the power is derived from the reference input. The amplitude of the two voltages need only be a few volts greater than the power amplifier output voltage, since both will change together if the reference level changes. As indicated in the diagram, the positive and negative pulsating power supply voltage levels will be consistently lower than the constant DC levels of any DC supplies. Because the voltage levels are lower, the power consumed will be much less. The power dissipated as heat is equal to the amplifier current times the difference in voltage between the power supply and the output. For the DSC-544, the power dissipated is reduced by approximately 50% for reactive loads.

Another advantage of deriving power from the reference input is that the amplifier section power is easily transformer isolated from the D/R converter. The converter output isolation transformer can therefore be located in front of the power amplifiers. Because it does not transfer power it can be made smaller, and an internal transformer can be used at 60 Hz.



PULSATING POWER SUPPLY VOLTAGE WAVEFORMS

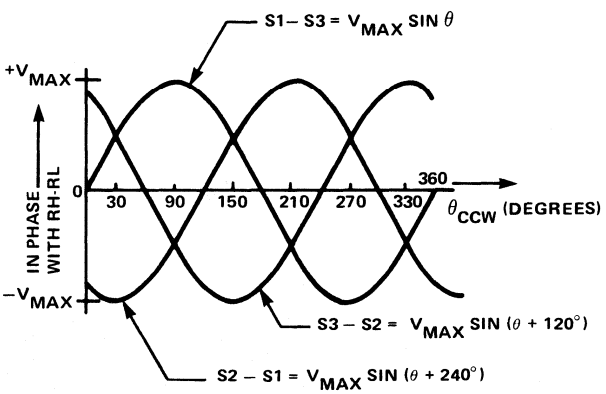
Minimum load impedances are listed in the Specifications Table under Drive Capability. The DSC-544 can drive these impedances under the worst case conditions stated in the table. The minimum load impedances correspond to 4.5 VA at 400 Hz and 1.5 VA at 60 Hz when the frequencies and voltage levels are at their nominal values. The metal top of the converter module should be provided with sufficient air circulation.

The thermal cutout disables the output power amplifiers when the internal temperature reaches 125° C. The output is automatically restored when the temperature drops again.

OUTPUT PHASING AND SCALE FACTOR

The analog output signals have the following phasing as shown in the synchro output signal diagram:

$S1 - S3 = (RH\text{-}RL)\ A_0\ (1 + A(\theta) \sin \theta$
$S3 - S2 = (RH\text{-}RL)\ A_0\ (1 + A(\theta) \sin (\theta + 120°)$
$S2 - S1 = (RH\text{-}RL)\ A_0\ (1 + A(\theta) \sin (\theta + 240°)$

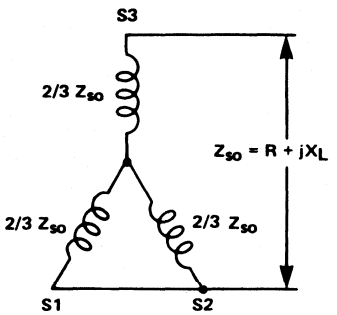


SYNCHRO OUTPUT SIGNALS

The output amplitudes simultaneously track reference voltage fluctuations because they are proportional to (RHRL). The amplitude factor A_0 is 90/115 for 90V rms L-L output. The maximum variation is A_0 from all causes is ±1.9%. The term A term $A(\theta)$ represents the variation of the amplitude with the digital input angle. $A(\theta)$, which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.001 for all values of θ. The total maximum variation in $A_0\ (1 + A(\theta))$ is therefore ±2%. Because $A(\theta)$ is so small, the DSC-544 can be used to drive systems such as X-Y plotters or CRT displays in which the sin and cos outputs are used independently (not ratiometrically as in control transformer).

DRIVING CT AND CDX LOADS

When driving CT and CDX loads the DSC-544 must have enough steady state power capability to drive the Z_{SO} of the load. Z_{SO} (stator impedance with rotor open-circuited) is measured as shown in the diagram:



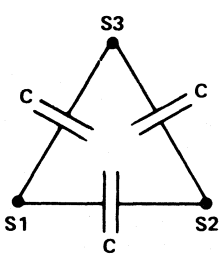
Z_{SO} MEASUREMENT

The following table shows the load impedance of some typical control transformers.

SOME COMMON CONTROL TRANSFORMERS AND THEIR LOAD IMPEDANCES

Military Type Number	Size	Z_{SO}
26V 08CT4c	08	100 + j490
26V 11CT4d	11	21 + j132
11CT4e	11	838 + j4955
15CT4c	15	1600 + j9300
15CT6b	15	1170 + j6780
18CT4c	18	1420 + j13260
18CT6b	18	1680 + j5040
23CT4a	23	1460 + j11050
23CT6a	23	1250 + j3980

Control transformers are highly inductive loads and it is possible to save power by tuning such loads. Three capacitors may be placed across the legs of the synchro stator in a delta configuration:



DELTA TUNING CONFIGURATION

The correct value of the capacitance C in Farads is given by:

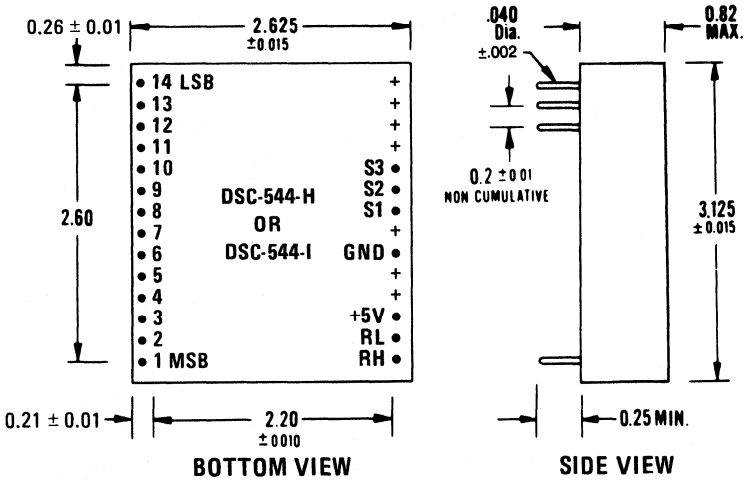
$$C = \frac{X_L}{4\pi f\,(R^2 + X^2)_L}$$

where f is the carrier frequency and R and X_L are the series real and reactive components of Z_{SO}. High grade capacitors must be used and they must be able to withstand the full AC output voltage.

When the load has been tuned more loads can be driven in parallel, because the load impedance Z is increased to:

$$Z = \frac{R^2 + X_L^2}{R}$$

MECHANICAL OUTLINE

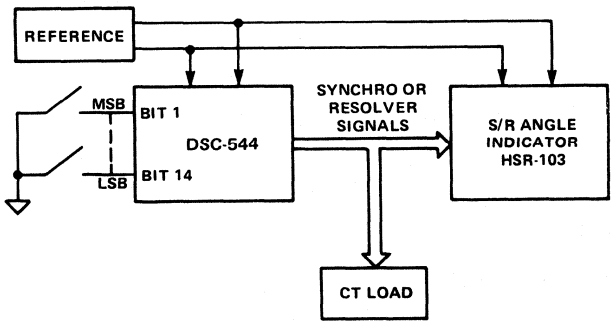


NOTES

1. Pin labels on bottom view are for reference only.
2. All dimensions shown are in inches.
3. Pin material meets solderability requirements of MIL-STD-202, Method 208C.
4. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F, except top surface is black anodized aluminum plate for heat transfer.
5. Any LSB pins not used should be grounded.

ACCURACY TESTS

The accuracy of the 544 may be tested with a high accuracy synchro/resolver angle indicator and a load such as a control transformer, as shown in the diagram. The bit switches are set to the desired test angles and the output angle is measured under load. The accuracy should conform to the specifications.



ORDERING INFORMATION

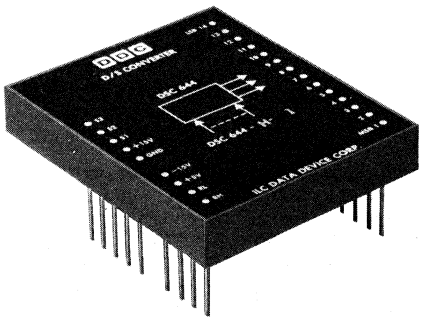
DSC 544 – H – 1 – R

- R = Enhanced Reliability
- Operating Temperature Range of Case Metal Top
  - 1 = -55° to +85° C
  - 3 = 0° C to +70° C
- Synchro Output Voltage Level and Frequency
  - H = 90 V rms L-L, 360-440 Hz
  - I = 90 V rms L-L, 57-63 Hz

If a converter module socket is required, order socket number 9010.

For further information, or help in ordering, call your nearest DDC representative listed in EEM.

14 BIT D/S AND D/R CONVERTER
New Low-profile Industry Standard



DESCRIPTION

The DSC-644 is the first low-profile D/S and D/R converter. It is only 0.52 inches high, has standard pin configuration, and is designed to be a new industry standard. The DSC-644 accepts 14 bit digital input angle and a reference excitation, and produces a synchro or resolver output with moderate drive capability. The output is fully protected to prevent damage to the converter. The rugged, current-limited power output stage has overload and transient protection, and a thermal cut off to prevent overheating. The output is short-circuit proof and an aluminum top plate improves the thermal dissipation. The DSC-644 also has a new circuit design that provides a more accurate output with an improved transient response and a negligible scale factor variation. Reliability has also been increased, and cost is reduced.

The DSC-644 module contains an input reference isolation transformer. An internal output transformer is also included for all 400 Hz versions. The 60 Hz option requires a separate output transformer.

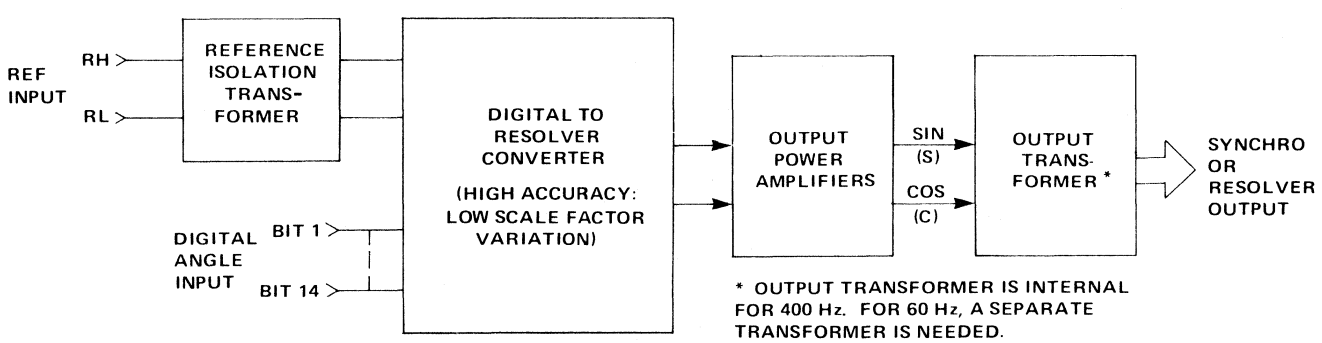
APPLICATIONS

The DSC-644 is used when digitized shaft angle data must be converted to synchro or resolver form to drive control transformers, control differential transmitters and angle indicators. Because these converters are very rugged, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial and military applications, including military ground support and avionics. They are used especially in computer based systems in which digital information is processed, such as simulators, flight trainers flight instrumentation, and fire control systems.

FEATURES

- *FULLY PROTECTED OUTPUT:*
  - *RUGGED OUTPUT AMPLIFIERS WITH CURRENT LIMITING*
  - *COMPLETELY SHORT-CIRCUIT PROOF*
  - *OVERVOLTAGE TRANSIENT PROTECTION*
  - *THERMAL CUTOFF*
- *METAL HEATSINK AT TOP OF CASE: CONSERVATIVE THERMAL DESIGN*
- *VERY LOW SCALE FACTOR VARIATION: 0.05% TYPICAL*
- *OUTPUT:*
  - *INTERNAL TRANSFORMER ISOLATION AT 400 Hz*
  - *ALL COMMON SYNCHRO/RESOLVER VOLTAGE LEVELS AND FREQUENCIES*
- *DIGITAL INPUT:*
  - *CMOS AND TTL COMPATIBLE PARALLEL BINARY ANGLE INPUT*
- *POWER REQUIRED:*
  - *±15V DC AND +5V DC*

*Patented



DSC-644 BLOCK DIAGRAM

DSC-644 SPECIFICATIONS

Apply over operating temperature and frequency ranges, ±5% variation of power supplies, ±10% reference amplitude variation, up to 10% reference harmonic distortion, and for any balanced load up to full load.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY (To Full Load)	
Output Accuracy	±4 minutes
Differential Linearity	±1 LSB max
DIGITAL INPUT	
Logic Type	Natural binary angle; parallel positive logic TTL compatible; Transient protected CMOS 33 KΩ pull-up to +5V
Loading	0.13 Std. TTL load

REFERENCE INPUT (TRANSFORMER ISOLATED)

	Ref. Voltage Level*	Max. Ref. Current
Units with 90V rms L-L Output	115V rms	0.6 mA
Units with 11.8V rms L-L Output	26V rms	0.6 mA

*+20% absolute max to avoid damage

ANALOG OUTPUT (TRANSFORMER ISOLATED)

Drive Capability (L-L Balanced*)	
Synchro Output	
90V rms L-L, 360 – 440 Hz (Option H)	4 KΩ min
90V rms L-L, 57 – 440 Hz (Option 6)	4 KΩ min
11.8V rms L-L, 360 – 440 Hz (Option L)	70 Ω min
Resolver Output	
11.8V rms L-L, 360 – 440 Hz (Option L)	93 Ω min
Output Scale Factor	
Absolute (All Causes)	±2% max simultaneous amplitude variation on all output lines, including variation with digital angle. Output amplitude tracks reference input amplitude.
Variation With Digital Angle	±0.1% max
Output Quadrature	±0.3% max

*The output amplifiers will drive loads with any phase angle from −90° to +90°.

POWER SUPPLIES

Voltage	+15V	−15V	+5V
Max Voltage Without Damage	+18V	−18V	+7V
Average Current	30 mA max	130 mA max	5 mA max
Peak Current With Normal Load	330 mA max	330 mA max	5 mA max
Peak Current at Power Turn-On or Short Circuit	450 mA max	450 mA max	5 mA max

TEMPERATURE RANGES

Operating (Temperature of Metal Plate on Top of Case)	
−1 Option	−55°C to +85°C
−3 Option	0°C to +70°C
Storage	−55°C to +125°C

PHYSICAL CHARACTERISTICS

Converter Module (encapsulated)	
Size	3.125 x 2.625 x 0.52 inch (7.94 x 6.67 x 1.32 cm)
Weight	5.1 oz max (145 g)
60 Hz Transformer Module (encapsulated)	
Size	2.25 x 2.25 x 0.81 inch (5.7 x 5.7 x 2.1 cm)
Weight	10.5 oz max (298 g)

TECHNICAL INFORMATION

INTRODUCTION

The DSC-644 contains an internal digital to resolver (D/R) converter (refer to the block diagram) which has an inherently high accuracy and low scale factor variation. The circuit in the internal D/R converter is based on an algorithm whose theoretical math error is only ±3.5 arc-seconds (less than 5% of 1 LSB), and whose theoretical scale factor variation with angle is less than ±0.015%. The output is well behaved, with negligible glitches at major transition points. The accuracy and scale factor error are now limited by the physical components, not by the algorithm.

The digital inputs are transient protected CMOS switches with 33 KΩ pull-up resistors to the +5V supply, and can be driven by all standard TTL gates. If the TTL gates drive other loads as well, the circuit must allow the 33 KΩ resistors to pull up the logic 1 level to within 1.0V of the +5V supply. Bit weights for the 14 binary inputs are given in the bit weight table. Angle is determined by adding bits in the logic 1 state.

Bit	Deg/Bit	Min/Bit
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.406	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14 LSB	0.0220	1.32

BIT WEIGHT TABLE

The internal reference input transformer provides isolation at both 60 Hz and 400 Hz, so a change of frequency will not cause damage. The input is specified for operation at a reference level of either 115V or 26V rms. The output signals are proportional to the applied reference, and any distortion in the reference input will appear in the output signals.

A thermal cutout disables the output power amplifiers when the internal temperature reaches 125°C. The output is automatically restored when the temperature drops again.

The DSC-644 will not be damaged by any sequencing order or interruptions in either the ±15V supplies or the reference input. However, if one of the 15V supplies is shut down or subsequently powered up, maximum turn on current (450 mA) will be drawn from the other 15V supply until the missing 15 V supply is restored.

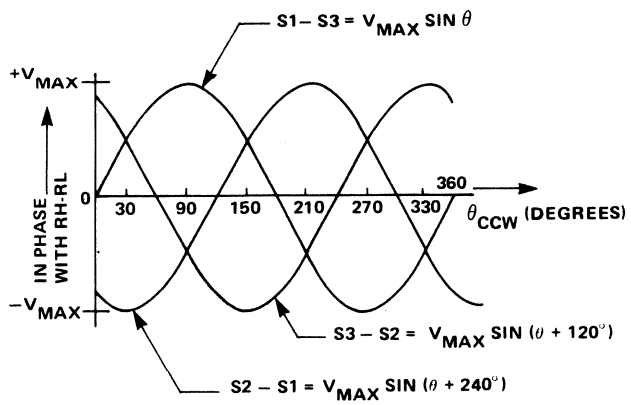
The 60 Hz synchro unit requires both a converter module (DSC-644-6) and a separate transformer because of the transformer size. The output power amplifiers on the −6 module provide a 7V rms nominal ±2% resolver signal for the external transformer when the reference input is 115V rms.

Minimum load impedances are listed in the Specifications Table under Drive Capability. The DSC-644 can drive these impedances under the worst case conditions stated in the table. The minimum load impedances correspond to a 1.5VA drive capability when the line voltages and frequencies are at their nominal values. The metal top of the converter module should be provided with sufficient air circulation.

DDC also manufactures the DSC-544, another D/S converter which provides 60 Hz and 400 Hz 90V L-L synchro output. The DSC-544 is a high efficiency, reference powered converter with a standard 0.82 inch high profile. It does not require ±15V power supplies. When driving the same load, the DSC-544 dissipates half as much power as the DSC-644. At 400 Hz the DSC-544 can drive 4.5VA compared to 1.5VA for the DSC-644. Both units can drive 1.5VA at 60 Hz, but the SDC-544 does not require an external transformer at this frequency.

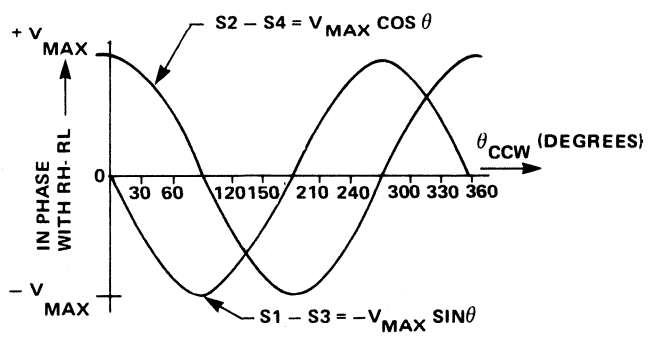
OUTPUT PHASING AND SCALE FACTOR

The analog output signals have phasing as shown in the following synchro and resolver output signal diagrams:



SYNCHRO OUTPUT SIGNALS

Synchro output
S1 – S3 = (RH-RL) A_0 (1 + A(θ)) sin θ
S3 – S2 = (RH-RL) A_0 (1 + A(θ)) sin (θ + 120°)
S2 – S1 = (RH-RL) A_0 (1 + A(θ)) sin (θ + 240°)



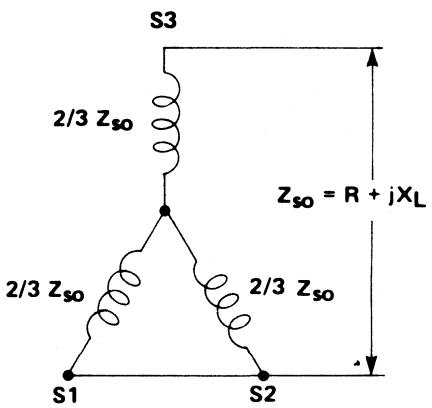
RESOLVER OUTPUT SIGNALS

Resolver output
S1 – S3 = –(RH-RL) A_0 (1 + A(θ)) sin θ
S2 – S4 = (RH-RL) A_0 (1 + A(θ)) cos θ

The output amplitudes simultaneously track reference voltage fluctuations because they are proportional to (RH-RL). The amplitude factor A_0 is 90/115 for 90V rms L-L output and 11.8/26 for 11.8V rms L-L output. The maximum variation in A_0 from all causes is ±1.9%. The term A(θ) represents the variation of the amplitude with the digital input angle. A(θ), which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.001 for all values of θ. The total maximum variation in A_0 (1 + A(θ)) is therefore ±2%. Because A(θ) is so small, the DSC-644 can be used to drive systems such as X-Y plotters or CRT displays in which the sin and cos outputs are used independently (not ratiometrically as in a control transformer).

DRIVING CT LOADS

When driving CT loads the DSC-644 must have enough power drive capability to drive the Z_{SO} of the load. Z_{SO} (stator impedance with rotor open-circuited) is measured as shown in the diagram:



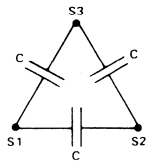
Z_{SO} MEASUREMENT

The following table shows the load impedance of some typical control transformers.

IMPEDANCES OF COMMON CONTROL TRANSFORMERS

Military Type Number	Size	Z_{SO}
26V 08CT4c	08	100 + j490
26V 11CT4d	11	21 + j132
11CT4e	11	838 + j4955
15CT4c	15	1600 + j9300
15CT6b	15	1170 + j6780
18CT4c	18	1420 + j13260
18CT6b	18	1680 + j5040
23CT4a	23	1460 + j11050
23CT6a	23	1250 + j3980

Control transformers are highly inductive loads and it is possible to save power by tuning such loads. Three capacitors may be placed across the legs of the synchro stator in a delta configuration:



DELTA TUNING CONFIGURATION

The correct value of the capacitance C in Farads is given by:

$$C = \frac{X_L}{4\pi f (R^2 + X_L^2)}$$

where f is the carrier frequency and R and X_L are the series real and reactive components of Z_{SO}. High grade capacitors must be used and they must be able to withstand the full AC output voltage.

When the load has been tuned more loads can be driven in parallel, because the load impedance Z is increased to:

$$Z = \frac{R^2 + X_L^2}{R}$$

ACCURACY TESTS

The accuracy of the 644 may be tested with a high accuracy synchro/resolver angle indicator and a load such as a control transformer, as shown in the diagram. The bit switches are set to the desired test angles and the output angle is measured under load. The accuracy should conform to the specifications.

TEST METHODS

DSC-644 converter modules are high quality products whose semiconductor components are hermetically sealed. These modules will meet the specific test methods and conditions of MIL-STD-202E shown unless alternative methods are specified by the customer in his procurement documentation.

METHOD	CONDITION	COMMENT
204C	C	10G, 2000 Hz vibration
213B	A	50G, 11ms shock
106D*	–	Moisture
107D	A	Thermal shock
101D	B	Salt spray
105C	B	50,000 ft. altitude

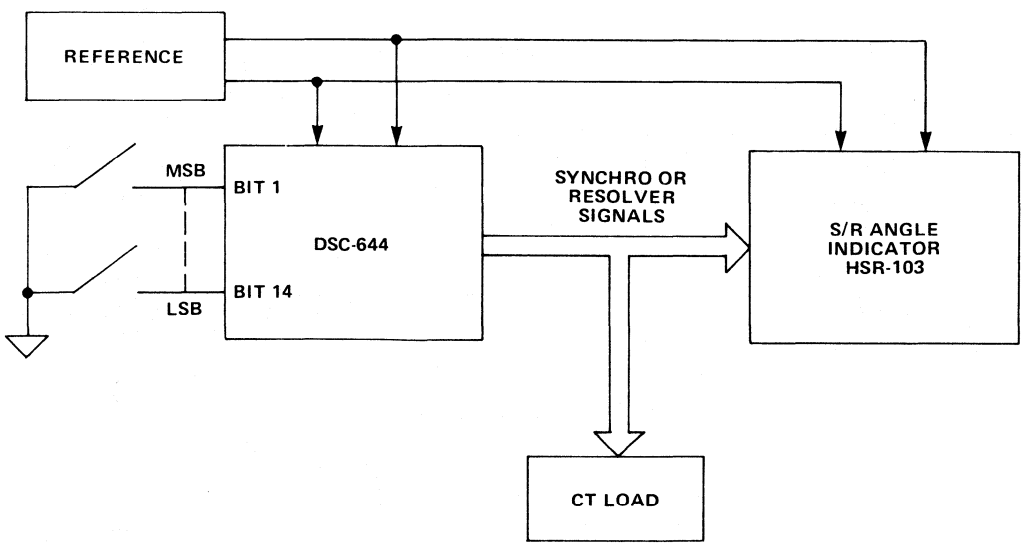
*when conformally coated on P.C. board

MIL-STD-202E TEST METHODS

PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc.

It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a pin connection by ripping out the plated through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.

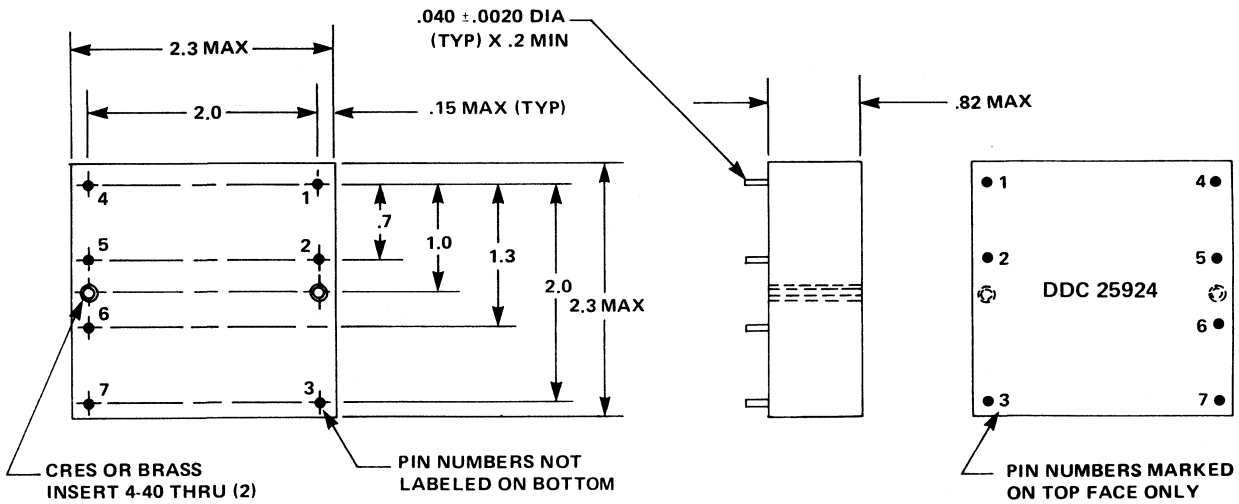


ACCURACY TEST CIRCUIT

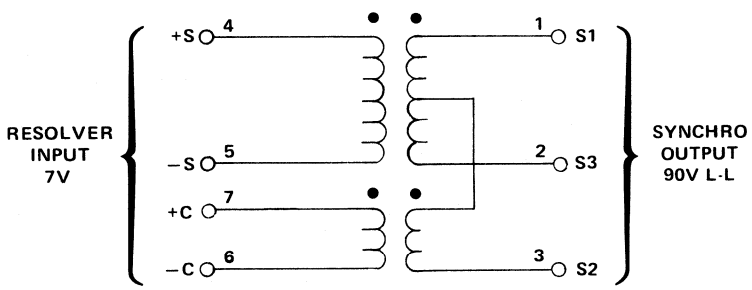
TRANSFORMER DIAGRAMS

60 Hz EXTERNAL SYNCHRO TRANSFORMER DDC-25924.

1. Mechanical Outline (Dimensions in inches, ±0.01 inch, unless otherwise indicated.)



2. Schematic Diagram

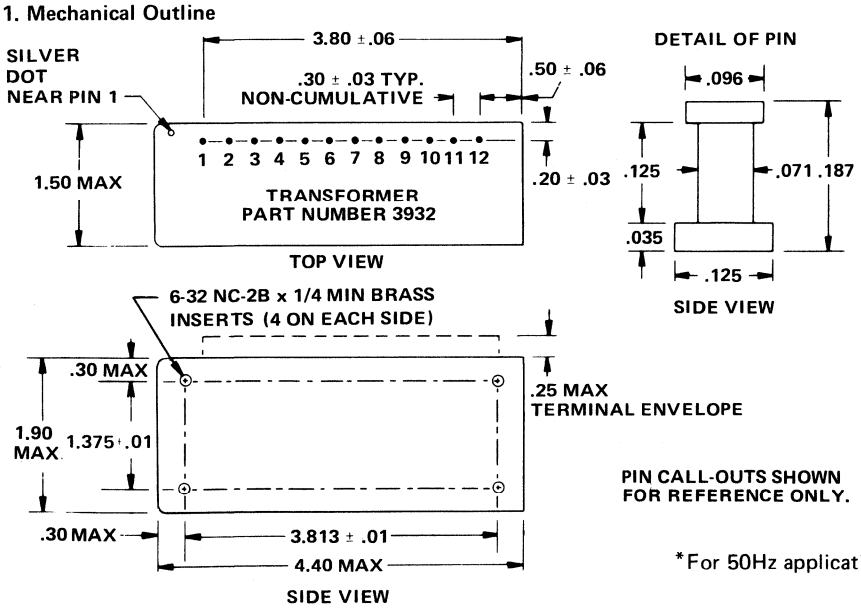


TRANSFORMER CONNECTIONS

Transformer Pin Number	Connect To
1	S1 } Synchro Output
2	S3 } 90V L-L
3	S2 } 57-440 Hz
4	SIN } To
5	GND } To
6	GND } Converter
7	COS } Module

50 Hz EXTERNAL SYNCHRO TRANSFORMER DDC-3932*

1. Mechanical Outline

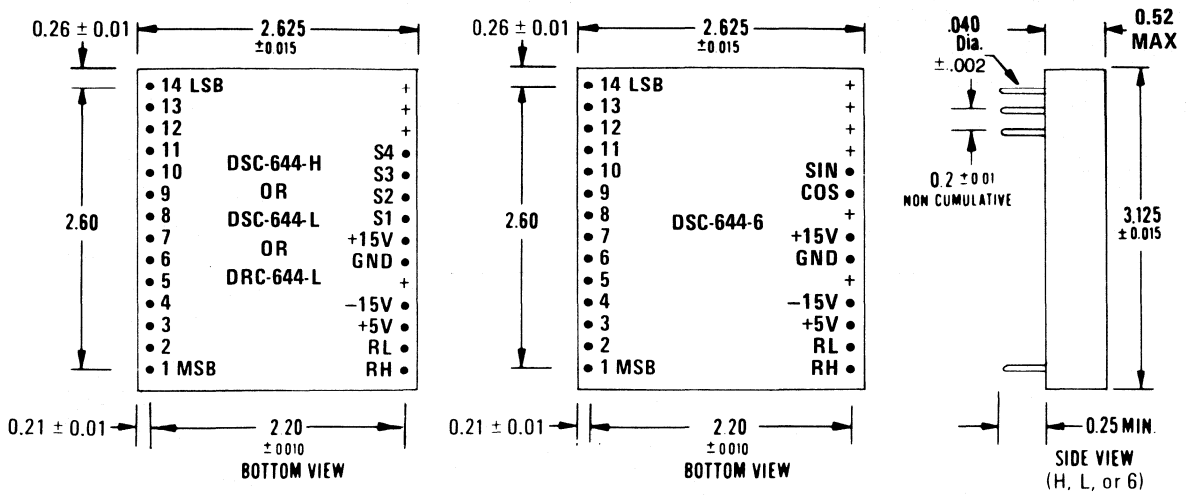


TRANSFORMER CONNECTIONS

Transformer Pin Number	Connect To
1	S1 } Synchro Output
2	S3 } 90V rms L-L
3	S2 } 47-440 Hz
4	SIN } To
5	GND } To
6	GND } Converter
7	COS } Module
8	RH } Do Not Use
9	RL } Do Not Use
10	+R } Do Not Use
11	RC } Do Not Use
12	–R } Do Not Use

*For 50Hz applications P/N DDC-3932 must be ordered.

MECHANICAL OUTLINE FOR CONVERTER MODULE



NOTES
1. Pin labels on bottom view are for reference only.
2. All dimensions shown are in inches.
3. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
4. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F, except top surface is a black anodized aluminum plate for heat transfer.
5. Pin S4 is present on resolver units only.
6. Any LSB pins not used should be grounded.

ORDERING INFORMATION

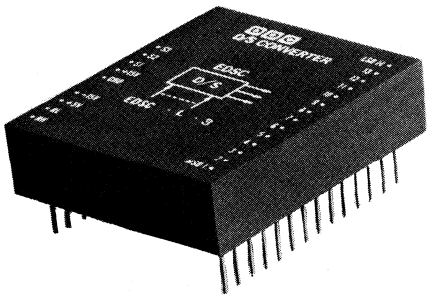
1. Order converter modules as follows. 400 Hz units (H and L) have an internal output transformer. 60 Hz units require an external transformer which must be ordered separately as desired below. If a converter socket is required, order socket number 9010.

DSC-644 – H – 1 – R

- R — High Reliability
- 1 — Operating Temperature Range of Metal Top
  - 1 = −55° C to + 85° C
  - 3 = 0° C to + 70° C
- H — Output Voltage Level and Frequency
  - H = 90 V rms L-L, 360-440 Hz (Synchro only)
  - L = 11.8 V rms, L-L, 360-440 Hz (Synchro or Resolver)
  - 6 = 90 V rms L-L, 47-440 Hz (synchro only) see No. 2 below
- DSC — Output Type
  - DSC = Synchro
  - DRC = Resolver

2. For -6 Option:
   (a) For 57-440 Hz application, either the transformer P/N DDC-3932 or DDC-25924 may be used.
   (b) For 47-440 Hz applications, transformer P/N DDC-3932 must be used. Reference pins should not be connected.

DDC
ILC DATA DEVICE CORPORATION



14 BIT D/S AND D/R CONVERTER
Improved Discrete Module

FEATURES

- *INDUSTRY STANDARD*
- *RUGGED OUTPUT POWER AMPLIFIERS WITH CURRENT LIMITING AND OVERVOLTAGE TRANSIENT PROTECTION*
- *METAL PLATE HEAT SINK AT TOP OF CASE – CONSERVATIVE THERMAL DESIGN*
- *ACCURACY: ±4 minutes*
- *OUTPUT: All common synchro and resolver voltages and frequencies*
  Low scale factor variation transformer isolation (internal at 400 Hz)
- *DIGITAL INPUT*
  TTL
  Parallel binary angle input
- *POWER REQUIRED: ±15V DC and +5V DC*

*Patented

DESCRIPTION

The EDSC* accepts a digital input angle and a reference excitation, and produces a synchro or resolver output with moderate drive capability. The industry standard, the EDSC has been redesigned with an aluminum top plate for better thermal dissipation, with a more rugged current-limited power output stage for short circuit and overload protection, with improved transient response, and with a lower scale factor variation. Reliability has been increased and cost reduced. The EDSC module contains an input reference isolation transformer, output power amplifiers, and output transformers.

APPLICATIONS

The EDSC is used when digitized shaft angle data must be converted to synchro or resolver form to drive control transformers, control differential transmitters and angle indicators. Because these converters are very rugged, and meet the requirements of MIL-STD-202E, they are suitable for the most severe industrial and military applications, including military ground support and avionics. They are used especially in computer based systems in which digital information is processed, such as simulators, flight trainers, flight instrumentation, and fire control systems.

SPECIFICATIONS

Apply over operating temperature and frequency ranges, ±5% variation of power supplies, ±10% reference amplitude variation, up to 10% reference harmonic distortion, and for any balanced load up to full load.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY	
Output Accuracy	±4 minutes
Differential Linearity	±1 LSB max
DIGITAL INPUT	
Logic Type	Natural binary angle; parallel positive logic TTL compatible
Loading	1 Std. TTL load

REFERENCE INPUT (TRANSFORMER ISOLATED*)

	Ref. Voltage Level*	Max Ref. Current
Units with 90V rms L-L Output	115V rms	3.3 mA rms
Units with 11.8V rms L-L Output	26V rms	5 mA rms

*+20% absolute max to avoid damage

ANALOG OUTPUT (TRANSFORMER ISOLATED*)

Drive Capability (L-L Balanced**)	
Synchro Output	
90V rms L-L, 360 – 440 Hz (Option H)	4 KΩ min
90V rms L-L, 47 – 440 Hz (Option 6)	4 KΩ min
11.8V rms L-L, 360-440 Hz (Option L)	100 Ω min
Resolver Output	
11.8V rms L-L, 360 – 440 Hz (Option L)	130 Ω min

PARAMETER	VALUE
Output Scale Factor	
Absolute (All Causes)	±5% max simultaneous amplitude variation on all output lines, including variation with digital angle. Output amplitude tracks reference input amplitude.
Variation With Digital Angle	±1% max
Output Quadrature	±0.2% max

** The output amplifiers will drive loads with any phase angle from –90° to +90°.

POWER SUPPLIES

Voltage	+15V	–15V	+5V
Max Voltage Without Damage	+18V	–18V	+7V
Average Current	150 mA max	130 mA max	50 mA max
Peak Current With Normal Load	450 mA max	450 mA max	50 mA max
Peak Current for 250 msec at Power Turn-On or Short Circuit	700 mA max	700 mA max	50 mA max

TEMPERATURE RANGES	
Operating (Temperature of Metal Plate on Top of Case)	
–1 Option	–55°C to +85°C
–3 Option	0°C to +70°C
Storage	–55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size (Encapsulated Module)	3.125 x 2.625 x 0.82 inch (7.94 x 6.67 x 2.08 cm)
Weight	8 oz max (227 g)

*Reference and Output Isolation Transformers are internal at 400 Hz; external at 60 Hz.

TECHNICAL INFORMATION

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing:

Synchro output

$S1 - S3 = (RH\text{-}RL)\ A_0\ (1 + A(\theta))\ \sin\theta$

$S3 - S2 = (RH\text{-}RL)\ A_0\ (1 + A(\theta))\ \sin(\theta + 120°)$

$S2 - S1 = (RH\text{-}RL)\ A_0\ (1 + A(\theta))\ \sin(\theta + 240°)$

Resolver output

$S1 - S3 = -(RH\text{-}RL)\ A_0\ (1 + A(\theta))\ \sin\theta$

$S2 - S4 = (RH\text{-}RL)\ A_0\ (1 + A(\theta))\ \cos\theta$

The output amplitudes simultaneously track reference voltage fluctuations because they are proportional to (RH-RL). The amplitude factor A_0 is 90/115 for 90V rms L-L output and 11.8/26 for 11.8V rms L-L output. The maximum variation in A_0 from all causes is ±4%. The term $A(\theta)$ represents the variation of the amplitude with the digital input angle. $A(\theta)$, which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.01 for all values of θ. The total maximum variation in $A_0(1 + A(\theta))$ is therefore ±5%.

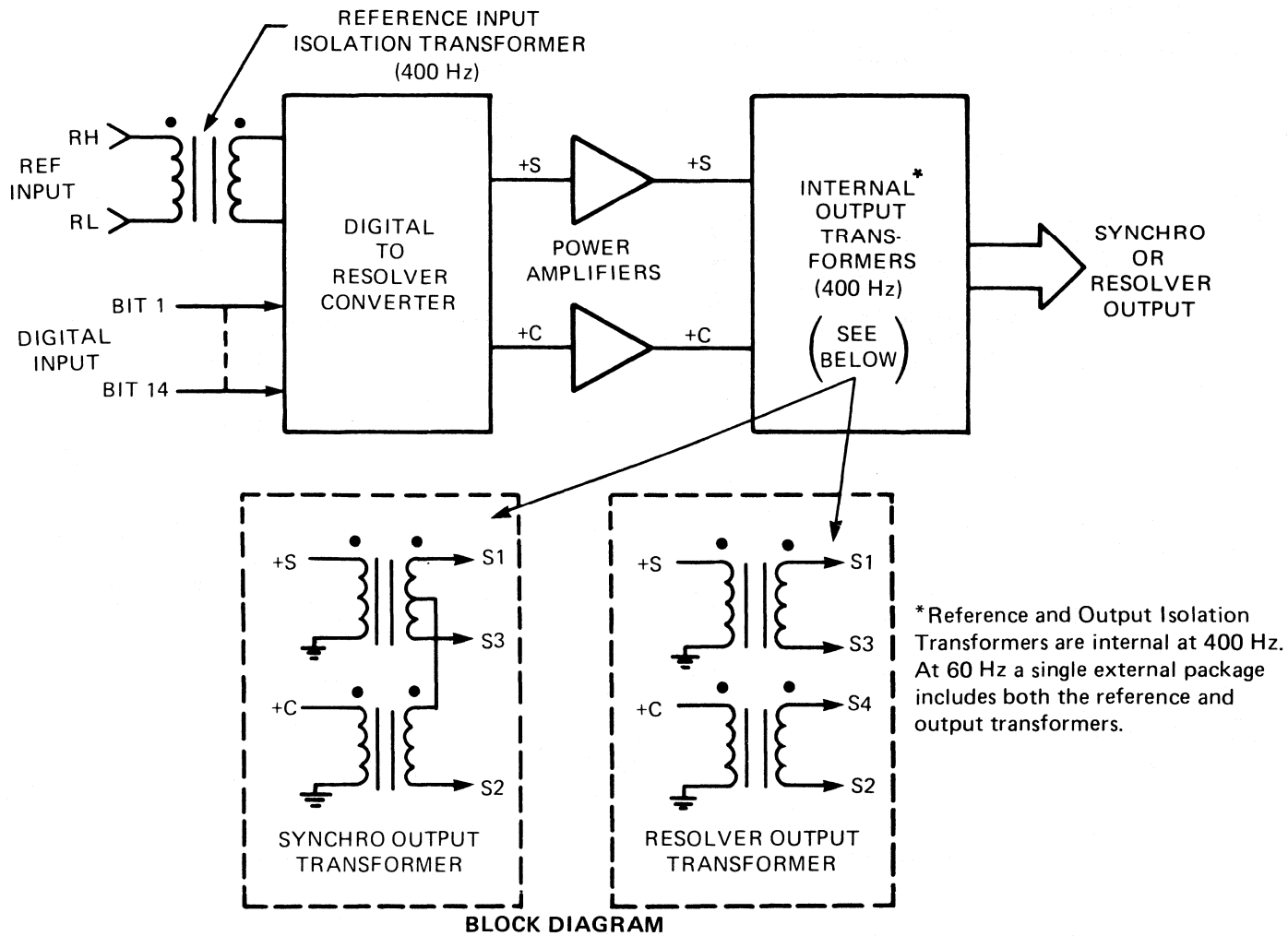
Because the amplitude factor (RH-RL) $A_0(1 + A(\theta))$ varies simultaneously on all output lines, it will not be a source of error when the EDSC is to drive a ratiometric system such as a synchro or resolver. However, if the outputs are used independently, as in X-Y plotters, the amplitude variations must be taken into account.

ORDERING INFORMATION

EDSC – H – 1

- 1 = Temperature of Case Metal Top (Operating)
  - 1 = –55°C to +85°C
  - 3 = 0°C to +70°C
- H = Output Voltage Level and Frequency
  - H = 90V rms L-L, 360-440 Hz (Synchro Only)
  - 6 = 90V rms L-L, 47-440 Hz (Synchro Only)
  - L = 11.8V rms L-L, 360-440 Hz (Synchro or Resolver)
  - M = 26V rms L-L, 360-440 Hz (Resolver only)
- EDSC = Output Type
  - EDSC = Synchro
  - EDRC = Resolver

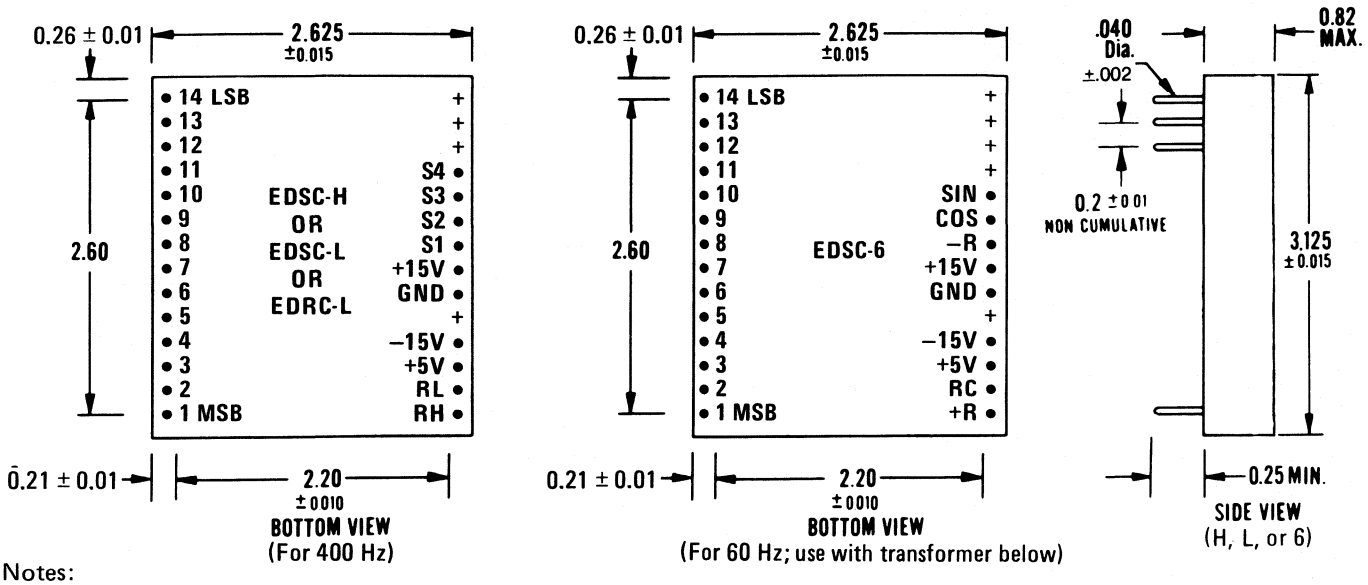
If a converter module socket is required, order socket number 9010.



BLOCK DIAGRAM

*Reference and Output Isolation Transformers are internal at 400 Hz. At 60 Hz a single external package includes both the reference and output transformers.

MECHANICAL OUTLINES FOR CONVERTER MODULE

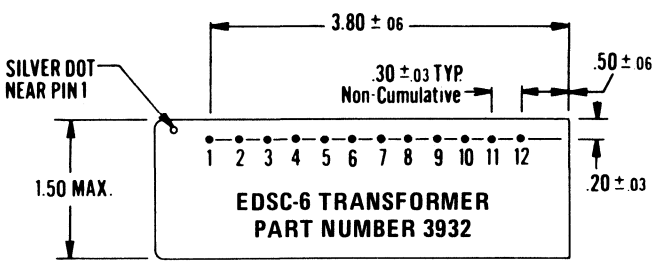


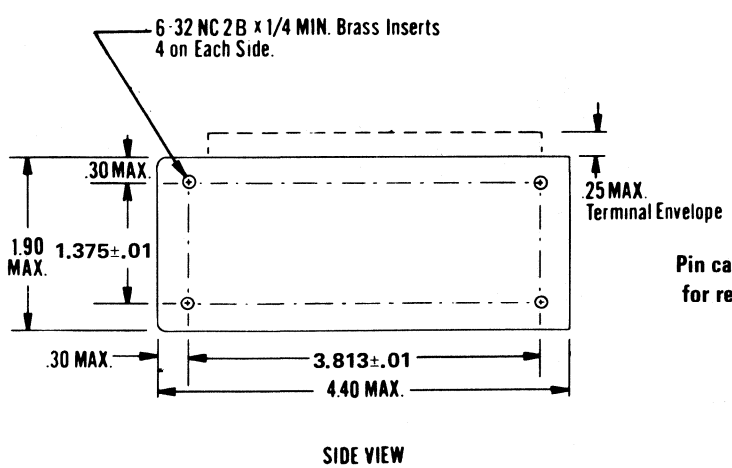
Notes:

1. Pin material is electrosoldered brass per MIL-F-14072, M222.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F, except top surface is a black anodized aluminum plate for heat transfer.
3. Pin S4 is present on resolver units only.
4. Any LSB pins not used should be grounded.

DIAGRAMS FOR 60 Hz TRANSFORMERS (EDSC-6)

TRANSFORMER MECHANICAL OUTLINE



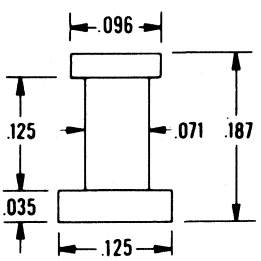


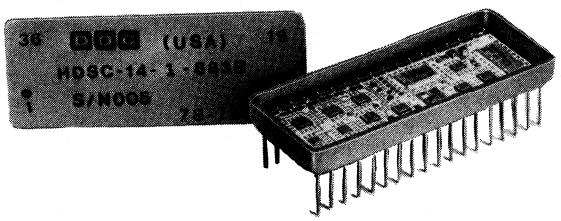
TRANSFORMER CONNECTIONS

Transformer Pin Number	Connect To	
1	S1	Synchro Output
2	S3	90V rms L-L
3	S2	50-60 Hz
4	SIN	To Converter Module
5	GND	
6	GND	
7	COS	
8	RH	Ref Input
9	RL	115V AC
10	+R	To Converter Module
11	RC	
12	−R	

Pin call-outs shown for reference only.

DETAIL OF PIN





14 BIT HYBRID D/S AND D/R CONVERTER Generates Sin/Cos DC or Rotating PPI Sweep

DESCRIPTION

The HDSC-14* is a versatile multiplying digital-to-analog converter. The digital input represents angle and the output is pin programmable either for resolver type sin/cos or for three-line synchro output. The reference input will accept any waveform, even a sawtooth for CRT drive. Because the reference is D.C. coupled to the output, the HDSC-14 can be used in many configurations:

With a synchro or resolver reference input, the HDSC-14 is a digital-to-synchro or digital-to-resolver converter.

With a D.C. reference input, the unit can be used as a hybrid digital-to-sin/cos DC converter.

With the reference input proportional to the radius vector, the HDSC-14 converts polar to rectangular coordinates.

With a sawtooth reference input and a rotating digital input, the module can generate a cartwheel rotating sweep for PPI displays.

Packaged in a 36 pin double DIP, the HDSC-14 is the only D/S and D/R converter complete in one hybrid module.

Hybrid technology results in low weight, low power consumption, very high reliability, and a wider operating temperature range. A new, improved circuit design allows higher accuracy and reduces the output scale factor so that the output can drive displays directly. The output line-to-line voltage can be scaled by external resistors. Other features include high AC and DC common mode rejection at the reference input and output short circuit protection.

APPLICATIONS

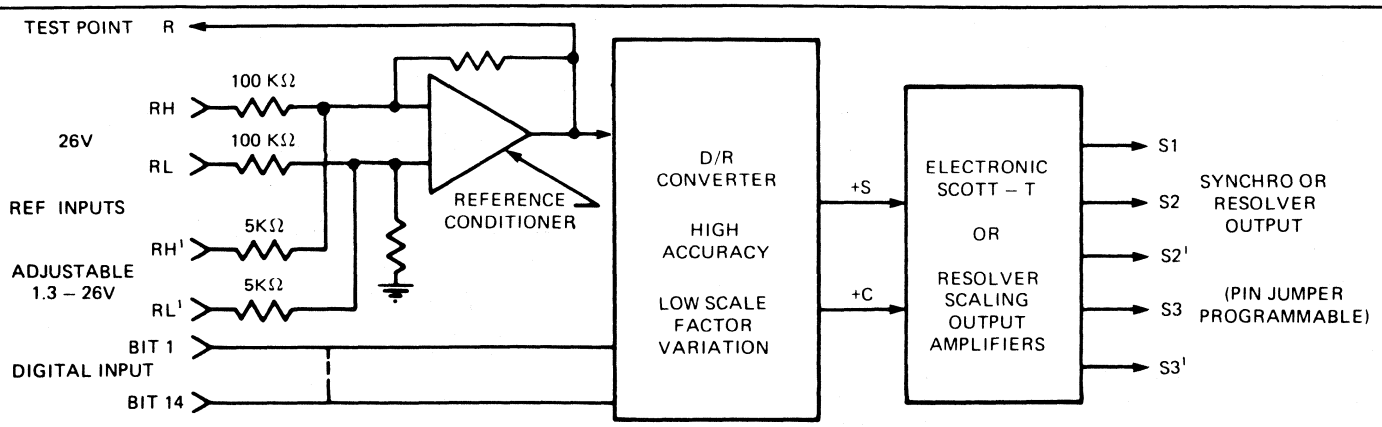
Because of its high reliability, small size and low power consumption, the hybrid HDSC-14 is ideal for remotely located and hard to access equipment, and suited to the most stringent and severe industrial and military ground or avionics applications. All units are processed to MIL-STD-883 Class C, with Class B processing as a standard option.

Among the many possible applications are computer based systems in which digital information is processed, such as simulators, flight trainers, flight instrumentation, fire control systems, radar and navigation systems, and PPI displays including moving target indicators.

FEATURES

- *ONE HYBRID MODULE CONTAINS COMPLETE D/S AND D/R CONVERTER*
- *PIN PROGRAMMABLE FOR SYNCHRO OR RESOLVER OUTPUT*
- *VERSATILE FUNCTION MODULE WITH MANY APPLICATIONS BECAUSE D.C. COUPLED REFERENCE ACCEPTS ANY WAVEFORM*
- *ACCURACY: ±4 minutes*
- *LOGIC: CMOS and TTL compatible Parallel binary angle input*
- *POWER REQUIRED: ±15V DC and logic voltage supply*

*Patented



HDSC-14 BLOCK DIAGRAM

SPECIFICATIONS

Apply over temperature range, power supply ranges, reference voltage and frequency range and 10% harmonic distortion in the reference.

PARAMETER	VALUE
Resolution	14 bits
ACCURACY AND DYNAMICS	
Output Accuracy	±4 minutes
Differential Linearity	±1 LSB max
Output Setting Time	Less than 20 μsec for any digital step change
DIGITAL INPUT	
Logic Type	Natural binary angle, parallel positive logic CMOS and TTL compatible Inputs are CMOS transient protected. Each input has a 20–80 KΩ pull-up resistor to V_L
Logic Voltage Level V_L	V = +4.5 V to +13 V Logic 0 = 0 to +0.2 V_L Logic 1 = 0.8 V_L to V_L
Load Current	±1 μA max plus pull-up resistor current
REFERENCE INPUT	
Type	Two differential solid state inputs, one for standard 26 V input and one programmable
Frequency Range	DC to 1000 Hz (to 10 KHz with reduced accuracy)
	Standard Input / Programmable Input
Voltage	26 V ±10% / 1.3 V min for full output. High voltages are scaled by adding two series resistors
Input Impedance	
Single Ended	100 KΩ ±0.5% / 5 KΩ ±0.5%
Differential	200 KΩ ±5% / 10 KΩ ±0.5%
ANALOG OUTPUT	
Type	Pin programmable for synchro or resolver mode
Output Current	2 mA rms max
Max Output Voltage (Tracks Reference Input Voltage)	11.8 V rms L-L ±0.4% nominal in synchro mode 6.81 V rms L-L ±0.4% nominal in resolver mode
Scale Factor Variation	Simultaneous amplitude variation in all output lines as a function of digital angle is ±0.2% max
D.C. Offset Each Line to Gnd	±50 mV max. Varies with input angle
Short Circuit Protection	Fully protected
POWER SUPPLIES	
Voltage	±15 V / -15 V / Logic Voltage V_L
Voltage Limits	±5% / ±5% / +4.5 V to 13 V
Max Voltage Without Damage	+18 V / -18 V / +15 V
Current or Impedance	30 mA max / 30 mA max / Z_{IN} = 1.5 KΩ min
TEMPERATURE RANGES	
Operating	
-1 Option	-55° C to +125° C
-3 Option	0° C to + 70° C
Storage	-55° C to +135° C
PHYSICAL CHARACTERISTICS	
Type	36 pin double DIP
Size	0.78 x 1.9 x 0.21 inch (2.0 x 4.8 x 0.53 cm)
Weight	0.85 oz (24g)

TECHNICAL INFORMATION

INTRODUCTION

As shown in the block daigram the signal conversion in the HDSC-14 is performed by a high accuracy digital to resolver converter whose sin and cos outputs have a low scale factor variation as a function of the digital input angle. This resolver output is either amplified by scaling amplifiers for resolver output, or is both amplified and converted to a synchro output by an electronic Scott-T. In both cases, the output line currents are limited to 2 mA rms max, which is sufficient for driving S/D converters, solid state control-transformers, and displays. Output power amplifiers will be required, however, for a driving electro-mechanical devices such as synchros and resolvers.

The reference conditioner has a differential input with high AC and DC common mode rejection, so that a reference isolation transformer will seldom be required. There are two sets of reference inputs. The RH, RL input provides the maximum synchro or resolver output voltage for a standard 26V rms reference input. The RH', RL' input is used to scale the output for other reference voltage levels. Series resistors can be added to the reference input as described below either to accommodate lower reference levels for full output, or to reduce the output level.

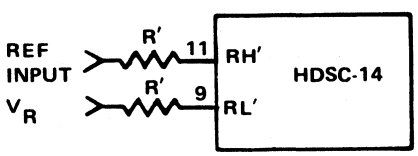
The reference conditioner output R is intended for test purposes. A signal between 2V and 2.5V at R indicates that a reference input signal is present.

OUTPUT SCALING AND REF. LEVEL ADJUSTMENT

The HDSC-14 operates like a multiplying D/A converter in that the voltage of each output line is directly proportional to the reference voltage.

The maximum line-to-line levels are determined by the output amplifiers and are nominally 11.8V for synchro output and 6.81V for resolver output. The RH, RL reference input is designed to provide this nominal output for the standard 26V reference level. The scaling adjustment is made by two internal 100 KΩ resistors in series with the reference conditioner input (see HDSC-14 Block Diagram). The maximum output levels without distortion are 10% greater than the nominal 11.8V and 6.81V levels.

The RH', RL' reference input has only 5 KΩ internal resistors in series with the reference conditioner input, so that nominal line-to-line output is obtained for a reference input of 1.3V. For higher reference voltages, two resistors R' must be inserted in series with the inputs as shown below. These resistors scale the HDRSC-14 outputs down to the nominal 11.8V and 6.81V levels stated above, or to lower voltages if desired. The magnitude of the resistors R' in ohms is calculated as follows:



$$R' = \frac{5000}{1.3}(V_R - 1.3)\left(\frac{\text{NOMINAL L-L VOLTAGE LEVEL}}{\text{DESIRED L-L VOLTAGE LEVEL}}\right)$$

OUTPUT PHASING AND OUTPUT SCALE FACTOR

The analog output signals have the following phasing:

Synchro output

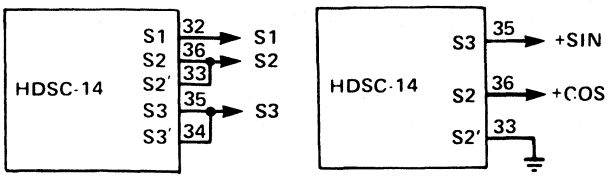
S3 – S1 = (RH-RL) A_O (1 + A(θ)) sin θ
S2 – S3 = (RH-RL) A_O (1 + A(θ)) sin (θ +120°)
S1 – S2 = (RH-RL) A_O (1 + A(θ)) sin (θ + 240°)

Resolver output

S3 = (RH-RL) A_O (1 + A(θ)) sin θ
S2 = (RH-RL) A_O (1 + A(θ)) cos θ

The output amplitudes simultaneously track reference voltage fluctuations because they are proportional to (RH-RL). The amplitude factor A_0 is 11.8/26 for 11.8V rms L-L output. The maximum variation in A_0 from all causes is ±0.2%. The term A (θ) represents the variation of the amplitude with the digital input angle. A (θ), which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.2% for all values of θ. The total maximum variation in A_0 (1 + A (θ)) is therefore ±0.4%.

Because the amplitude factor (RH-RL) A_0 (1 + A(θ)) varies simultaneously on all output lines, it will not be a source of error when the HDSC-14 is to drive a ratiometric system such as a synchro or resolver. However, if the outputs are used independently, as in X-Y plotters, the amplitude variations must be taken into account.



SYNCHRO OUTPUT RESOLVER OUTPUT

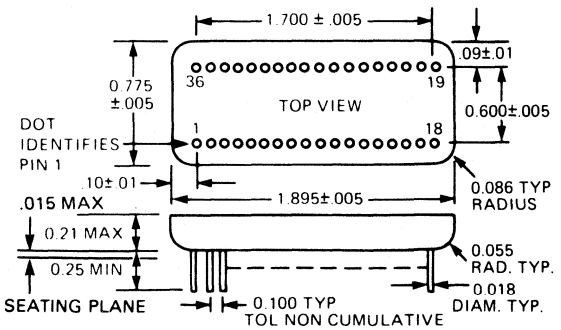
OUTPUT PIN PROGRAMMING

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All HDSC-14 hybrids are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5008 except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) is 1,320,000 hours, Ground Fixed, at 25°C.

MECHANICAL OUTLINE



PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING
PINS ARE KOVAR WITH GOLD PLATING: (50 μ INCH MIN).
CASE IS ELECTRICALLY FLOATING

PIN CONNECTION TABLE

Pin	Name	Pin	Name	Pin	Name
1	TP8	13	BIT 13	25	BIT 1 (MSB)
2	+15V	14	BIT 12	26	NC
3	GND	15	BIT 11	27	TP1
4	−15V	16	BIT 10	28	TP2
5	TP6 (−10V)	17	BIT 9	29	TP3
6	VL	18	BIT 8	30	TP4
7	TP7 (R)	19	BIT 7	31	TP5
8	RL	20	BIT 6	32	S1
9	RL′	21	BIT 5	33	S2′
10	RH	22	BIT 4	34	S3′
11	RH′	23	BIT 3	35	S3 (+SIN)
12	BIT 14 (LSB)	24	BIT 2	36	S2 (+COS)

NOTES:
1. Test points TP1 through TP5 and TP8 are for factory use only.
2. Test point TP6 (−10V) can be used in situations requiring lower power supply voltages and lower output voltage. Consult factory for further information.
3. Test point TP7 (R) can be used for test purposes to detect whether a reference signal is present. See block diagram.

ORDERING INFORMATION

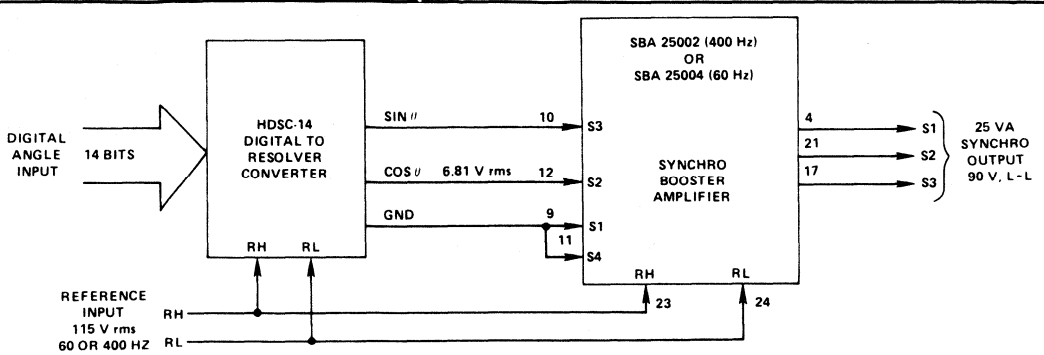
HDSC – 14 – 1 – 883B

MIL-STD-883 Processing:
883B = Conforms to MIL-STD-883 DDC procedures
Blank = Same, except pre burn in test and burn in are omitted.

Operating Temperature Ranges (Ambient):
1 = −55°C to +125°C
3 = 0°C to +70°C

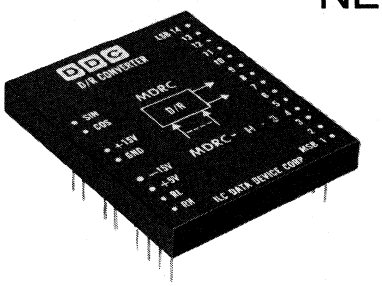
APPLICATION NOTE

The HDSC-14 can directly drive our Synchro Booster Amplifiers (Models SBA 25002 and 25004). The diagram below shows how to interconnect these two products.



HDSC-14/SBA CONNECTION DIAGRAM

14 BIT D/R CONVERTER
NEW LOW-PROFILE INDUSTRY STANDARD



FEATURES

- *LOW PROFILE MODULE 0.43 INCHES*
- *VERY LOW SCALE FACTOR VARIATION: 0.05% TYPICAL*
- *OUTPUT: 6.81V RMS SINE & COSINE*
- *OUTPUT MAGNITUDE/PHASE SCALEABLE WITH A RESISTOR/ CAPACITOR*
- *DIGITAL INPUT: CMOS AND TTL COMPATIBLE PARALLEL BINARY ANGLE INPUT*
- *POWER REQUIRED: ±15V DC AND +5V DC*

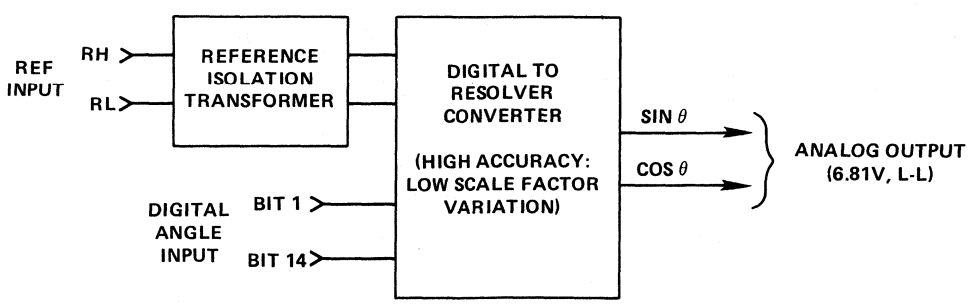
*Patented

DESCRIPTION

The MDRC is a low-profile D/R converter. It is only 0.43 inches high, has standard pin configuration, and is designed to be a new industry standard. The MDRC accepts 14 bit digital input angle and a reference excitation, and produces a sine or cosine output that is short-circuit proof. The MDRC also has a new circuit design that provides a more accurate output with an improved transient response and a negligible scale factor variation. Reliability has also been increased, and cost is reduced. The module contains an input reference isolation transformer.

APPLICATIONS

The MDRC is used when digitized shaft angle data must be converted to resolver form to drive synchro booster amplifiers, plan position indicators, moving target indicators and angle indicators. Because these converters are very rugged, and meet the requirements of MIL-STD-202, they are suitable for the most severe industrial and military applications, including military ground support and avionics. They are used especially in computer based systems in which digital information is processed, such as simulators, flight trainers flight instrumentation, and fire control systems.



MRDC BLOCK DIAGRAM

MDRC SPECIFICATIONS

Apply over operating temperature and frequency ranges, ± 5% variation of power supplies, ± 10% reference amplitude variation, up to 10% reference harmonic distortion, and for any balanced load up to full load.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY (To Full Load)	
Output Accuracy	± 4 minutes
Differential Linearity	± 1 LSB max
DIGITAL INPUT	
Logic Type	Natural binary angle; parallel positive logic TTL compatible. Transient protected CMOS 33 KΩ pull-up to + 5V
Loading	0.13 Std. TTL load
REFERENCE INPUT (TRANSFORMER ISOLATED)	Ref. Voltage Level* / Max. Ref. Current: 115V rms / 0.6 mA; 26V rms / 0.6 mA
	*+20% absolute max to avoid damage
ANALOG OUTPUT	
Drive Cabability (L-L Balanced)	
Resolver Output	
6.81 V rms L-L 47-440	2KΩ min
Output Scale Factor	
Absolute (All Causes)	± 2% max simultaneous amplitude variation on all output lines, including variation with digital angle. Output amplitude tracks reference input amplitude.
Variation With Digital Angle	± 0.1% max
POWER SUPPLIES	+ 15V / − 15V / + 5V
Voltage	
Max Voltage Without Damage	+ 18V / − 18V / + 7V
Current	20 mA max / 20 mA max / 5 mA max
TEMPERATURE RANGES	
Operating Temperature	
− 1 Option	− 55°C to + 105°C
− 3 Option	0°C to + 70°C
Storage	− 55°C to + 125°C
PHYSICAL CHARACTERISTICS	
Converter Module (encapsulated)	
Size	3.125 X 2.625 X 0.43 inch (79.4 X 66.7 X 11 mm)
Weight	4 oz max (113g)

TECHNICAL INFORMATION

INTRODUCTION

The MDRC contains an internal digital to resolver (D/R) converter (refer to the block diagram) which has an inherently high accuracy and low scale factor variation. The circuit in the internal D/R converter is based on an algorithm whose theoretical math error is only ± 3.5 arc-seconds (less than 5% of 1 LSB), and whose theoretical scale factor variation with angle is less than ± 0.015%.

The output is well behaved, with negligible glitches at major transition points. The accuracy and scale factor error are now limited by the physical components, not by the algorithm.

The digital inputs are transient protected CMOS switches with 33 KΩ pull-up resistors to the + 5V supply, and can be driven by all standard TTL gates. If the TTL gates drive other loads as well, the circuit must allow the 33 KΩ resistors to pull up the logic 1 level to within 1.0V of the +5V supply. Bit weights for the 14 binary inputs are given in the bit weight table. Angle is determined by adding bits in the logic 1 state.

Bit	Deg/Bit	Min/Bit
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.406	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14 LSB	0.0220	1.32

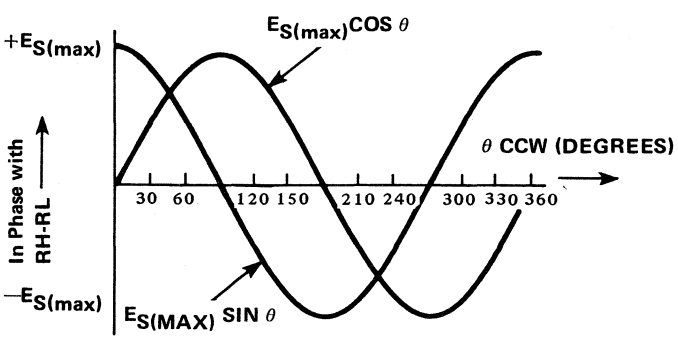
BIT WEIGHT TABLE

The internal reference input transformer provides isolation at 47 to 440 Hz, so a change of frequency will not cause damage. The input is specified for operation at a reference level of either 115V or 26V rms. The output signals are proportional to the applied reference, and any distortion in the reference input will appear in the output signals.

The MDRC will not be damaged by any sequencing order or interruptions in either the ± 15V supplies or the reference input.

OUTPUT PHASING AND SCALE FACTOR

The analog output signals have phasing as shown in the following resolver output signal diagram.



Resolver Signals

Resolver output

$$+\text{SIN to WRT} = (\text{RH-RL})\, A_0\, (1 + A(\theta))\, \sin\theta$$
$$+\text{COS to WRT} = (\text{RH-RL})\, A_0\, (1 + A(\theta))\, \cos\theta$$

The output amplitudes simultaneously track reference voltage fluctuations because they are proportional to (RH-RL). The amplitude factor A_o is 6.81/115 for 115V rms reference input and 6.81/26 for 26V rms reference input. The maximum variation in A_o from all causes is ±1.9%. The term $A(\theta)$ represents the variation of the amplitude with the digital input angle. $A(\theta)$, which is called the scale factor variation, is a smooth function of θ without discontinuities and is less than ±0.001 for all values of θ. The total maximum variation in A_o $(1 + A(\theta))$ is therefore ±2%. Because $A(\theta)$ is so small, the MDRC can be used to drive systems such as X-Y plotters or CRT displays in which the sin and cos outputs are used independently (not ratiometrically as in a control transformer).

ACCURACY TESTS

The accuracy of the MDRC may be tested with a high accuracy synchro/resolver angle indicator and a load such as shown in the diagram. The bit switches are set to the desired test angles and the output angle is measured under load. The accuracy should conform to the specifications.

TEST METHODS

MDRC converter modules are high quality products whose semiconductor components are hermetically sealed. These modules will meet the specific test methods and conditions of MIL-STD-202 shown unless alternative methods are specified by the customer in his procurement documentation.

METHOD	CONDITION	COMMENT
204	C	10G, 2000 Hz vibration
213	A	50G, 11ms shock
106*	—	Moisture
107	A	Thermal shock
101	B	Salt spray
105	B	50,000 ft. altitude

*when conformally coated on P.C. board

MIL-STD-202 TEST METHODS

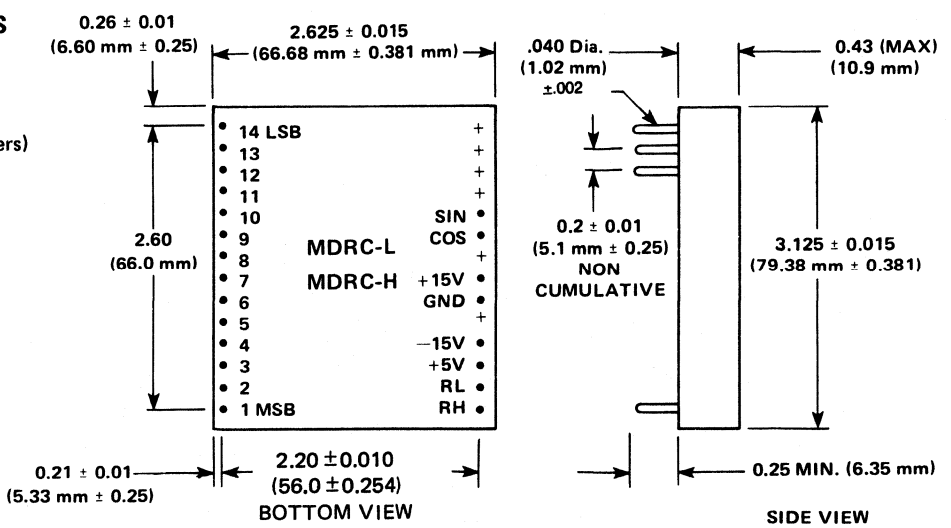
PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc.

It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of the PC board from the module, there will be no risk of destroying a pin connection by ripping out the plated through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.

MECHANICAL OUTLINES FOR CONVERTER MODULE

Dimensions in inches (millimeters)



NOTES
1. Pin labels on bottom view are for reference only.
2. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
3. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.
4. Any LSB pins not used should be grounded.

ORDERING INFORMATION

MDRC —H —1 —R

- R=Enhanced reliability
- Operating Temperature Range
  - 1 = 55°C to + 105°C
  - 3 = 0°C to + 70°C
- Output Voltage Level and Frequency
  - H = 47 to 440 Hz, Reference Input 115V rms
  - L = 47 to 440 Hz, Reference Input 26V rms

Note: If a converter socket is required, order socket number 9010.

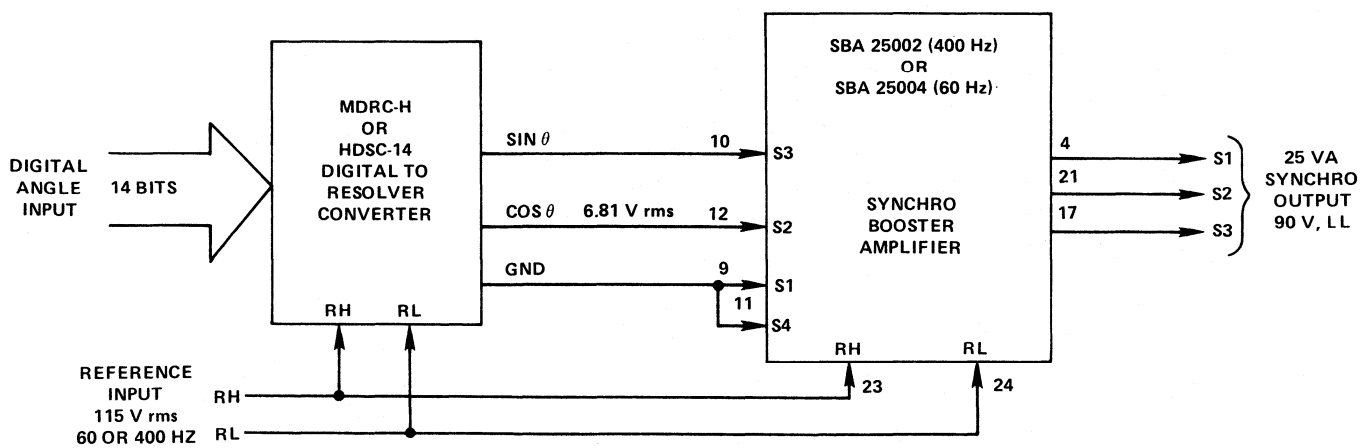
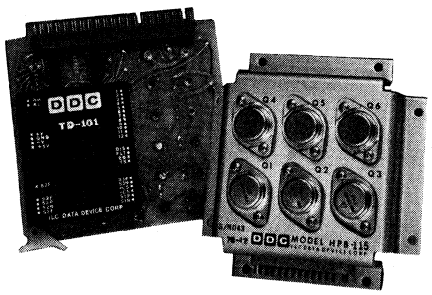


FIGURE 5. MDRC/SBA CONNECTION DIAGRAM



12 BIT HIGH POWER D/S TORQUE DRIVER
Fully Protected Output

DESCRIPTION

The TD-100 and TD-101 are torque drivers which accept digital angle input and produce a high power 3-line synchro output. This output can drive torque receivers or multiple CT or CDX loads. A complete unit has either of the following two configurations:

TD-100: A PC card containing both the D/S converter and an output power-buffer designed for convection cooling. Drive capability is 3 amps peak.

TD-101: A PC card containing the D/S converter and a separate output power-buffer which can be bolted to a chassis for conductive cooling. Drive capability is either 4 or 15 amps peak, depending on choice of buffer.

In addition, separate isolation transformers are available for both the synchro output and the reference input.

The TD-100 and TD-101 incorporate special features which protect them against overloading and which allow them to be computer-controlled in a sophisticated fashion to conserve power. A current sense, a thermal sense, and a voltage transient clamp protect the TD-100 and TD-101 against overloads, stalled rotor conditions, inductive kickback, and power supply loss. All units contain logic controls which can be used to switch the output off to conserve power, or to switch it on to continue operation in spite of thermal overload under battle short conditions. To warn when operating conditions are not normal, a fault indicator goes to logic 1 whenever the thermal or current sense indicates overload, or when the disable is applied.

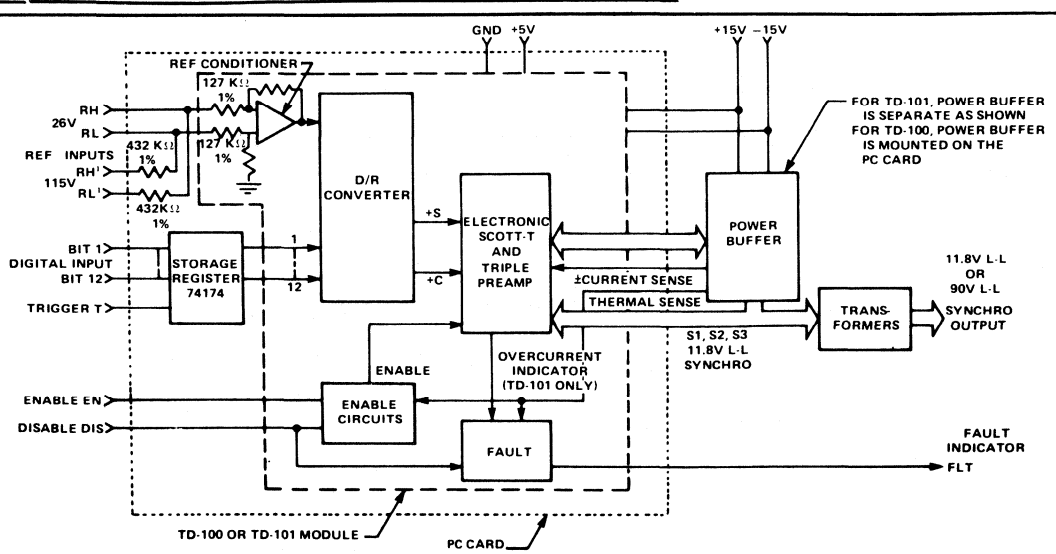
APPLICATIONS

The TD-100 and TD-101 are rugged units, requiring no calibrations or adjustments. They are used in training simulators, remote indicators, gun fire control, and shipboard retransmission systems. Their power conserving features recommend them especially for installations requiring multiple units, and their control features are designed for computer supervision.

FEATURES

- *VIRTUALLY INDESTRUCTIBLE:*
  - *PROTECTED AGAINST SHORT CIRCUITS, OUTPUT OVERLOADING, THERMAL OVERLOAD, VOLTAGE TRANSIENTS, AND POWER SUPPLY SHUTDOWN*
- *OUTPUT:*
  - *DESIGNED TO DRIVE BOTH CT OR CDX PASSIVE LOADS AND TORQUE RECEIVERS*
  - *DIRECTLY COUPLED 11.8V L-L OUTPUT*
  - *WITH OUTPUT ISOLATION TRANSFORMERS: 400 Hz AT 11.8V L-L, AND 60 Hz OR 400 Hz AT 90V L–L*
  - *PEAK POWER UP TO 108 VA*
- *ACCURACY:*
  - *±21 MINUTES, FULL LOAD*
  - *±10 MINUTES, NO LOAD*
- *LOGIC:*
  - *TTL COMPATIBLE*
  - *PARALLEL BINARY ANGLE INPUT WITH STORAGE REGISTER*
  - *OUTPUT CAN BE ENABLED OR DISABLED*
  - *FAULT INDICATOR*
- *POWER REQUIRED: ±15V DC AND +5V DC*

*Patented



TD-100 AND TD-101 BLOCK DIAGRAM

SPECIAL FEATURES

Current Limiting. The card mounted power buffer and the HPB power buffer both contain a current sense which is used to limit the output current. The limiting value is the peak transient output power listed in the specifications.

Thermal Sense. If the thermal sense in the power buffer heat sink indicates a temperature exceeding 125°C, the enable circuits will shut off the triple amplifier output until the temperature drops below 125°C. The Fault Indicator will also be activated to indicate a fault.

Fault Indicator. The Fault Indicator signals when the output is off because of thermal overload or because the disable has been applied. In the TD-101, it also signals when the current has exceeded 2/3 of the peak transient current level.

Disable. The Disable shuts down the output. It can be used to conserve power when the output is not needed. When several torque drivers are used, the Disable lines can be used to sequence turn-on so that a smaller power supply is required.

Enable. This control line overrides the thermal sense so that operation can continue in spite of a thermal overload.

Voltage Transient Clamp. The buffer output stage is protected against voltage transients caused by inductive kickback from the load.

Power Supply Shutdown Protection. The power buffer will shut down if any of the power supplies is shut off or disconnected.

TECHNICAL INFORMATION

OUTPUT PHASING AND SCALE FACTOR

The AC amplitudes of the synchro output lines can be described as follows:

$$S1 - S3 = A_0\ (1 + A(\theta)(RH\text{-}RL) \sin\theta \sin\omega t$$
$$S3 - S2 = A_0\ (1 + A(\theta)(RH\text{-}RL) \sin(\theta + 120^\circ) \sin\omega t$$
$$S2 - S1 = A_0\ (1 + A(\theta)(RH\text{-}RL) \sin(\theta + 240^\circ) \sin\omega t$$

The scale factor, $A_0\ (1 + A(\theta)(RH\text{-}RL)$, is proportional to the reference voltage (RH-RL). The angular independent term A_0 is accurate to within ±2%. In addition, there is an angular dependence expressed by the scale factor variation $A(\theta)$. $A(\theta)$ is ±8% for the TD-100, but only ±1% for the TD-101 because the D/R converter within the TD-101 module has an inherently low scale factor variation. The scale factor variation will not cause errors in situations where the outputs are used ratiometrically as, for instance, to drive synchros.

SPECIFICATIONS

Apply over temperature range, power supply range, ±10% reference voltage and frequency variation, and ±10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	12 bit binary angle input
ACCURACY (All Causes, Balanced Load)	±21 minutes full load ±10 minutes no load

DIGITAL INPUT/OUTPUT (TTL Compatible)

Digital Inputs	
12 Parallel Data Bits	Natural binary angle; positive logic
Trigger (T)	Trigger for card-mounted storage register for input data bits Triggers on positive edge
Disable (DIS)	Logic 1 or open: Shuts down the output Logic 0 or GND: Normal operation
Enable (EN)	Logic 1 or open: Overrides thermal cutout Logic 0 or GND: Allows thermal cutout to operate normally
Fault Indicator Output (FLT)	Logic 0: normal operation Logic 1: indicates any of the following three conditions: (1) Thermal overload (trip point = 125° C) (2) Disable (DIS) is at logic 1 so that the output is shut down (3) Current overload for TD-101 (not for TD-100). Trip point is at approximately 2/3 of peak current setting. For the HPB-14, the trip point is about 2.7A, which corresponds to 20 VA output. For the HPB-115, the trip point is about 10A, corresponding to 75 VA output.

Loading or Drive Capability	Logic Type	Loading (STD TTL)	Pullup To +5V (Nominal)	Voltage Levels or Logic 0 Current
12 Parallel Data Bits				
TD-100 Module or Card	TTL	1		
TD-101 Module	CMOS		33 KΩ	logic 0 ≤ 1V logic 1 ≥ 1V less than +5V supply
TD-101 Card Mounted	TTL	1		
Trigger (Card Mtd Units Only)	TTL	2		
Disable and Enable				
TD-100	TTL	1		
TD-101	LS	0.2		
Fault Indicator				
TD-100			6 KΩ	6.4 mA
TD-101			4.7 KΩ	3.2 mA

REFERENCE INPUT

Frequency Range	47–440 Hz, solid state differential input
Voltage Levels	26V rms or 115V rms, separate inputs

Minimum Input Impedance (Balanced, Resistive)

	Differential	Single Ended
26V Input	260 KΩ	130 KΩ
115V Input	1100 KΩ	550 KΩ

Common Mode Range (DC level plus recurrent AC peak)	
26V Input	50V rms
115V Input	250V rms

PARAMETER	VALUE		
SYNCHRO OUTPUT			
Voltage Level			
L-L Voltage	11.8V direct output 11.8V or 90V transformer output Output voltage level tracks reference level		
Scale Factor	±2% max compared to nominal 11.8V or 90V		
Scale Factor Variation			
TD-100	±8% max variation with angle		
TD-101	±1% max variation with angle		
Output Power	CMA and CMB	HPB-14	HPB-115
Peak Transient	25W	32W	125W
Steady State	8 VA	20 VA	30 VA
Transformer Parameters	Transformer Number	Input Imped. Z_{SO} Min	Output Imped. Z_{SS} Max
For CMA and HPB-14 Options			
360–440 Hz, 90V rms L-L	18884	50Ω	40Ω
360–440 Hz, 11.8V rms L-L	18883	100Ω	1.0Ω
57–63 Hz, 90V rms L-L	18885	100Ω	110Ω
For HPB-115 Options			
360–440 Hz, 90V rms L-L	24748	60Ω	20Ω
57–63 Hz, 90V rms L-L	22638	12Ω	15Ω
Input Voltage, All Transformers	11.8V rms L-L		
POWER SUPPLIES			
Voltage	+15V±5%	−15V±5%	+5V±5%
Max Voltage Without Damage	+18V	−18V	+7V
Current	65 mA + load	40 mA + load	150 mA
Max Continuous Current			
CM and CMA Options	1A	1A	
HPB-14	2.5A	2.5A	
HPB-115	3.6A	3.6A	
Current Limiting			
CM and CMA Options	3A peak	3A	
HPB-14	4A	4A	
HPB-115	15A	15A	
THERMAL CHARACTERISTICS			
Temperature Ranges			
Operating (PC Card and Transformer Ambient; HPB Chassis Temperature)			
−1	−55°C to +85°C		
−3	0°C to +70°C		
Storage	−55°C to +125°C		
Heat to be Dissipated	2.5 Watts per VA delivered		
Thermal Resistance at Junction of Power Transistor and Heat Sink			
CM and CMA Options	7°C/Watt, with natural convection		
HPB-14	2°C/Watt, conduction cooling		
HPB-115	1.7°C/Watt, conduction cooling		
PHYSICAL CHARACTERISTICS			
PC Card, Options 100CM and 100CMA			
Size	5.38 x 5.26 x 0.73 high inch (13.7 x 13.4 x 1.9 cm)		
Weight	8 oz (227 g)		
PC Card Option 101CMB			
Size	5.38 x 5.26 x 0.65 high inch (13.7 x 13.4 x 1.7 cm)		
Weight	12.5 oz (355 g)		
HPB-14 and HPB-115 Buffer			
Size	5 x 5 x 1.35 inch (12.7 x 12.7 x 3.4 cm)		
Weight	11 oz (312 g)		
Transformers	See Mechanical Outline drawings		

DRIVING TORQUE RECEIVERS

A torque driver must have a peak transient output power capacity sufficient to drive a torque receiver to null, as well as enough steady state power capability to maintain the torque receiver at null. The various TD-100 and TD-101 models can drive the following torque receiver loads:

MAXIMUM TORQUE RECEIVER LOAD CAPABILITIES

Model	Output		Max Load (Z_{SS})
TD-100CM	Direct Output	11.8V, 400 Hz	1Ω
TD-100CMA or TD-101CMB with HPB-14	Transformer	11.8V, 400 Hz	1Ω
		90V, 400 Hz	50Ω
		90V, 60 Hz	100Ω
TD-101CMB With HPB-115	Transformer	90V, 400 Hz	6.5Ω
		90V, 60 Hz	15Ω

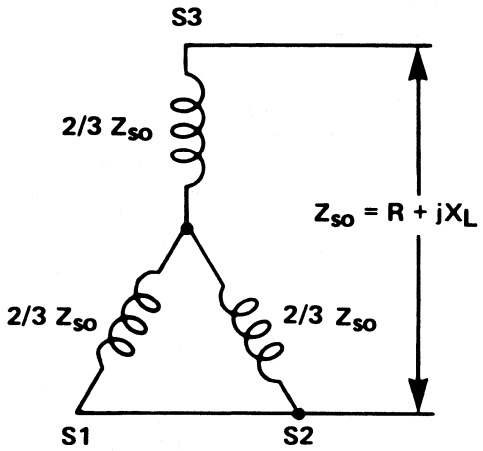
Some common torque receivers and their Z_{SS} (stator input impedance with rotor shorted) are listed in the following table.

SOME COMMON TORQUE RECEIVERS AND THEIR LOAD IMPEDANCES

Synchro	V_{L-L}/freq. (Hz)	Z_{SS}(Ω)
26V – 11TR4c	11.8V/400	3.3 to 4.2
11TR4c	90V/400	180 to 250
15TRx4a	90V/400	50 to 82
15TRx6a	90V/60	920
18TRx4a	90V/400	16 to 21
18TRx6b	90V/60	350 to 430
23TR6	90V/60	110 to 145
23TR6a	90V/60	110 to 145
23TRx4a	90V/400	6.5 to 8.1
23TRx6b	90V/60	110 to 145

DRIVING CT AND CDX LOADS

When driving CT and CDX loads the torque driver must have enough steady state power capability to drive the Z_{so} of the load. Z_{so} (stator impedance with rotor open-circuited) is measured as shown in the diagram:



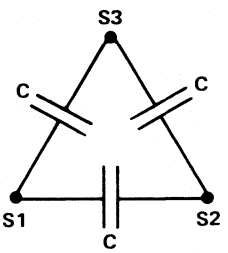
Z_{so} MEASUREMENT

The following table shows the load impedance of some typical control transformers.

SOME COMMON CONTROL TRANSFORMERS AND THEIR LOAD IMPEDANCES

Military Type Number	Size	Z_{so}
26V 08CT4c	08	100 + j490
26V 11CT4d	11	21 + j132
11CT4e	11	838 + j4955
15CT4c	15	1600 + j9300
15CT6b	15	1170 + j6780
18CT4c	18	1670 + j11883
18CT6b	18	1680 + j5040
23CT4a	23	1460 + j11050
23CT6a	23	1250 + j3980

Control transformers are highly inductive loads and it is possible to save power by tuning such loads. Three capacitors may be placed across the legs of the synchro stator in a delta configuration:

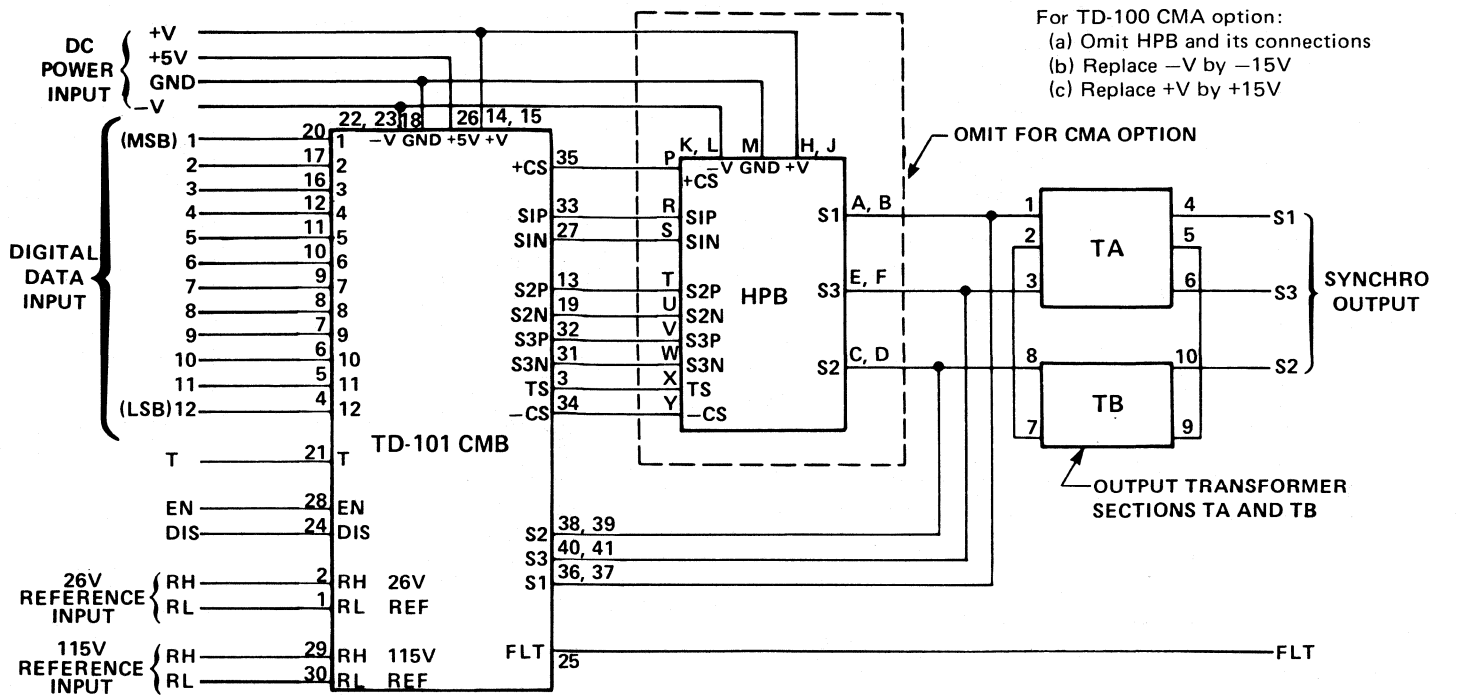


DELTA TUNING CONFIGURATION

INTERCONNECTION DIAGRAM FOR CMA AND CMB OPTIONS

Note:
Connect as shown for TD-101 CMB option.

For TD-100 CMA option:
(a) Omit HPB and its connections
(b) Replace −V by −15V
(c) Replace +V by +15V



The correct value of the capacitance C in Farads is given by:

$$C = \frac{X_L}{4\pi f Z_{SO}} = \frac{X_L}{4\pi f\,(R^2 + X_L{}^2)}$$

where f is the carrier frequency and R and X_L are the real and reactive components of Z_{SO}. Good grade capacitors must be used and they must be able to withstand the full AC output voltage.

When the load has been tuned more loads can be driven in parallel, because the load impedance Z is increased to:

$$Z = \frac{Z_{SO}}{R} = \frac{R^2 + X_L{}^2}{R}$$

FALSE NULL

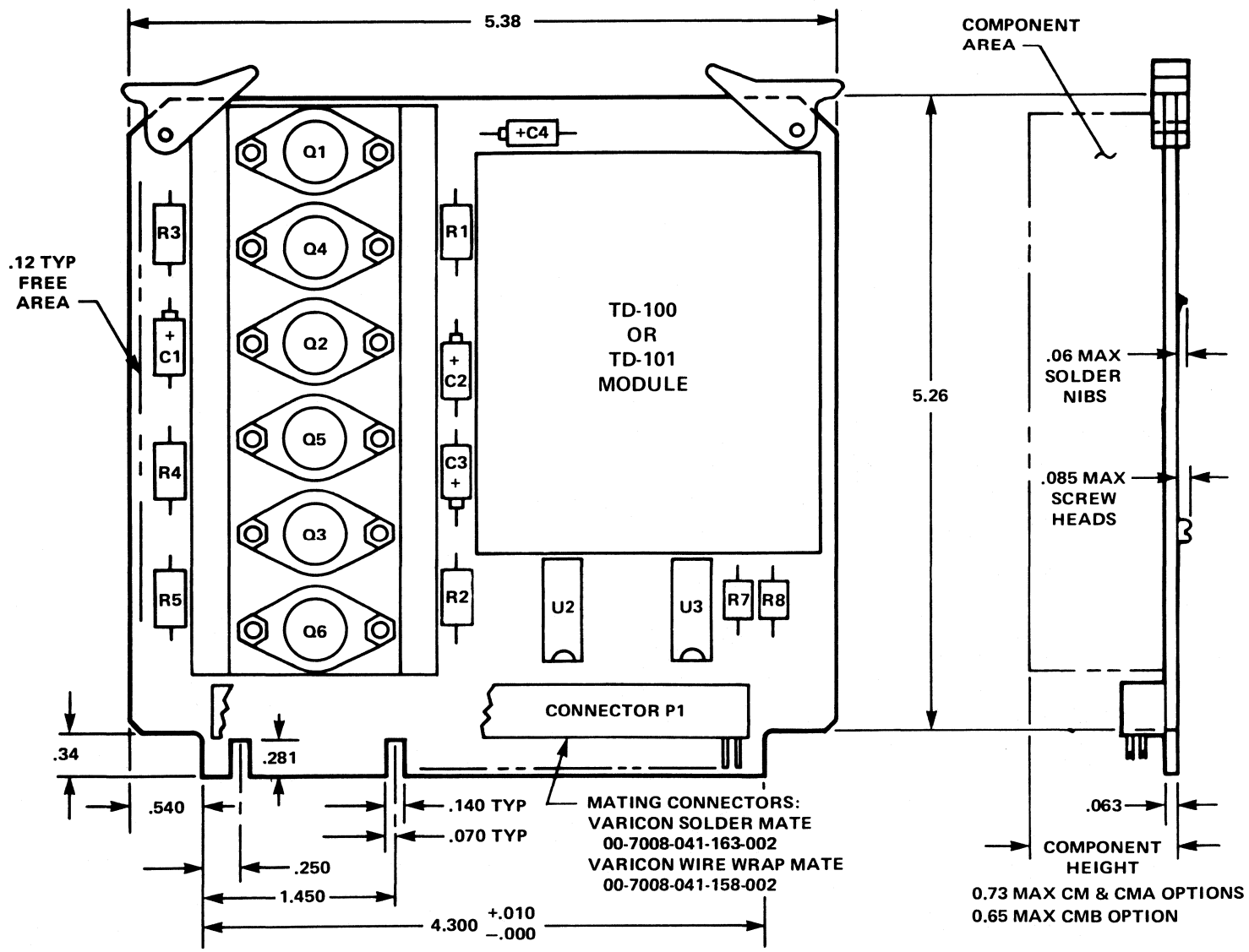
A hang-up condition can occur in a torque receiver or a servo if the rotor is exactly 180° away from the true null. The restoring torque is a sinusoidal function of angle and goes to zero 180° away from the true angle. This is a false null and if there were a finitie error signal the rotor would be driven back toward the true null. The TD-100/101 output angle can change 180° in less than 100 μsec, which is much faster than the electromechanical rotor response. Therefore the digital angle should never be changed 180° in a single step.

TRANSIENTS

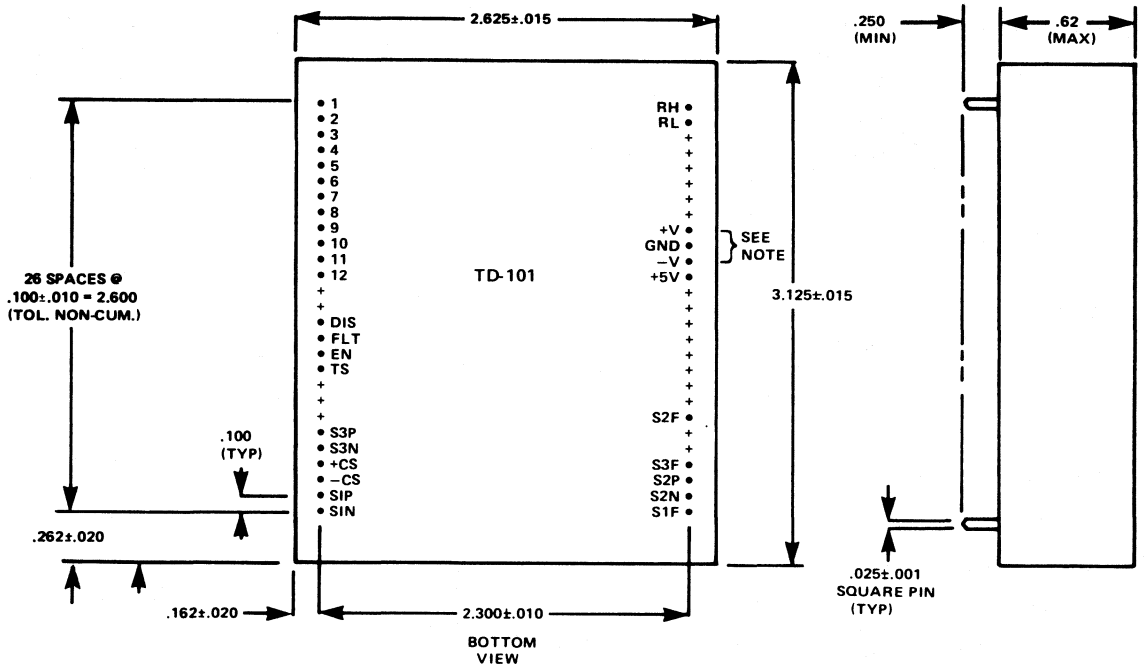
Minor transients occur each time the data angle changes. They last for approximately 100 μsecs and usually do not cause any error, since the bandwidth of the driven servo filters them out.

PC CARD MECHANICAL OUTLINE

The diagram below shows the location of all components as on the CM option.
For option CMA the output resistors R3, R4, R5 are omitted.
For option CMB resistors R1, R2, R3, R4, R5 and the heat sink with Q1 to Q6 are omitted.

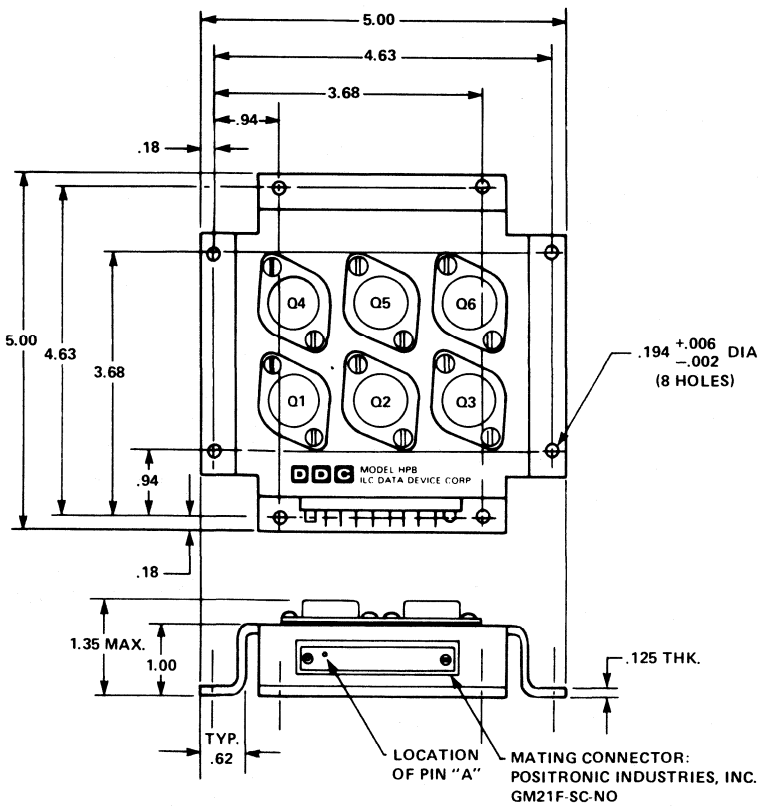


MECHANICAL OUTLINE, TD-100 AND TD-101 MODULES



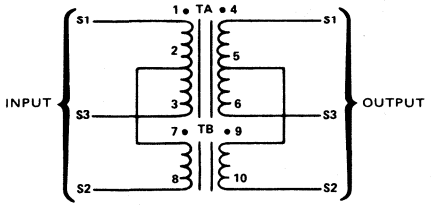
NOTES:
1. The TD-100 module has the same mechanical outline except that pin +V is +15V and pin −V is −15V.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.
3. Pins meet solderability requirements of MIL-STD-202E, Method 208C.

MECHANICAL OUTLINE, HIGH POWER BUFFER, HPB-14 OR HPB-115



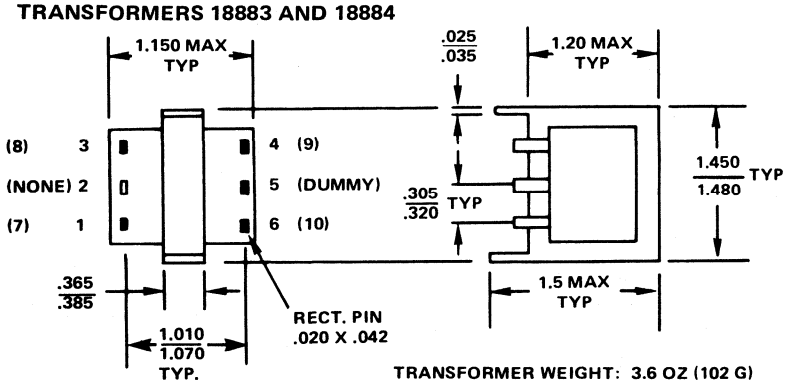
OUTPUT TRANSFORMERS DIAGRAMS

1. Schematic Diagram For all Output Transformers 18883, 18884, 18885, 24748 and 22638



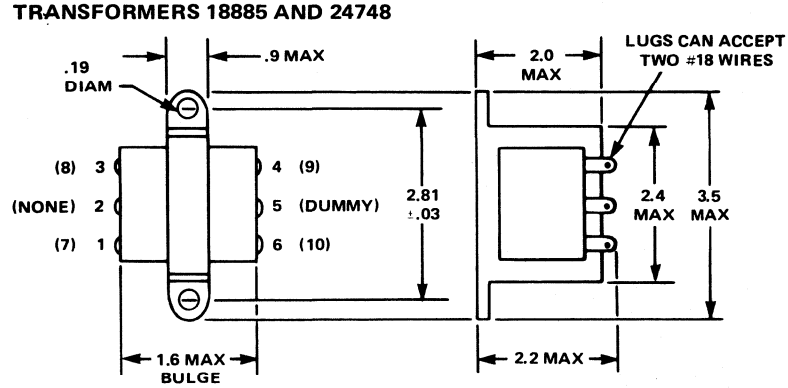
2. Mechanical Outlines
Each output transformer has two sections, TA and TB. Both sections have the same physical dimensions, but pin designations are different. In the following diagrams, pin designations without parenthesis refer to section TA (pins 1 through 6) and pin designations with parenthesis refer to section TB (pins 7 through 10.)

TRANSFORMERS 18883 AND 18884



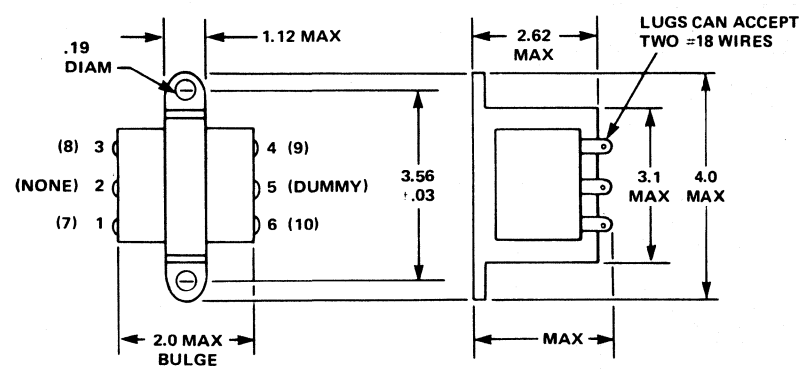
TRANSFORMER WEIGHT: 3.6 OZ (102 G)

TRANSFORMERS 18885 AND 24748



TRANSFORMER WEIGHT: 15.1 OZ (428 G)

TRANSFORMER 22638



TRANSFORMER WEIGHT: 33.2 OZ (942 G)

ORDERING INFORMATION

1. Order the basic torque driver or replacement modules as follows. Transformers and remote high power buffers must be ordered separately as described below in parts 2 and 3. All card mounted units are supplied with a mating connector.

TD – 101CMB – 1

Operating Temperature Ranges (Ambient):
1 = –55°C to +85°C
3 = 0°C to +70°C

Type:
100 = TD-100 replacement module only
101 = TD-101 replacement module only
100CM = Card mounted TD-100 module with card mounted medium power buffer. Includes three 1Ω output resistors. Unit is not intended for output transformers.
100CMA = Card mounted TD-100 module with card mounted medium power buffer. Output resistors are not included. Unit is intended for output transformers, which must be ordered separately below.
101CMB = Card mounted TD-101 module intended for separate remote medium or high power buffer. Order buffer and transformers separately below.

2. The high power buffer for the CMB option must be ordered separately as follows. These buffers are supplied with a mating connector. (See below for output transformers.)

HPB – 14 – 1

Temperature Range (chassis):
1 = –55°C to +85°C
3 = 0°C to +70°C

Output current:
14 = 4 amperes current limiting
115 = 15 amperes current limiting

3. Output transformer pairs for CMA and CMB options must be ordered separately as follows. A pair of transformers is supplied for each part number.

L-L Voltage	Frequency	Part Number	
		CMA or HPB-14	HPB-115
11.8V	360–440 Hz	18883	–
90V	360–440 Hz	18884	24748
90V	57–63 Hz	18885	22638

Reference isolation transformers are also available. Consult factory for information.

SECTION G

SPECIAL FUNCTIONS

PRODUCT SUMMARY TABLE

1. CONTROL TRANSFORMERS (CT) AND CONTROL DIFFERENTIAL TRANSMITTERS (CDX)

Name	Form Factor	Features	Page
HSCDX-14	Two 36 pin DDIP hybrids	Hybrid control differential transmitter; ±4 minute or ±2 minute accurate resolver type output represents the difference between broadband 47-1000 Hz synchro or resolver input angle and 14 bit digital angle.	242

2. SYNCHRO BOOSTER AMPLIFIERS

SBA SERIES	7.4 x 5.1 x 2.1 (60 Hz) 7.4 x 5.1 x 1.3 (400 Hz)	High power synchro output 90V at 60 Hz or 400 Hz. Drives multiple CT or CDX loads up to 25 VA. Very high efficiency, deriving power from reference, reduces heat dissipation by 50%. Protected against short circuits, over loading, transients, temperature and reference supply shut down.	247

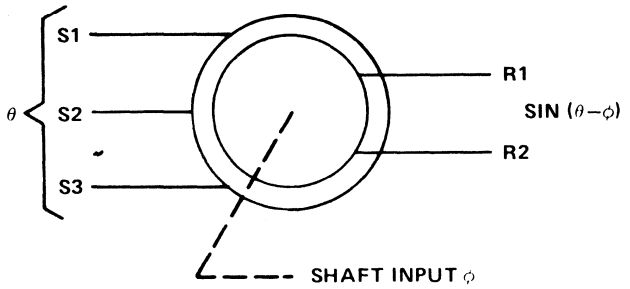
3. INDUCTOSYN TO DIGITAL CONVERTER

DDC-5525/ DDC-4181/ DDC-4182	10.5 x 8.4" P.C. card 4.5 x 3.8" P.C. card 3.5 x 2.5" P.C. card	3 channel position control board compatible with DEC LSI-11 computer. Directly interfaces with Q-BUS. DEC Quad board construction contains complete 3 channel position control. Includes reference source and selectable gain for speed control. Accepts resolver or inductosyn inputs.	253
DDC-35500	12.0 x 6.7" P.C. Card	3-channel resolver or Inductosyn interface card for Multibus® based numerical control systems. 125 rps tracking, turns counting to 255 turns, converter and reference fault flags.	257
IDC-14542 and IDC-14544	36 pin DDIP hybrid	12 or 14 bit Inductosyn to digital converter hybrid, with 100 rps tracking capability (12 bit) and 25 rps (14 bit). Accuracy is +8.5 or +5.3 minutes respectively. Reference input range is from 4 to 50V rms at 360Hz to 22kHz for 12 bit, and 600Hz to 22kHz for 14 bit devices.	261
IDC-35300	3.1 x 2.6 x 0.4" Encap. Module	Low cost inductosyn† or resolver to digital converter. Count, Direction, Major Carry and Velocity outputs standard. Operates at 20 KHz for improved signal to noise ratio.	266
IDC-35303	Encap. Module 3.1 x 2.6 x 0.4	A versatile inductosyn and resolver to digital converter module with 4000 count serial data output, accurate to ±2 counts. Type II servo loop permits continuous tracking up to 150 rps with repeatability of count 1. Direction and Carry outputs are standard.	272

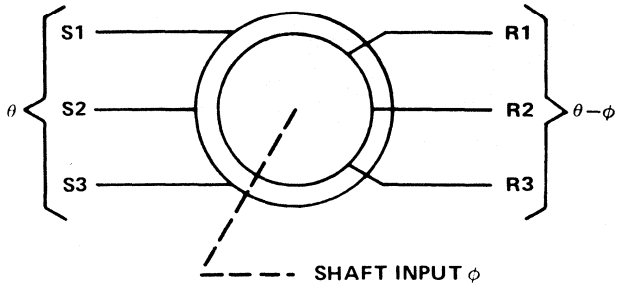
†Trademark Farrand Controls, Inc.

Multibus® is a registered trademark of Intel Corporation.

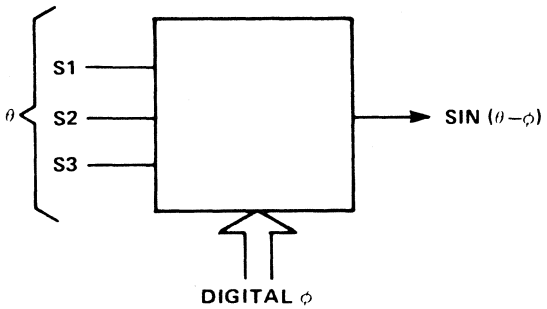
BACKGROUND INFORMATION



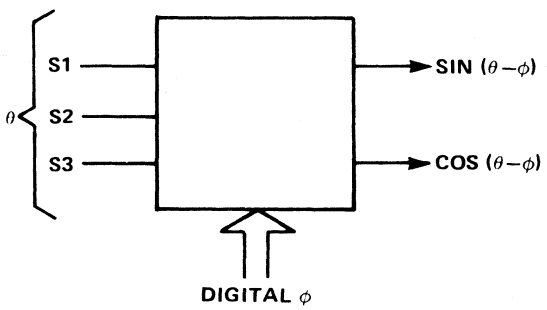
MECHANICAL CT



MECHANICAL CDX



SOLID STATE CT



SOLID STATE CDX

FIGURE 1

INTRODUCTION

This section will explain several special synchro conversion functions and their applications. The functions discussed (Figure 1) will be a solid state control transformer (CT) and a solid state control differential transmitter (CDX).

THEORY OF OPERATION

Solid state CTs and CDXs are the electronic equivalents of their mechanical counterparts, the major difference being that the mechanical shaft is replaced with a digital word (see Figure 1). Thus, the two inputs are a synchro angle here referred to as θ, and a digital input referred to as ϕ. The output from a CT is a voltage derived from the reference whose amplitude is equal to sin $(\theta-\phi)$, while the output from a CDX includes both sin $(\theta-\phi)$ and cos $(\theta-\phi)$ to form a resolver output. Both devices use special multiplying D/As to solve the equation:

$$\sin(\theta-\phi) = \sin\theta\cos\phi - \cos\theta\sin\phi.$$

The CDX also uses a cos control transformer to generate cos $(\theta-\phi)$.

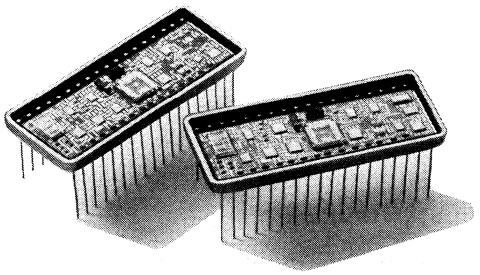
APPLICATIONS

Control transformers are most frequently used as error signal generators in closed loop servos. They are useful whenever digital angles must be subtracted from analog synchro or resolver angles, particularly when offset or correction angles must be provided under computer control.

Control differential transmitters (CDX) subtract digital angles from analog synchro or resolver angles. They are used to provide angle offsets or correction angles when a resolver or synchro type output is required, and are especially adapted to computer controlled systems.

DDC
ILC DATA DEVICE CORPORATION

14 BIT HYBRID CONTROL DIFFERENTIAL TRANSMITTER



DESCRIPTION

The HSCDX-14* series are the smallest solid state control differential transmitters available. They are high reliability units consisting of two 36 pin double DIP packages.

Input isolation transformers are available but will seldom be required because the solid state signal input is true differential with high AC and DC common mode rejection. The AC analog output signals are the sin and cos of the difference between the synchro or resolver angle input and the digital angle input, modulated by the carrier frequency.

The HSCDX-14 is part of Data Device Corporation's second generation of hybrid synchro-digital conversion products, which includes S/D converters, D/S converters, control transformers, and multi-speed converters.

APPLICATIONS

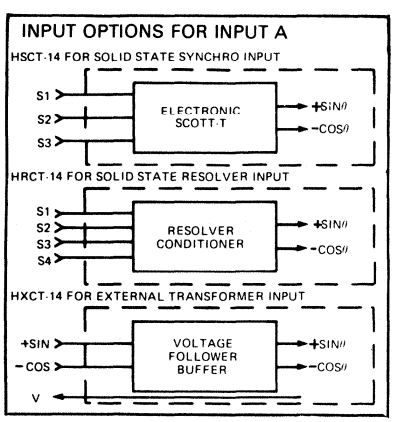
Control differential transmitters (CDX) subtract digital angles from analog synchro or resolver angles. They are used to provide angle offsets or correction angles when a resolver or synchro type output is required, and are especially adapted to computer controlled systems.

Because of their small size and low power requirements, the HSCDX-14 series of control differential transmitters is especially ideal for remotely located and hard to access equipment where high MTBF is critical. They are well suited to the most stringent and severe industrial or military ground and avionics applications. In conjunction with other devices, they are readily adapted for closed loop control. Designed for printed circuit board mounting by standard techniques, the HSCDX-14 can be readily incorporated into other equipment by the OEM user.

FEATURES

- *ACCURACY:*
  ±4 Minutes Normal Accuracy
  ±2 Minutes High Accuracy
- *SIGNAL AND REF. INPUTS:*
  Internal solid state isolation or external isolation transformers
  All common L-L voltage levels and frequencies
- *LOGIC INPUT:*
  TTL and CMOS compatible
  14 bit parallel binary angle
- *POWER REQUIRED:*
  +15V DC and logic voltage supply

*Patented



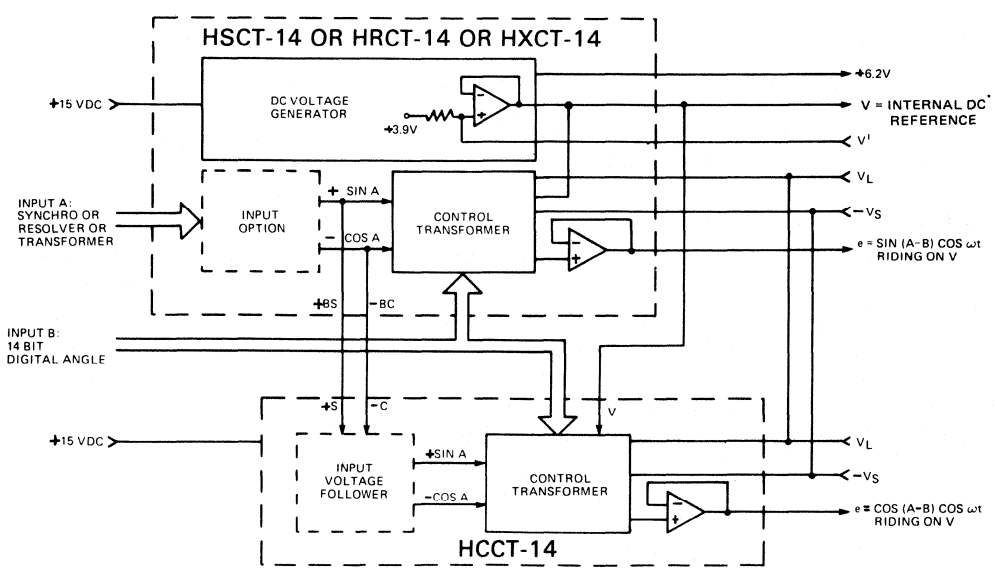


FIGURE 1. BLOCK DIAGRAM

TECHNICAL INFORMATION

1. INTRODUCTION

As shown in the block diagram Figure 1, the HSCDX-14 control differential transmitter consists of two control transformer modules. One module is a complete unit with an input option, DC voltage generator, and a sin output. This module, with synchro, resolver, or transformer input, is called the HSCT-14 series and is described in a separate data sheet. The second HSCDX-14 module is a cos output control transformer and is called the HCCT-14. It relies on the first module for input conditioning and for DC voltage transformation.

The HSCDX-14 has two inputs: an analog synchro or resolver signal, and a 14 bit digital angle. It provides two AC outputs which are the sin and cos respectively of the difference between the synchro or resolver angle A and the digital angle B. The outputs ride on the internal D.C. Reference V and are modulated at the carrier freguency.

Power for the internal CMOS logic in both units must be provided at pins V_L. The user connects pin V_L to the +6.2V internal power supply when the external logic supply voltage is less than 6.2V, and to the external logic supply when the logic voltage is $\geq$6.2V.

Pin $-V_S$ provides the negative power supply voltage for the internal op-amps. This voltage is usually chosen to be either 0 to minimize power consumption, or −7V to optimize the common mode voltage or voltage range of the input option. Pin V′ is used to bring the internal analog ground to normal ground potential when V_L = 6.2V and $-V_S$ = −7V.

As indicated in Figure 1, there are three types of input options: an electronic Scott-T for direct synchro input (HSCDX); a signal conditioner for direct resolver input (HRCDX); and a voltage follower buffer (HXCDX). Depending on the line voltage, there are actually six possible options: two HSCDX, three HRCDX, and one HXCDX. The HXCDX input requires an external signal conditioner such as a synchro or resolver isolation transformer or a solid state buffer.

Interconnection layout is not critical. The analog outputs are derived from op-amps, have low output impedance, and are short circuit proof.

2. POWER SUPPLIES

Two power supplies are required: +15 VDC nominal supply and a logic voltage supply V_L. The +15V supply can vary from +11 to +16.5V with no change in the specifications. The logic supply voltage can range from +4.5V to the voltage of the +15V supply. The logic supply is used in two ways, depending on the nature of the digital logic. When the digital input logic is TTL or DTL, current is drawn from the logic supply by 22K pull-up resistors (see Figure 2). When the logic supply voltage is greater than 6.2V, the logic supply must provide power to drive the internal CMOS logic through pin V_L.

A power supply for $-V_S$, which supplies the negative power supply voltages for the internal op-amps, is optional. $-V_S$ may be any voltage between ground and a negative voltage fifteen volts less than the positive logic supply voltage V_L. For instance, if V_L = 6.2V, $-V_S$ can range from 0V to −8.8V. For minimum power dissipation, $-V_S$ is connected to normal ground, and no connection is made to V′. The internal ground will then be at 3.9V. As $-V_S$ is made more negative, the common mode of the solid state input options HSCT-14 and HRCT-14 increases, the input voltage range of the buffer input option HXCT-14 increases, and the voltage of the internal ground V may be decreased. If V_L = 6.2V and $-V_S$ = −7V, V′ may be grounded so that V is at normal ground potential. The solid state input common mode, the buffer input voltage range, and the power consumed will all be increased as indicated in the specifications table.

While testing or evaluating the HSCDX-14 series, it is advisable to limit the power supply currents. Limit the +15V supply current to 75 mA, and the logic supply current to 5 mA. Power supply transients greater than 18V may damage the module.

SPECIFICATIONS

For listed temperature, power supply, and signal amplitude ranges.

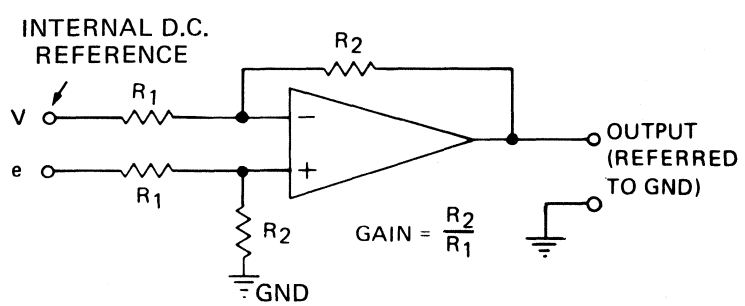
PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY	
Normal Accuracy	±4 minutes max
High Accuracy Option "a"	±2 minutes max
SOLID STATE BUFFER INPUT (HSCDX AND HRCDX UNITS)	
Carrier Frequency Range	47 – 1000 Hz
Synchro and Resolver Input Characteristics	
Voltage Options and Minimum Input Impedance (Balanced)	
Synchro (HSCDX)	Z_{IN} Line to Line / Z_{IN}, Each Line to GND
90V L-L (Option H)	130 KΩ / 85 KΩ
11.8V L-L (Option L)	17.5 KΩ / 11.5 KΩ
Resolver (HRCDX)	Z_{IN} Single Ended / Z_{IN} Differential / Z_{IN}, Each Line to GND
90V L-L (Option H)	175 KΩ / 350 KΩ / 175 KΩ
26V L-L (Option M)	50 KΩ / 100 KΩ / 50 KΩ
11.8V L-L (Option L)	23 KΩ / 46 KΩ / 23 KΩ
Common Mode Range (DC Common Mode Plus Recurrent AC Peak)	$-V_S$ = 0V / V_L = +6.2V and $-V_S$ = −7V
90V L-L (Option H)	150V max / 300V max
26V L-L (Option M)	45V max / 90V max
11.8V L-L (Option L)	20V max / 60V max
VOLTAGE FOLLOWER INPUT (FOR TRANSFORMER UNITS)	
HXCT Input Characteristics	
Carrier Frequency Range	47 – 1000 Hz
Voltage Range	
$-V_S$ = 0V	1V rms nominal; 1.15V max; 0.1V min
V_L = +6.2 and $-V_S$ = −7V	3V rms nominal; 3.5V max; 0.1V min
Max Voltage Without Damage	15V rms continuous
	100V peak transient
Input Impedance	Z_{IN} > 10 MΩ (transient protected voltage follower)
TRANSFORMER CHARACTERISTICS	
400 Hz SIGNAL TRANSFORMER	
Carrier Frequency Range	360 – 1000 Hz
Minimum Input Impedances (Balanced)	Synchro Z_{IN} (Z_{SO}) / Resolver Z_{IN}
90V L-L (Option 4H)	180 KΩ / 100 KΩ
26V L-L (Option 4M)	– / 30 KΩ
11.8V L-L (Option 4L)	20 KΩ / 30 KΩ
Breakdown Voltage to GND	700V peak
60 Hz SIGNAL TRANSFORMER	
Carrier Frequency Range	47 – 440 Hz
Input Voltage Range	10 – 100V rms L-L; 90V rms L-L nominal
Input Impedance	148 KΩ min L-L balanced resistive
Input Common Mode Voltages	±500V rms, transformer isolated
Output Description	Resolver output, +sin (+S) and −cos (−C) derived from op-amps. Short circuit proof.
Output Voltage	1.0V rms nominal riding on DC reference V. Output voltage level tracks input level.
Power Required	4 mA typ, 7 mA max from +15V supply
DIGITAL INPUT	
Logic Type	TTL/DTL/CMOS compatible, depending on logic supply voltage
Coding	Natural binary angle; positive logic
Number of Bits	14
Loading	±1μA max (transient protected CMOS)
ANALOG OUTPUTS	
Outputs e:	
$e = +\sin(A-B)\cos\omega t$ and $e = +\cos(A-B)\cos\omega t$	A = Synchro or resolver input angle; B = digital input angle; ω = signal carrier frequency
Scale Factor Error	±2% max (absolute error, not a function of angle)
Scale Factor Variation With Digital Angle B	±0.25% max
Maximum Output	1V rms (operates over full ±180° range of (A-B))
DC Offset	±25 mV max (varies smoothly as function of digital angle B)

PARAMETER	VALUE
ANALOG OUTPUTS (Cont'd)	
Internal D.C. Reference V	
Voltage	3.9 VDC nominal when $-V_S = 0$. Can be set to zero for suitable $-V_S$ voltage levels.
Current Capability	±1 mA
Bias Voltage	
Voltage	6.2VDC
Current Capability	±0.1 mA
Buffered +Sin A and −Cos A (+BS and −BC)	
Voltage Level	1V rms nominal
Current Capability	±1 mA
DYNAMIC CHARACTERISTICS	
Input Rate	Maximum conversion rate limited only by rate at which digital input changes
Settling Time	
For Normal Tracking	No lag error
For 179° step change	10μs to final value
TEMPERATURE RANGE	
Operating	
−1 Option	−55°C to +125°C
−3 Option	0°C to 70°C
Storage	−55°C to +135°C

POWER SUPPLIES			
Voltage	+15 VDC	Logic Supply	$-V_S$ (Optional)
Voltage Limits	+11V to +16.5V	+4.5V to +15 supply voltage	0 to (V_L − 15V)
Max Voltage Without Damage	+18V	+18V	−(18V-V_L)
Current or Impedance	+50 mA* max	Z_{IN} = 5 KΩ min	−50 mA* max

*Does not include current required by 60 Hz active transformer.

PARAMETER	VALUE
PHYSICAL CHARACTERISTICS	
Converter Modules (Two)	
Type	36 pin double DIP
Size	0.78 x 1.9 x 0.21 inch (2.0 x 4.8 x 0.53 cm)
Weight	1 oz max (28 g)
400 Hz Transformer Modules	
Type	Encapsulated module. Signal input uses 2 modules (T1A and T2B). Ref uses 1 module (T2).
Size	0.8 x 0.6 x 0.3 inch (2 x 1.5 x 0.8 cm)
Weight	0.4 oz max (11 g)
60 Hz Transformer Modules	
Type	Encapsulated module. Signal transformer and reference transformer each consist of one such module.
Size	1.125 x 1.125 x 0.42 inch (2.86 x 2.86 x 1.07 cm)
Weight	0.7 oz max (20 g)



CIRCUIT FOR REFERENCING OUTPUT TO NORMAL GROUND

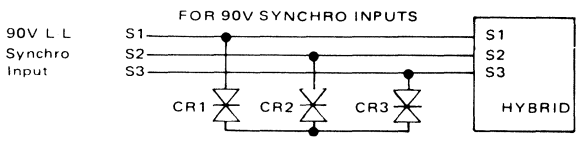
3. SYNCHRO AND RESOLVER INPUT (ANGLE A)

Solid State Buffer Input (HSCDX and HRCDX):

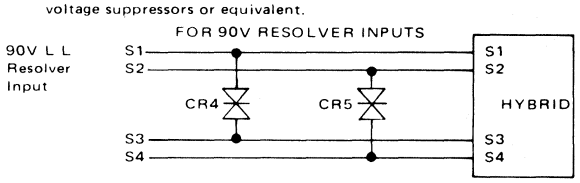
The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection, so that separate isolation transformers will seldom be required. Input impedance is maintained with power off. The common mode voltage range (recurrent AC peak + DC common mode voltage) depends on $-V_S$ and should not exceed the following values:

INPUT	COMMON MODE IF $-V_S = 0$	MAXIMUM IF $-V_S = -7V$	MAX TRANSIENT PEAK VOLTAGE
90V L-L	150V Peak	300V Peak	350V
26V L-L	45V Peak	90V Peak	150V
11.8V L-L	20V Peak	60V Peak	150V

90V line-to-line systems generally have voltage transients which exceed the 350V specification listed above. These transients can destroy the thin film input resistor network in the hybrid. Therefore, 90V L-L solid state input modules should always be protected by installing voltage suppressors as shown below.



CR1, CR2 and CR3 are 1N6130, 100V bi polarity transient voltage suppressors or equivalent.



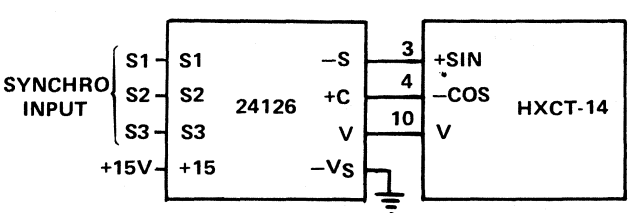
CR 4 and CR5 are 1N6137, 200V bi-polarity transient voltage suppressors or equivalent.

CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

Voltage Follower Buffer Input:

HXCDX units require a signal isolation transformer, a Scott-T, or a similar signal conditioner. They may be preferred in applications where the signal conditioner can be integrated with other components, as in many multiplexed systems. The HXCDX-14 input is high impedance and compatible with any device providing resolver type signals of appropriate amplitude riding on internal analog ground V. The maximum input voltage amplitude depends on $-V_S$ and will be greater if the magnitude of $-V_S$ is increased, as discussed in the Power Supplies section.

The 60 Hz signal transformer 24126 is an active device with op-amp outputs, and requires connection to the +15V power supply as shown below. An active transformer is provided because a passive transformer would be much larger at 60 Hz than at 400 Hz.



4. DIGITAL INPUT ANGLE B

The logic 0 level is from 0 to .3V_L and the logic 1 level from .7V_L to V_L. For TTL/DTL logic, V_L is 6.2V (see Figure 2), so 22K pull-up resistors to +5V should be added by the user to each digital input line.

5. OUTPUTS SIN (A-B) AND COS (A-B)

The outputs e are AC voltages sin (A-B) cos ωt, and cos (A-B) cos ωt, at the carrier frequency. The amplitude of e is 0.38 mV per LSB of angle difference A-B, where 1 LSB = .02197 degrees = 1.318 minutes. The maximum output amplitude reached is 1 volt rms nominal, which represents an angular difference of ±90°. The phase of the modulation cos ωt indicates whether the angle difference A-B is positive or negative. The maximum loading is 1 mA rms.

The outputs e ride on V, the D.C. Reference. When $-V_S$ is grounded, V = + 3.9V nominal. A difference circuit as shown, may be used to reference e with respect to normal ground instead of V, and also to provide gain.

6. DYNAMIC CHARACTERISTICS

The HSCDX-14 differential control transmitter is essentially a fast logic circuit. During normal tracking, when the synchro or resolver update information is continuously available and the digital input is updated in LSB steps, there is no lag error in the output, and it is continuously available. If an instantaneous 179° step occurs in either input, the settling time to within final accuracy is 10μs.

RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

All HSCDX-14 hybrids are built in accordance with requirements of MIL-STD-883 and are screened as shown in our Processing Flow Chart. This screening is based on the requirements of Method 5008 except for burn in, which is optional. To specify pre-burn in tests and burn in, add 883B to the part number. The computed MTBF value for MIL-STD-883B processing (including burn in) is 610,000 hours, Ground Fixed, at 25°C.

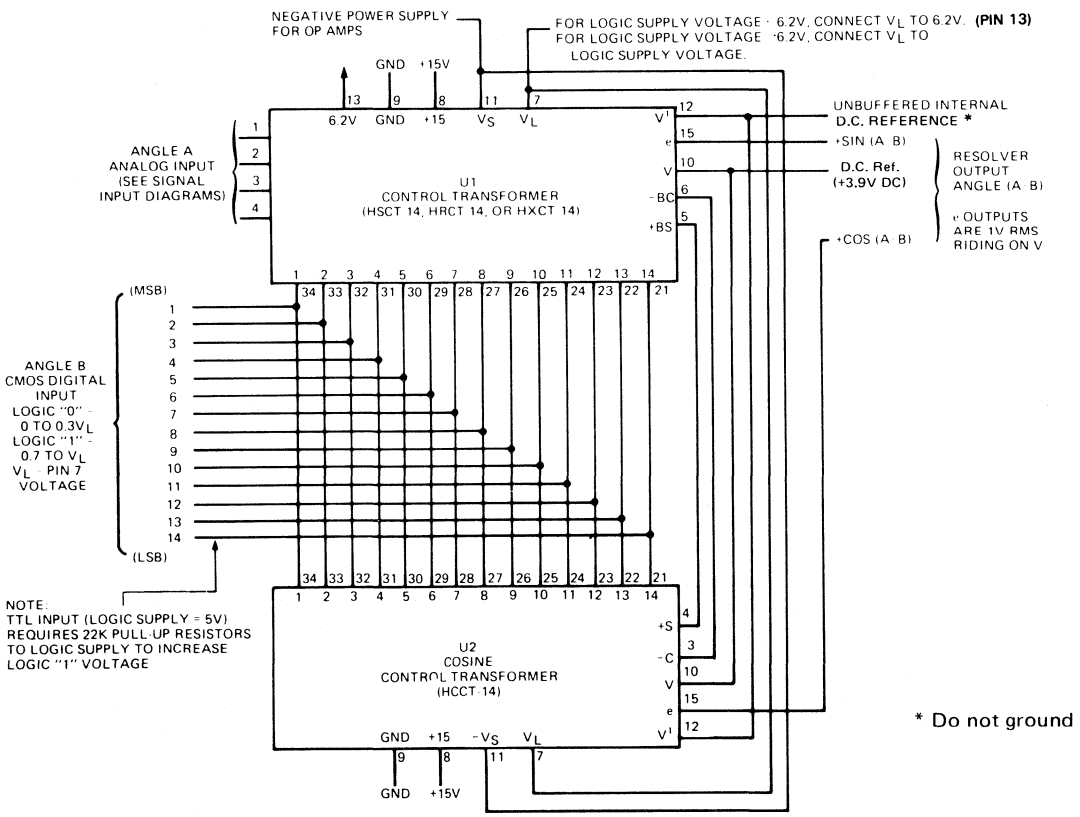
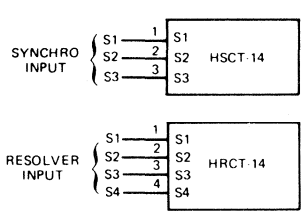
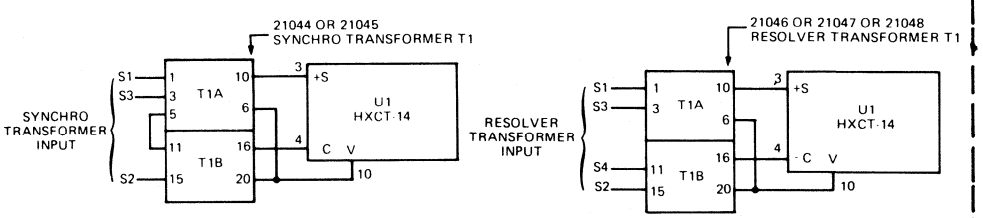


FIGURE 2. INTERCONNECT DIAGRAM

INPUT SIGNAL DIAGRAMS FOR SOLID STATE BUFFER UNITS

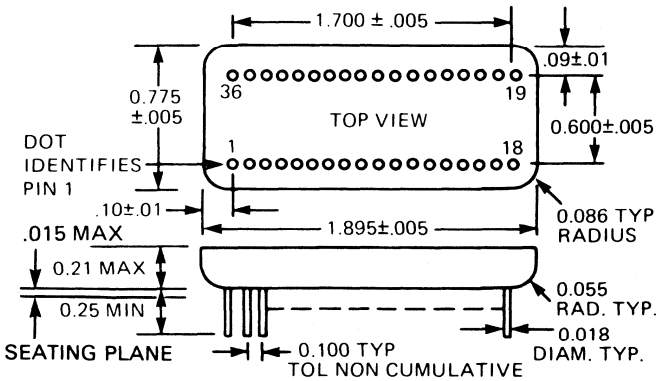


INPUT SIGNAL DIAGRAMS FOR VOLTAGE FOLLOWER BUFFER UNITS WITH TRANSFORMERS



CONTROL TRANSFORMER MODULE DIAGRAMS

1. Mechanical Outline (HSCT, HRCT, HXCT, and HCCT)
   36 pin double DIP



PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING
PINS ARE KOVAR WITH GOLD PLATING: (50 μ INCH MIN).
CASE IS ELECTRICALLY FLOATING

2. Pin Assignments

PIN	FUNCTION HSCT	HRCT	HXCT	HCCT	PIN	FUNCTION
1	S1	S1	N.C.	N.C.	19	TP 3
2	S2	S2	N.C.	N.C.	20	TP 1
3	S3	S3	+SIN	−C	21	BIT 14 LSB
4	S4	N.C.	−COS	+S	22	BIT 13
5	+BS	+BS	+BS	−BC (TP)	23	BIT 12
6	−BC	−BC	−BC	+BS (TP)	24	BIT 11
7	V_L				25	BIT 10
8	+15V				26	BIT 9
9	GND				27	BIT 8
10	V (Internal D.C. Ref.)				28	BIT 7
11	$-V_S$				29	BIT 6
12	V′				30	BIT 5
13	6.2V	6.2V	6.2V	N.C.	31	BIT 4
14	TP 4				32	BIT 3
15	e				33	BIT 2
16	TP 5				34	BIT 1 MSB
17	NC				35	TP6
18	TP2				36	TP7

Note: Test Points TP are for Factory Use Only

Note:

Mechanical outlines and schematic diagrams for all signal transformers (400 Hz, 21044 to 21048 and 60 Hz, 24126) can be found with HSDC-14 product information.

ORDERING INFORMATION

The HSCDX differential control transmitters consist of two control transformer modules:

A sin output with choice of synchro, resolver, or voltage follower buffer input (HSCT, HRCT, or HXCT).

A cos output without choice of input (HCCT).

If signal isolation transformers are required for HXCDX units, they must be ordered separately from part 2 below.

1. Order a differential control transmitter consisting of two hybrid modules as follows:

HSCDX−14−H−1−a−883B

- 883B: MIL-STD-883 Processing
  - 883B = Conforms to MIL-STD-883 DDC procedures
  - Blank = Same, except pre burn in test and burn in are omitted.
- a: Accuracy
  - Blank = ±4 minutes
  - a = ±2 minutes
- 1: Temperature Range (Operating)
  - 1 = −55°C to +125°C
  - 3 = 0°C to +70°C
- H: Voltage Levels
  1. Synchro solid state input (HSCDX)
     - H = 90V L-L
     - L = 11.8V L-L
  2. Resolver solid state input (HRCDX)
     - H = 90V L-L
     - M = 26V L-L
     - L = 11.8V L-L
  3. Voltage follower input (HXCDX)
     - Omit voltage level specification.
     - One HXCDX model accepts all normal voltage levels.
- 14: Resolution = 14 Bits
- HSCDX: Input Type
  - HSCDX = Solid state synchro
  - HRCDX = Solid state resolver
  - HXCDX = Voltage follower buffer. Requires external signal conditioner such as an isolation transformer.

2. 400 Hz and 60 Hz transformers may be ordered by part number (P/N) as follows.

Type	Frequency	Ref. Voltage	L-L Voltage	Part Numbers Ref. Xfmr.	Signal Xfmr.
Synchro	400 Hz	115V	90V	21049	21045*
Synchro	400 Hz	26V	11.8V	21049	21044*
Resolver	400 Hz	115V	90V	21049	21048*
Resolver	400 Hz	26V	26V	21049	21047*
Resolver	400 Hz	26V	11.8V	21049	21046*
Synchro	60 Hz	115V	90V	24133-1† -3†	24126-1† -3†

* The part number for each 400 Hz synchro or resolver isolation transformer includes two separate modules as shown in the line drawings.

†-1 and -3 indicates operating temperature ranges available.

3. Order each sin or cos control transformer module as follows. Part 1 of the ordering information describes the alternatives in each portion of the part number.

HSCT−14−H−1−a−883B

- 883B: MIL-STD-883 Processing
  - Omit or 883B
- a: Accuracy
  - Omit or a
- 1: Temperature Range (Operating)
  - 1 or 3
- H: Voltage Level
  - H, M, or L
  - Omit for HXCT and HCCT
- 14: Resolution 14 bits
- HSCT: Type
  - HSCT = Control transformer with solid state synchro input
  - HRCT = Control transformer with solid state resolver input
  - HXCT = Control transformer with voltage follower buffer input
  - HCCT = Cosine control transformer

HIGH POWER SYNCHRO BOOSTER AMPLIFIERS
Also Boosts Output of D/S & D/R Converters

DESCRIPTION

The SBA-Series amplifiers are compact units designed to be bolted to a chassis (see mechanical outline). Both 60 and 400HZ units require signal input levels of 90V synchro or 6.81V resolver. Their signal output is high power 90V L-L synchro. A connection to the signal reference voltage provides the power to drive the amplifier. The only other connections are for logic controls: a Disable input, a BIT output, and +5V power supply to drive the logic. All signal inputs and outputs are transformer isolated from each other, and logic inputs and outputs are opto-isolated.

The SBA is a high efficiency device. Because power is derived from the reference rather than DC supplies, heat dissipation is reduced by 50% and the unit is smaller in size. Another energy saving feature is the Disable, which allows the output to be turned off when it is not required. The SBA components are mounted on a 1/8 inch thick aluminum plate which conducts heat efficiently to the chassis to which the unit is bolted.

The SBA is fully protected. Current limiting prevents damage from overloads and short circuits. Voltage clamps protect against reference and load transients. A thermal cutout disables the output at 125° C.

In addition to retaining the high efficiency and protection features of previous DDC torque drivers, the SBA has a new feature: a kick circuit. When the rotor in a torque receiver is hung up, the automatic kick circuit in the SBA will shift the synchro output by 120° for 1/2 second to free the hang-up.

APPLICATIONS

SBA amplifiers are rugged units, requiring no calibrations or adjustments, that can be used wherever high power synchro output is required. They can drive large passive loads such as multiple CTs and CDXs, or active loads such as torque receivers. The SBA can be used to amplify the output of a synchro transmitter directly, but its most common useage is for D/S conversion. Only two modules are required for high power D/S conversion: a standard, low power hybrid or discrete D/S or D/R converter, and the SBA.

High power synchro drive capability is often required in training simulators, remote indicators, gun fire control, and Navy retransmission systems. The power conserving features and compactness of the SBA amplifiers recomment them especially for installations requiring multiple units, and the DISABLE and BIT logic are designed for computer supervision.

FEATURES

- *MOST COMPACT, EASY TO USE SYSTEM FOR HIGH POWER SYNCHRO OUTPUT*
  - *ONLY ONE MODULE NEEDED TO BOOST SYNCHRO SIGNALS.*
  - *POWERED FROM REFERENCE ±15V POWER SUPPLIES NOT REQUIRED.*
  - *PROVIDES HIGH POWER D/C CONVERSION WHEN USED WITH LOW POWER D/S OR D/R CONVERTER.*
- *90V, 60 OR 400 Hz SYNCHRO OUTPUTS:*
  - *DRIVES MULTIPLE CT AND CDX LOADS UP TO 25VA.*
  - *DRIVES TORQUE RECEIVER LOADS UP TO Zss = 6Ω.*
- *KICK CIRCUIT FREES TORQUE RECEIVER ROTOR TO PREVENT HANGUPS.*
- *VERY HIGH EFFICIENCY:*
  - *DERIVING POWER FROM REFERENCE REDUCES HEAT DISSIPATION BY 50%.*
- *VIRTUALLY INDESTRUCTIBLE:*
  - *PROTECTED AGAINST SHORT CIRCUITS, OVERLOADING, TRANSIENTS, TEMPERATURE, AND REFERENCE SUPPLY SHUT DOWN.*

SPECIFICATIONS

Apply over temperature range, ± 10% reference voltage and frequency variation, and ± 10% harmonic distortion in the reference.

PARAMETER	VALUE
ACCURACY	
Passive Loads (CT and CDX)	±3.0 arc-minutes
Active Loads (torque receiver)	± 10 arc-minutes
SIGNAL INPUT	
Input Isolation	Transformer Isolation, 500V rms min. breakdown to ground
Synchro Input	Frequency / L-L Voltage / Impedance
SBA-25001	400 Hz ± 10% / 90V / 400 KΩ min, balanced
SBA-25003	60 Hz ± 5% / 90V / 100 KΩ min, balanced
Resolver Input	
SBA-25002	400 Hz ± 10% / 6.81V / 4 KΩ min, balanced
SBA-25004	60 Hz ± 5% / 6.81V / 4 KΩ min, balanced
	Other frequencies line-to-line voltages and output power levels are available. Please consult factory.
SYNCHRO OUTPUT	
L-L Voltage for Nominal Input Voltage	90V ±1%
Minimum Load Impedance of Passive Loads	Z_{so} = 243Ω
Minimum Load Impedance of Active Loads	Z_{ss} = 6Ω
CONTROL LINES	
Disable (DIS)	TTL compatible Logic 0 enables power amplifier output if internal temperature does not exceed 125°C Loading is 2.5mA max. at logic 0 Opto-isolated, 1000V peak min. breakdown to ground.
Overload Indicator (BIT)	TTL compatible Logic 1 indicates that normal output is not being provided for either of two reasons: 1. A thermal overload prevents the disable from turning the output on. 2. A current overload condition exists and output is reduced by internal current limiting Drive capability is 2 Std. TTL loads Opto-isolated, 1000V peak min. breakdown to ground.
Kick Circuit (K and CO)	Jumper connection in mating connector. Normally connected for torque receiver loads (not for passive CT and CDX loads). Shifts output by 120° for 1/2 sec. to unjam rotor if output is hung up by an overcurrent condition. Repeat every 4-1/2 seconds so long as overcurrent condition persists. Cannot cause damage to SBA or to torque receiver.
POWER SUPPLIES	
Reference Input (Must Be Same As Signal Reference)	
Reference Signal Isolation	Transformer isolated, 500V rms min. breakdown to ground.
Frequency:	400 Hz / 60 Hz
Nominal Value	400 Hz / 60 Hz
Range	360-440 Hz / 57-63 Hz
Voltage:	
Nominal Value	115V rms
Range	± 10%
Max. Value Without Damage	130V rms
Current:	
No-load	50 mA max / 100 mA max
Additional With Load	1 mA per mA of output load
Logic Voltage Supply (+5V)	
Voltage Level	+ 5V DC ±10%
Max. Voltage Without Damage	+ 10V
Current	10 mA max.
THERMAL CHARACTERISTICS	
Temperature Ranges: (Case Temperature)	
Operating	−25°C to +85°C
Storage	55°C to +125°C
Heat to be Dissipated	1.5 Watts max. per VA delivered
Thermal Resistance at Junction of Power Transistor to Heat Sink	1.5°C/Watt, conduction cooling
Thermal Cutoff	Amplifier output is disabled whenever internal temperature exceeds 125°C.
PHYSICAL CHARACTERISTICS	400 Hz / 60 Hz
Size (Bolts to Chassis)	7.4 X 5.1 X 1.8 inches (188 X 130 X 46 mm) / 7.4 X 5.1 X 2.6 inches (188 X 130 X 66 mm)
Weight	4 lb (1.82 Kg) max / 7 lb (3.1 Kg) max

TECHNICAL INFORMATION

Figure 1 shows that the SBA consists of three main parts: a power amplifier with a transformer isolated signal input, an internal power supply which is transformer isolated from the reference power source, and digital controls with opto-isolation.

SIGNAL INPUT

90V L-L synchro input passes through an isolation transformer. 6.81V L-L resolver input passes through a Scott-T transformer which changes it to S1, S2, S3, synchro format as well as providing signal isolation. If frequencies or voltage levels, other than those specified are required, please consult the factory.

POWER AMPLIFIER

The triple power amplifier accepts synchro input and produces high power, 90V L-L synchro output. The output is current limited with a sharp limit transition at 1.0A peak. The current limiting prevents damage from output overloads or short circuits, and voltage clamping prevents damage from load transients.

If the reference input is lost, the amplifier output shuts down. In a shut down condition, the SBA presents a safe, open circuit configuration to the load.

The amplifier is thermally protected by a cutout which disables the output when the internal temperature reaches 125°C. The output is automatically restored when the temperature drops below 125°C.

The kick circuit in the amplifier is described in a separate section.

POWER SUPPLY

The high efficiency, low heat dissipation characteristics of the SBA are made possible by the pulsating power supply. This supply produces two unfiltered, full-wave rectified positive and negative voltages as shown in the diagram. These voltages are always in phase with the amplifier output voltage because the power is derived from the reference input. The amplitude of the two voltages need only be a few volts greater than the power amplifier output voltage, since both will change together if the reference level changes. As indicated in Figure 2, the positive and negative pulsating power supply voltage levels will be consistently lower than the constant DC levels of any DC supplies. Because the voltage levels are lower, the power consumed will be much less. The power dissipated as heat is equal to the amplifier current times the difference in voltage between the power supply and the output. For the SBA, the power dissipated is reduced by approximately 50% for reactive loads.

DIGITAL CONTROLS

Two logic lines emerge from the power amplifier, one indicating whether a current overload condition exists (current overload indicator) and one indicating when the internal temperature exceeds 125°C (thermal overload indicator). Logic 1 signifies overload. The Overload Indicator (BIT) will be at logic 1 when either or both of the indicator lines are at logic 1. To prevent nuisance signals in the BIT, the current overload logic line has a 4 second delay before responding to an actual overload condition.

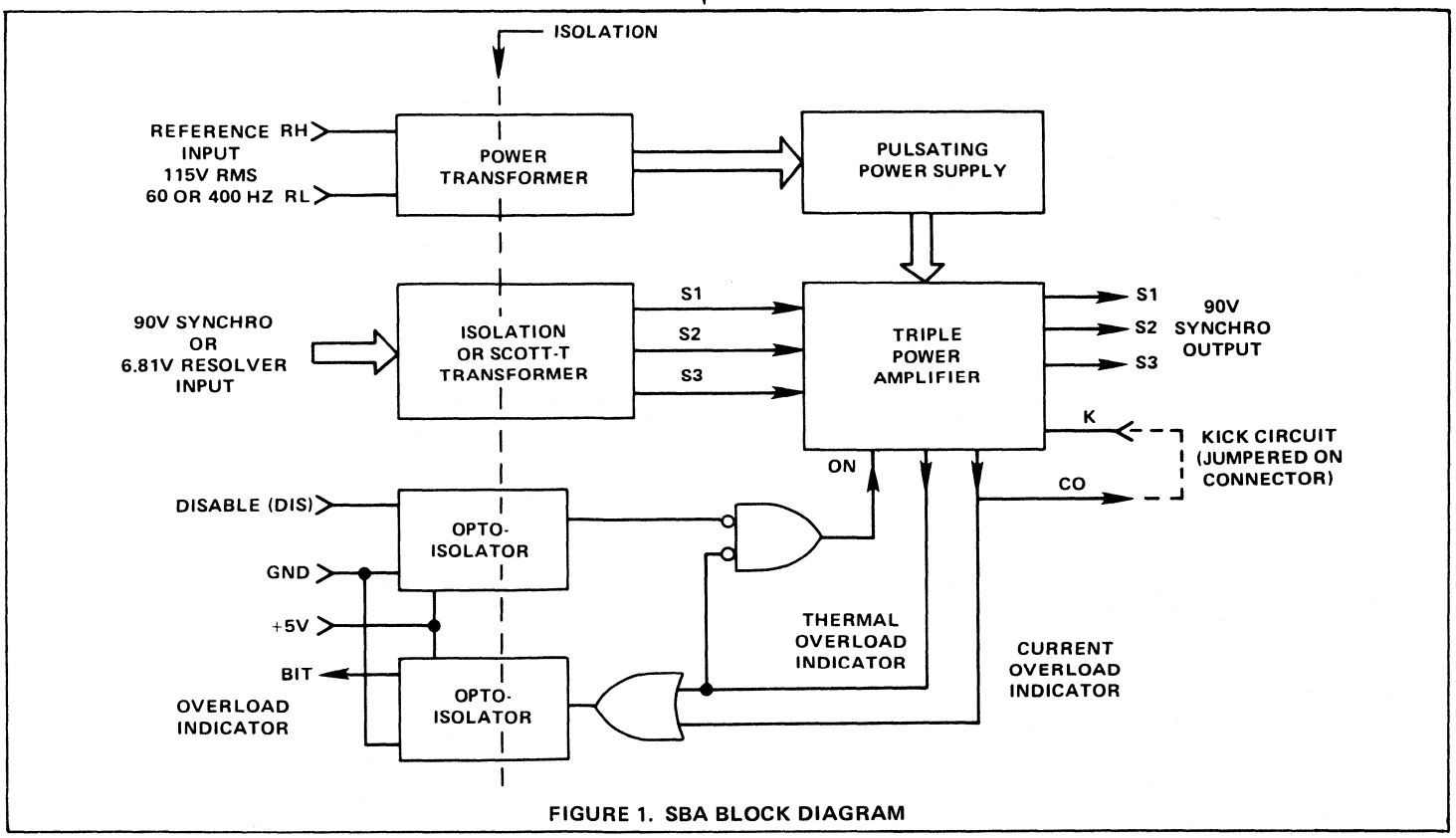


FIGURE 1. SBA BLOCK DIAGRAM

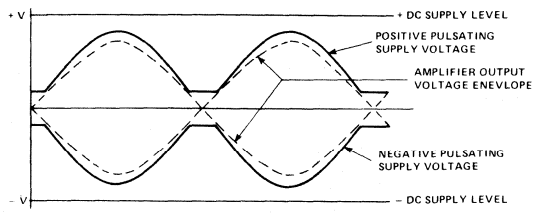


FIGURE 2. PULSATING POWER SUPPLY VOLTAGE WAVEFORMS

The Disable (DIS) makes it possible to switch the power amplifier output on or off. The reference input current drain, as indicated in the specifications, is much smaller if the output is off. If several SBA amplifiers are connected to the same reference, their disable lines can be used to sequence the SBA turn on. This reduces the transient reference power requirement because torque receivers generally draw the maximum limiting current at turn on when the rotors are off null.

The Disable can turn the output on only if two conditions are satisfied. One condition, indicated by the AND gate in the block diagram, is that no thermal overload exists (temperature above 125°C). The other condition is that the reference input must be supplied, since the output shuts down if the amplifier loses power.

KICK CIRCUIT

A hang-up condition can occur in a torque receiver in which the rotor is not driven back to null but stalls at some other angle. The function of the kick circuit in the SBA is to free the hang-up so that the rotor can return to null.

The kick circuit frees rotor hang-ups by shifting the synchro output angle by 120° for a period of 1/2 second. As shown in the block diagram, the kick circuit is activated by connecting the kick input K to the current overload indicator logic line CO. Because the driving current supplied by the SBA is limited to 1 ampere, a current overload condition will usually exist except around null. Such current overloading, if it persists longer than the 4 second delay in the CO response time, will drive the CO line to logic 1, and activate the kick circuit.

Usually one kick is enough to free a rotor hang-up. However, the kick circuit will repeat its 1/2 second, 120° angle shift every 4.5 seconds so long as the current overload condition persists. Repeated cycling cannot harm the torque receiver or the SBA.

The output currents in the SBA are limited to 1A. Without the kick circuit, larger drive currents would be required to reduce the probability of rotor hang-ups. A kick circuit is therefore an important asset in reducing the size and cost of a torque driver.

The kick circuit pin K should be left unconnected for passive loads such as CTs and CDXs.

DRIVING CT AND CDX LOADS

When driving CT and CDX loads the SBA must have enough steady state power capability to drive the Z_{so} of the load. Z_{so} (stator impedance with rotor open-circuited) is measured as shown in the Figure 3:

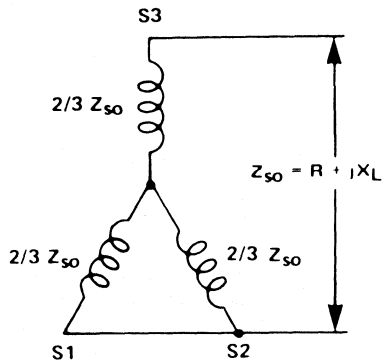


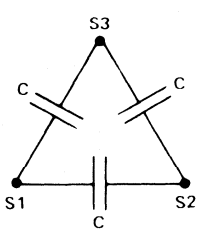
FIGURE 3. Z_{so} MEASUREMENT

The SBA can drive CT and CDX loads whose Z_{so} has a magnitude $(R^2 + X_L^2)^{1/2}$ which is at least as great as the minimum load impedance of $Z_{so} = 243\Omega$ listed in the specifications table. The following table shows the load impedance of some typical control transformers and control differential transmitters.

SOME COMMON CT AND CDX LOAD IMPEDANCES

Military Type Number	Size	Z_{so} (Nominal)
CONTROL TRANSFORMERS:		
11CT4e	11	838 + j4955
15CT4c	15	1600 + j9300
15CT6b	15	1170 + j6780
18CT4c	18	1420 + j13260
18CT6b	18	1680 + j5040
23CT4a	23	1460 + j11050
23CT6a	23	1250 + j3980
CONTROL DIFFERENTIAL TRANSMITTERS:		
11CDX4b	11	253 + j1802
15CDX4d	15	140 + j1000
15CDX6c	15	404 + j2290
18CDX4c	18	63 + j 695
18CDX6d	18	521 + j1605
23CDX4c	23	32 + j 306
23CDX6c	23	221 + j 958

Control transformers are highly inductive loads and it is possible to save power by tuning such loads. Figure 4 illustrates three capacitors placed across the legs of the synchro stator in a delta configuration:



DELTA TUNING CONFIGURATION

FIGURE 4. CT LOAD TUNING

The correct value of the capacitance C in Farads is given by:

$$C = \frac{X_L}{4\pi f\,(R^2 + X_L^2)}$$

where f is the carrier frequency and R and X are the series real and reactive components of Z_{so}. Good grade capacitors must be used and they must be able to withstand the full AC output voltage.

When the load has been tuned more loads can be driven in parallel, because the load impedance Z is increased to:

$$Z = \frac{R^2 + X_L^2}{R}$$

DRIVING TORQUE RECEIVER LOADS

In addition to having enough steady state power capability to maintain a torque receiver at null, a torque driver must have a peak transient power sufficient to drive the torque receiver back to null. This transient power capability is indicated by the maximum torque receiver load capability Z_{ss} which can be driven. For the SBA, the maximum load Z_{ss} is 6Ω.

Some common torque receivers and their load impedances Z_{ss} (stator input impedance with rotor shorted) are listed in the following table:

SOME COMMON TORQUE RECEIVERS AND THEIR LOAD IMPEDANCES

Synchro	V_{L-L}/freq. (Hz)	Z_{ss}(Ω)
11TR4c	90V/400	180 to 250
15TRx4a	90V/400	50 to 82
15TRx6a	90V/60	920
18TRx4a	90V/400	16 to 21
18TRx6b	90V/60	350 to 430
23TR6	90V/60	110 to 145
23TR6a	90V/60	110 to 145
23TRx4a	90V/400	6.5 to 8.1
23TRx6b	90V/60	110 to 145

The SBA-25002 and 25004 Synchro Booster Amplifiers are directly compatible with our MDCR-H or HDSC-14 Digital to Resolver/Synchro Converters. Figure 5 illustrates the connection procedure for this application.

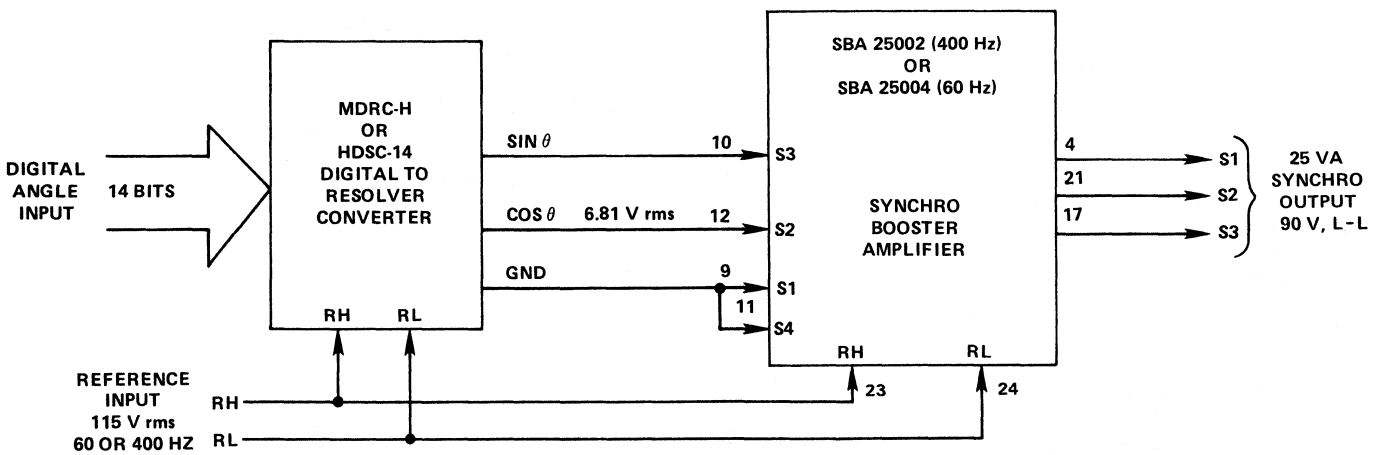
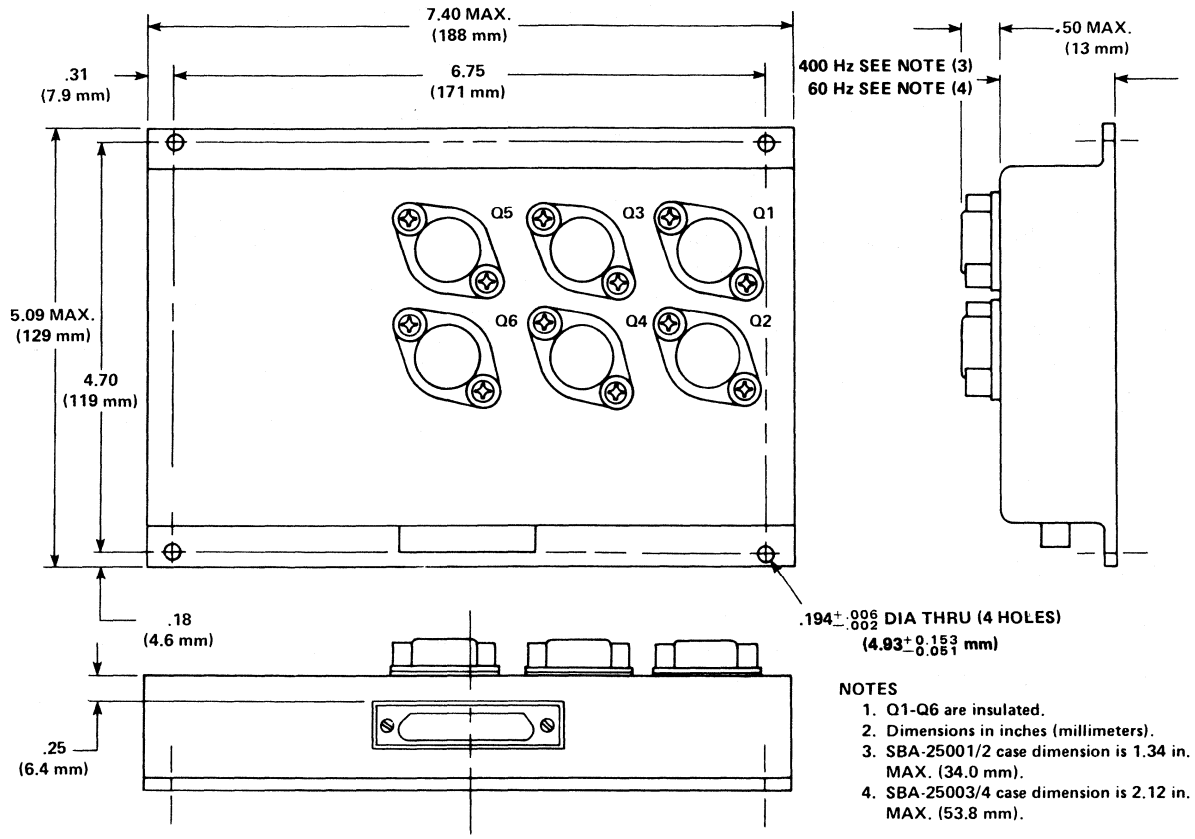


FIGURE 5. MDRC/SBA CONNECTION DIAGRAM

MECHANICAL OUTLINE

Metal case bolts to chassis for heat-sinking.
Mating connector and locking hardware supplied.



NOTES
1. Q1-Q6 are insulated.
2. Dimensions in inches (millimeters).
3. SBA-25001/2 case dimension is 1.34 in. MAX. (34.0 mm).
4. SBA-25003/4 case dimension is 2.12 in. MAX. (53.8 mm).

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	+5V	14	DIS INPUT
2	BIT OUTPUT	15	NC
3	NC	16	GND
4	S1 OUT	17	S3 OUT
5	TP	18	CO
6	K	19	NC
7	TP	20	TP
8	TP	21	S2 OUT
9	S1 IN	22	NC
10	S3 IN	23	RH
11	S4 IN	24	RL
12	S2 IN	25	NC
13	TP		

NOTES:
1. Pin S4 is for resolver input versions only.
2. To enable the kick circuit for torque receivers, connect pin 6 to pin 18.
3. NC means no connection is made to this pin internally.
4. TP are test points intended for factory use only.

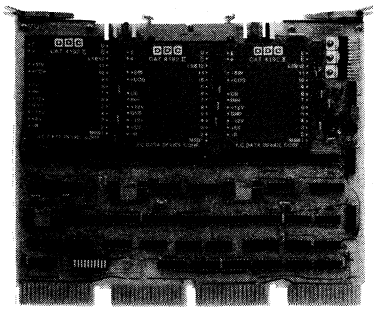
ORDERING INFORMATION

SBA-25001
- 1 = 400 Hz, 90V L-L synchro input
- 2 = 400 Hz, 6.81V L-L resolver input
- 3 = 60 Hz, 90V L-L synchro input
- 4 = 60 Hz, 6.81V L-L resolver input

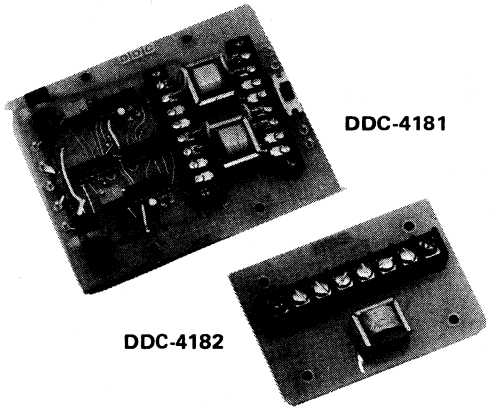
All units provide 25VA synchro output

NOTE: The following hardware is supplied with each order:
Mating Connector AMP 205207-1
One set Male Retainer Screws AMP 205980-1
15 Sockets AMP 205090-1

(3) CHANNEL RESOLVER/INDUCTOSYN INTERFACE
Sub-System for LSI-11 Based NC Systems



DDC-5525



DDC-4181

DDC-4182

FEATURES

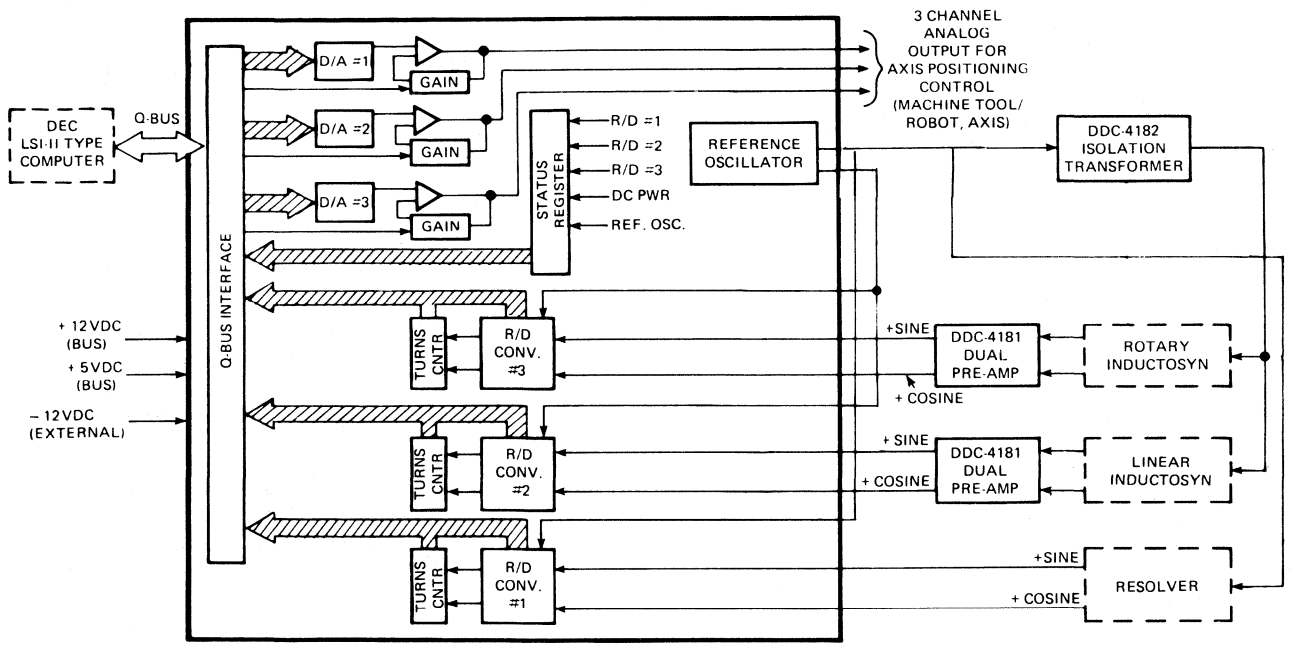
- *DEC LSI-11 Compatible*
  *Directly interfaces with Q-Bus**
- *DEC Quad board construction*
  Inserts directly into a single thickness main frame slot
- *Complete 3 Channel control*
  3 independent channels of resolver or inductosyn conversion with 3 independent channels of 12 Bit D/A conversion for axis servo motor control
- *Servo motor control*
  Selectable gains for slew or fine speed control of servo control motors
- *Resolver/Inductosyn compatible*
  Can be used directly with resolvers or inductosyns (with inductosyn buffer accessories DDC-4181 and 4182)

DESCRIPTION

The DDC-5525 is a Q-BUS compatible printed circuit card which enables a DEC LSI-11 type computer to directly interface with three (3) independent channels of Resolver to Digital conversion to obtain positional information, as well as three (3) independent channels of Digital to Analog conversion for a resulting closed system Servo Axis monitoring/positioning control sub-system. The R/D converters can interface with resolvers and/or inductosyns as transducer inputs. Transducer excitation (10KHz) is also provided on the printed circuit card.

The DDC-5525 is a Quad size, DEC style printed circuit card sub-system. It is addressed via the Q-BUS interface as 4 Read cells (R/D #1, 2, 3 and status register) and 3 Write cells (D/A #1, 2, 3).

Optional accessories: DDC-4181 (Dual Preamplifier) and DDC-4182 (Isolation Transformer), are available for inductosyn applications to facilitate scale impedance matching and slider signal buffering.



NOTE:

DDC-4182	Isolation Transformer is used for linear inductosyn scales of 3m or less and/or rotary inductosyns.
DDC-4181	Dual preamplifier is used for linear inductosyn scales of 3.3m to 9m and/or rotary inductosyns. DDC-4181 has the capability (via internal jumpers) to match variable inductosyn output voltages to the input levels required by the DDC-5525 R/D converters.
General:	Figure 1 is a functional block diagram showing a typical application of the Converter; Dual Pre-Amplifier and Isolation Transformer

*Q-BUS is a registered trademark of Digital Equipment Corporation (DEC)

FIGURE 1. DDC-5525 FUNCTIONAL BLOCK DIAGRAM

PERFORMANCE SPECIFICATIONS

PARAMETER	VALUE
R/D CONVERSION	
Resolution	12 Bits (4096 counts) equiv. to: 0.088 degrees (resolver) 0.4883 microns (Inductosyn—2mm pitch)
Accuracy	±2 LSB's equiv. to: ±0.178 degrees (resolver) ±0.9766 microns (Inductosyn-2mm pitch)
Tracking velocity (full accuracy)	15m per minute equiv. to: 512,000 counts per sec (125 revolutions/sec or pitch cycles/sec)
Tracking acceleration (full accuracy)	100mm per sec/sec (205,000 counts per sec/sec)
4 Bit turns counter	Maintains number of full revolution or pitch transitions, to provide absolute position. Combined with the 12 bits of data from R/D converter to obtain a 16 bit word to the Q-Bus, representing axis position.
D/A CONVERSION & SERVO DRIVER AMPLIFIER	
Resolution	12 Bits (13th used for gain selection)
Input coding	2's complement (sign & magnitude)
Servo Amplifier	Selectable: G1 = 0.5mv per LSB (12th BIT) G2 = ±10V maximum**
Gain	
Drive	5.0 ma maximum
Accuracy	D/A + Servo Amplifier
Gain	±2LSB's Gain error maximum
Offset	±2LSB's DC Offset error maximum (Trim adjustments available for system gain & offset trim)
Reference	Internal precision D/A reference generator
REFERENCE OSCILLATOR (FOR RESOLVERS/INDUCTOSYNS)	
Frequency	10KHz
Output Type	Short Circuitproof
Output Voltage	4.4V for 0.454 Transformation Ratio (Resolvers)
For resolvers	

PARAMETER	VALUE
For Resolvers	12V for 0.165 Transformation Ratio Resolvers
For Inductosyns	4.4V, 6V, 10.4V, 12V (DDC-5525) 0.6V, 2V, 4V (DDC-5525 with DDC-4182)
Output Phase	Dual: (0° & 90° phase shift)
0° Phase Shift	For resolver applications
90° Phase Shift	For inductosyn applications 0° & 90° reference outputs are used to excite the external resolvers and/or inductosyns as well as providing input reference signals to the R/D converters
Output Drive	
Resolver use	capable of providing 100 ma rms max.
Inductsoyn use	capable of providing 100 ma rms max.

STATUS REGISTER

Provides individual and/or master fault status
- Individual R/D converter faults
- Reference oscillator/DC power fault
- Master fault (any fault)

COMPUTER INTERFACE

Directly compatible with DEC Q-Bus
- 4 read cells (R/D #1, #2, #3 and status register)
- 3 write cells (D/A #1, #2, #3)

Base Address
- Selectable via printed circuit card mounted dip switches

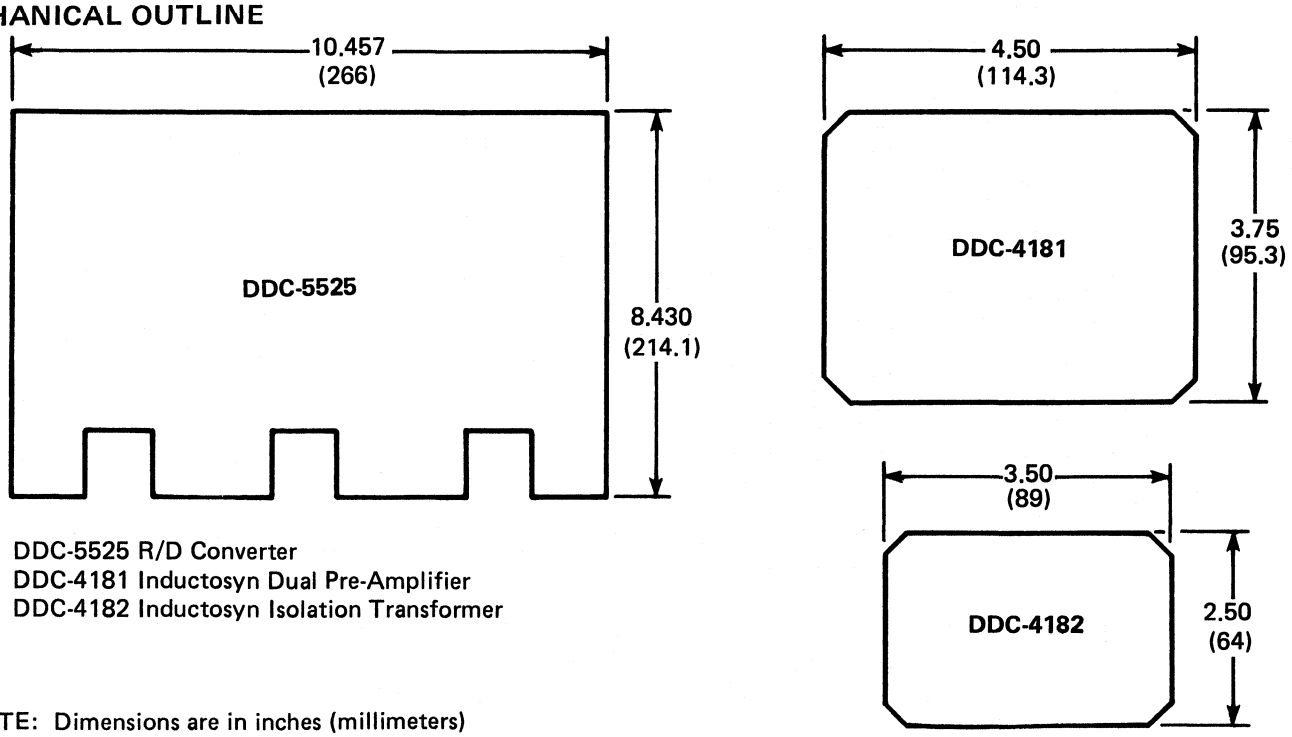
Bus and Analog connections
- All bus connections are made by inserting the DDC-5525 Sub-system into the computer main frame.
- All analog input and output connections and −12V power supply connections are made via a 40 pin I/O connector located at the opposite edge from the digital bus connections.

POWER SUPPLY REQUIREMENTS

	(+12VDC) BUS	(−12VDC) EXTERNAL	(+5VDC) BUS
DDC-5525 (3 chan R/D card)	400ma	600ma	1850ma
DDC-4181 (Dual Pre-amp)	N/A	15ma	15ma
DDC-4182 (Isolation Transformer)	N/A	N/A	N/A

**Linearity maintained on G2 up to ±7.5V.

MECHANICAL OUTLINE



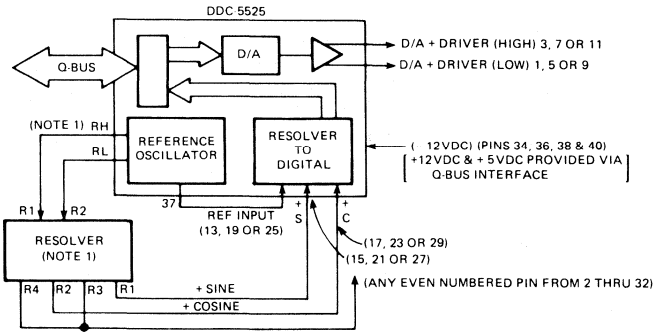
DDC-5525 R/D Converter
DDC-4181 Inductosyn Dual Pre-Amplifier
DDC-4182 Inductosyn Isolation Transformer

NOTE: Dimensions are in inches (millimeters)

SCOPE

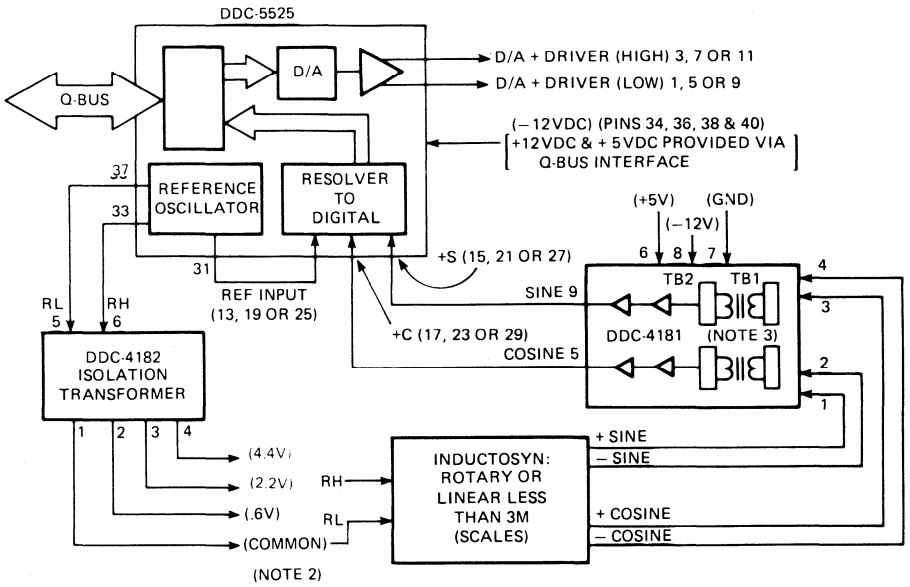
The DDC-5525 is a Q-Bus compatible three channel, Resolver or Inductosyn to Digital Converter with three channels of digital to analog conversion, for use in closed servo system applications.

These applications are separated into the basic categories of resolver to digital and/or inductosyn to digital conversion. These categories will be explained as separate applications, but both resolvers and/or inductosyns may be connected to the same converter card.



NOTE: 1a) For Resolvers with 26 VRMS reference & 11.8 VRMS Line/Line outputs (0.454 transformation ratio)
RH = Ground (any even numbered pin from 2 thru 32)
RL = Pin 37 (−4.4R)
b) For Resolvers with (0.165 transformation ratio)
RH = Pin 33 (+6R)
RL = Pin 35 (−6R)

FIGURE 2. RESOLVER APPLICATION (1 of 3 channels shown)



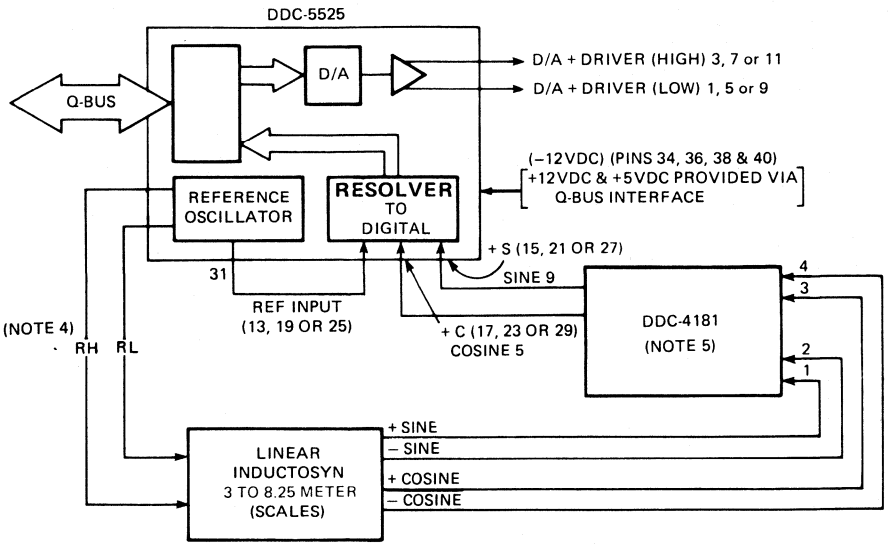
NOTE 2:
The following table shows the various connections required from the output of the DDC-4182 to the inductosyn being used, dependent upon type and length:

Inductosyn Scale Length	Inductosyn Type	Inductosyn RH to 4182 Pin
3 meters	linear	4 (4.4V)
1.5 meters	linear	3 (2.2V)
1.25 meters or less	linear	3 (2.2V) & RL TO 2(0.6V)
Rotary Inductosyn	rotary	2 (0.6V)

NOTE 3:
The DDC-4181 Dual Pre-Amplifier has the capability of interfacing with numerous inductosyns and scale lengths. Dependent upon different scale lengths, the output voltage from the Inductosyn will vary. Internal to the DDC-4181 are terminal boards which can be jumpers selected for different input voltages. These jumpers are set as follows:

Input Voltage to DDC-4181	TB1-4 to TB1-	TB1-8 to TB1-	TB2-4 to TB2-	TB2-8 to TB2-
1.7 to 2.3mv	1	5	3	7
2.1 to 2.8 mv	2	6	3	7
2.6 to 3.4 mv	3	7	3	7
3.1 to 4.1 mv	1	5	2	6
3.8 to 5.0 mv	2	6	2	6
4.6 to 6.2 mv	3	7	2	6
5.6 to 7.5 mv	1	5	1	5
6.8 to 9.2 mv	2	6	1	5
8.3 to 11.4 mv	3	7	1	5

FIGURE 3. INDUCTOSYN APPLICATIONS: LESS THAN 3 METERS (1 of 3 channels shown)



NOTE 4:
Different Inductosyn lengths reguire different reference connections to the DDC-5525 Reference Oscillator Output. These are summarized in the table below:

(RH) DDC-5525 Pin	(RL) DDC-5525 Pin	Scale Length	Oscillator Voltage
33 (+6R)	35 (–6R)	8.25M	12V
33 (+6R)	37 (–4.4R)	7M	10.4V
33 (+6R)	GND*	4M	6V
37 (–4.4R)	GND*	3M	4.4V

*GND are even numbered pins from pin 2 thru pin 32.

NOTE 5:
The DDC-4181 Dual Pre-Amplifier has the capability of interfacing with numerous inductosyns and scale lengths. Dependent upon different scale lengths, the output voltage from the Inductosyn will vary. Internal to the DDC-4181 are terminal boards which can be jumpers selected for different input voltages. These jumpers are set as follows:

Input Voltage to DDC-4181	TB1-4 to TB1-	TB1-8 to TB1-	TB2-4 to TB2-	TB2-8 to TB2-
1.7 to 2.3mv	1	5	3	7
2.1 to 2.8 mv	2	6	3	7
2.6 to 3.4 mv	3	7	3	7
3.1 to 4.1 mv	1	5	2	6
3.8 to 5.0 mv	2	6	2	6
4.6 to 6.2 mv	3	7	2	6
5.6 to 7.5 mv	1	5	1	5
6.8 to 9.2 mv	2	6	1	5
8.3 to 11.4 mv	3	7	1	5

FIGURE 4. DDC-5525—INDUCTOSYN APPLICATIONS: 3 METERS TO 8.25 METERS
(1 of 3 channels shown)

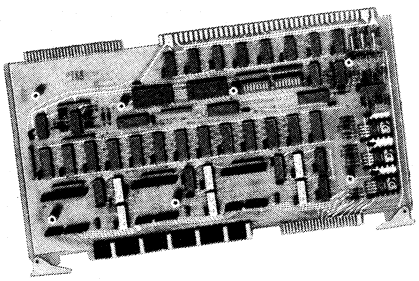
ORDERING INFORMATION

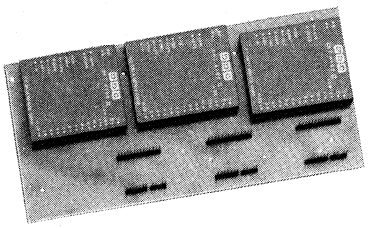
ORDER DDC-5525

NOTES: 1. DDC-4181 Dual Preamplifier and DDC-4182 Isolation Transformer may be ordered as optional accessories.
2. DDC-5525-1 (2 channel version = same card with one channel deleted).

3 CHANNEL RESOLVER/INDUCTOSYN™ INTERFACE

Subsystem For Multibus® Based NC Systems





DESCRIPTION

The DDC-35500 is an Intel Multibus compatible printed circuit card, which is mechanically and electrically compatible with Intel Specification 9800683-04 and interfaces to a standard Multibus chassis with three independent channels of resolver or inductosyn to digital conversion. The board gives position and turns count data, which is formatted into three 8-bit bytes per channel and transferred in accordance with standard Multibus interface control signals. Logic is provided to perform channel selection functions as well as handshaking between the computer and the DDC-35500 (Figure 1).

Address programming is accomplished with card mounted DIP switches. The upper 16 address lines are used to select the device (card) on the bus. The lower four address lines (ADR 3-ADR 0) are used to select the channel's position data read registers (3 per channel), its read/write control registers and its device status read registers. The status (BITE) word indicates to the host processor the presence of a fault condition in any of the R/D or I/D conversion channels or the reference oscillator. A 10 kHz onboard reference oscillator and a power amplifier are supplied for reference excitation.

Optional Accessories. Dual Preamplifier (DDC-4181) and Isolation Transformer (DDC-4182) are available for inductosyn applications. These devices respectively perform slider buffering and scale impedance matching functions. In addition, an RFI/EMI shielded Nema 12 enclosure (DDC-35500-605) which contains one each of the DDC-4181 and DDC-4182 is also available.

FEATURES

- *MULTIBUS COMPATIBLE*
- *OPERATES WITH INDUCTOSYN OR RESOLVER TRANSDUCER JUMPER SELECTABLE*
- *TURNS COUNTING TO 255 TURNS*
- *125 RPS TRACKING SPEED*
- *ONBOARD 10 KHz REFERENCE OSCILLATOR FOR TRANSDUCER EXCITATION*
- *INDIVIDUAL CONVERTER REFERENCE OSCILLATOR AND MASTER FAULT FLAGS*
- *OPTIONAL BUFFER ACCESSORIES FOR INDUCTOSYN APPLICATIONS*

Note: Inductosyn™ is a trademark of Farrand Controls Corporation.
Multibus® is a registered trademark of Intel Corporation

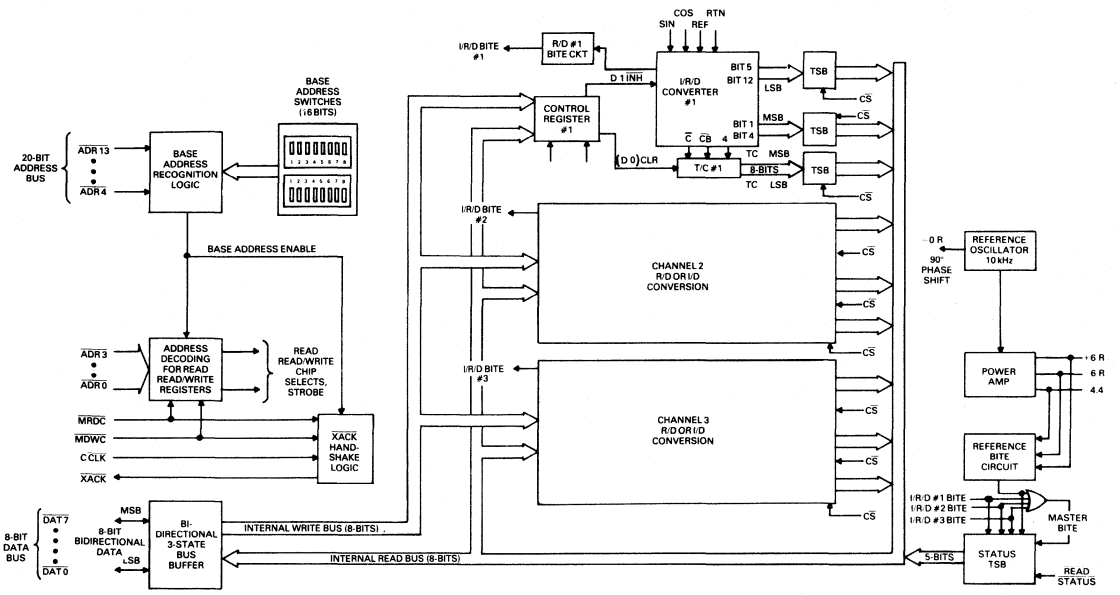


FIGURE 1. DDC-35500 BLOCK DIAGRAM

SPECIFICATIONS			
PARAMETER	**VALUE**		
NUMBER OF CHANNELS	3, Jumper selectable for resolver or inductosyn inputs		
R/D CONVERSION			
Design Specification	For Intel "Multibus" system		
Resolution	12-bits (4096 counts)		
Resolver	0.088 degrees		
Inductosyn	0.4883 microns (2mm pitch)		
Accuracy	±2 LSB's ±0.176 degrees (resolver) ±0.9766 microns (inductosyn–2mm pitch)		
Turns Counting	Up to ±255 turns with "clear zeroing" capability		
Dynamic Characteristics			
Tracking Rate	15m per minute 512,000 counts per sec (125 rps or pitch cycles/sec)		
Acceleration	100mm per sec/sec (205,000 counts per sec/sec)		
REFERENCE OSCILLATOR			
Frequency	10 kHz		
Output Short Circuit Duration	Continuous		
Maximum Load	100 mA		
Phase Shift	0° for resolver, 90° leading for inductosyn applications, pin programmable		
Output Voltages	4.4, 6, 10.4, 12 (all VAC)		
SIGNAL INPUTS			
Resolver/Inductosyn	Each channel individually selectable by pin programming		
Programmable Jumpers			
Resolver	E1 to E3 (CH1) E4 to E6 (CH2) E7 to E9 (CH3)		
Inductosyn	E1 to E2 (CH1) E4 to E5 (CH2) E7 to E8 (CH3)		
MULTIBUS INTERFACE	See Pin Assignment Table (P1)		
POWER SUPPLIES			
Voltage Levels	+5 VDC	+12 VDC	−12 VDC
Current	1200mA max	400mA max	600mA max
Jumper Connections			
Chassis Inputs	E16 to E18	E10 to E12	E13 to E15
External Inputs*	E16 to E17	E10 to E11	E13 to E14
TEMPERATURE RANGE			
Operating Range	0 to 70°C		
PHYSICAL CHARACTERISTICS			
Configuration	Double card slot (Intel Multibus standard)		
Size	12.0 x 6.75 x 1 inch (30.5 x 17.2 x 2.5 cm)		

*Via test points

TECHNICAL INFORMATION

Each channel of the DDC-35500 consists of a resolver/inductosyn to digital converter and an 8-bit turns counter. The onboard 10 kHz reference oscillator is common to all channels as an input to each converter and excitation to their respective transducers. The converter reference inputs are each pin programmable for "in-phase" resolver reference (Figure 2) or 90° phase shift for inductosyn applications (Figure 3).

A status register output (5-bits) is provided to indicate failure in any of the converters or the reference oscillator. In addition, a "Master Fault" indication which flags the presence of one or more fault conditions is provided as the MSB of the status word.

The DDC-35500 presents the Intel Multibus Interface with three bytes per channel of position information. Two bytes from the selected converter channel are position data. The first byte consists of bits 5 through 12 (LSB) and the second byte contains bits 1 through 4 of the converter output. The third byte contains the 8-bit word corresponding to the turns count of the channel. The counters will count up to 255 revolutions or pitches in either direction.

The 20-bit address provided by the Multibus interface is divided into two functional parts. The upper 16-bits are used for device selection. The lower 4 bits are used for selection of the read and read/write registers of the appropriate channel. A circuit to provide the $\overline{\text{XACK}}$ handshake signal is also included, with provisions for pin-programming the delay time (200 to 900 ns) between the $\overline{\text{MRDC}}$ or $\overline{\text{MWTC}}$ and $\overline{\text{XACK}}$ signals.

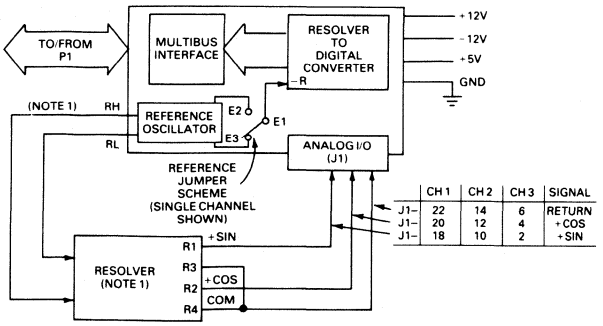
A control (read/write) register is also provided for each channel. The functions of converter INHIBIT and turns counter CLEAR are performed by setting the appropriate bits of these signals.

INDUCTOSYN APPLICATIONS

The DDC-35500 is capable of operating with a wide range of Inductosyn configurations when coupled with two versatile DDC interfacing accessories, DDC-4181 and DDC-4182. The DDC-4181 is a dual preamplifier, which is programmable via user selected jumper terminals that provide the required 2V rms signal input to J1 of the DDC-35500. The Inductosyn Connection Table defines the connection scheme for these applications.

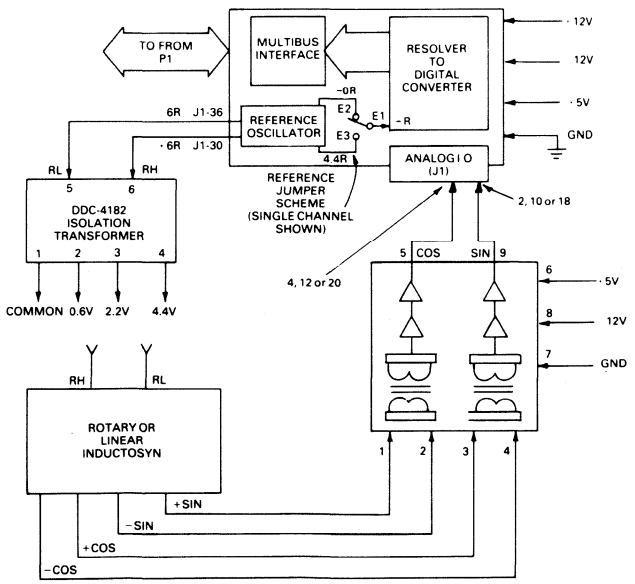
Reference excitation level for inductosyn applications is dependent upon the type of inductosyn and scale length; therefore, the optional multi-tapped DDC-4181 Isolation Transformer is designed to supply a reference signal that is compatible with the most commonly used inductosyns. These applications frequently use the +6V and −6V reference output from the DDC-35500 J1 connector (e.g. pins 30 & 36, 29 & 35 or 32 & 38)* connected respectively to the DDC-4182 RH (pin 6) and RL (pin 5) input terminals. When the DDC-4182 is connected as shown in Figure 3, the Inductosyn Connection Table is used to determine the connection scheme.

*Any combination of +6V to RH and −6V to RL is acceptable and will produce the voltage level required for inductosyn application.



Notes: 1a. For resolvers with 26V rms reference and 11.8 V rms Line to Line outputs (0.454 transformation ratio):
RH=GND
RL=J1-39,40 or 42 (−4.4R)
b. For resolvers with (0.165 transformation ratio):
RH=J1-29,30,32 (+6R)
RL=J1-35,36,38 (−6R)

FIGURE 2. RESOLVER CONNECTION DIAGRAM



Notes: 1. Induction applications using scale lengths between 3 meters and 8.25 meters do not require Isolation Transformer (DDC-4182). Connect Inductosyn signal outputs to DDC 4181 Dual Preamplifier in accordance with the Inductosyn Connection Table.
2. Power supplies for the Multibus card may be connected to Chassis Connector (P1) or via external test points; consult factory.

FIGURE 3. INDUCTOSYN CONNECTION DIAGRAM

PIN ASSIGNMENT TABLE (J1)

PIN	FUNCTION	PIN	FUNCTION
1	NC	26	+5V
2	SIN CH. 3	27	−12V
3	NC	28	−12V
4	COS CH. 3	29	+6R
5	NC	30	+6R
6	RET CH. 3	31	NC
7	NC	32	+6R
8	REF CH. 3	33	NC
9	NC	34	NC
10	SIN CH. 2	35	−6R
11	NC	36	−6R
12	COS CH. 2	37	NC
13	NC	38	−6R
14	RET CH. 2	39	NC
15	NC	40	−4.4R
16	REF CH. 2	41	NC
17	NC	42	−4.4R
18	SIN CH. 1	43	−0 R
19	+12V	44	−0 R
20	COS CH. 1	45	NC
21	+12V	46	−0 R
22	REF CH. 1	47	ANALOG GND
23	+12V	48	ANALOG GND
24	REF CH. 1	49	NC
25	+5V	50	ANALOG GND

INDUCTOSYN CONNECTION TABLE

SCALE LENGTHS BETWEEN 3 AND 8.25 METERS			
J1 PIN	VOLTAGE	SCALE LENGTH	OSCILLATOR VOLTAGE
29,30,32 35,36,38	+6R (RH) −6R (RL)	8.25M	12V
29,30,32 39,40,42	+6R (RH) −4.4R (RL)	7M	10.4V
29,30,32 47,48,50	+6R (RH) GND (RL)	4M	6V
39,40,42 47,48,50	−4.4R (RL) GND (RH)	3M	4.4V
SCALE LENGTHS OF LESS THAN 3 METERS			
SCALE LENGTH	INDUCTOSYN TYPE	DDC-4182 VOLTAGE	INDUCTOSYN (RH) TERMINAL TO DDC-4182 PIN NO.
3M	Linear	4.4V	4,1
1.5M	Linear	2.2V	3,1
1.25M	Linear	1.6V	3,2
Rotary Inductosyn	Rotary	0.6V	2,1

DUAL PREAMPLIFIER (DDC-4181) JUMPER CONNECTION TABLE

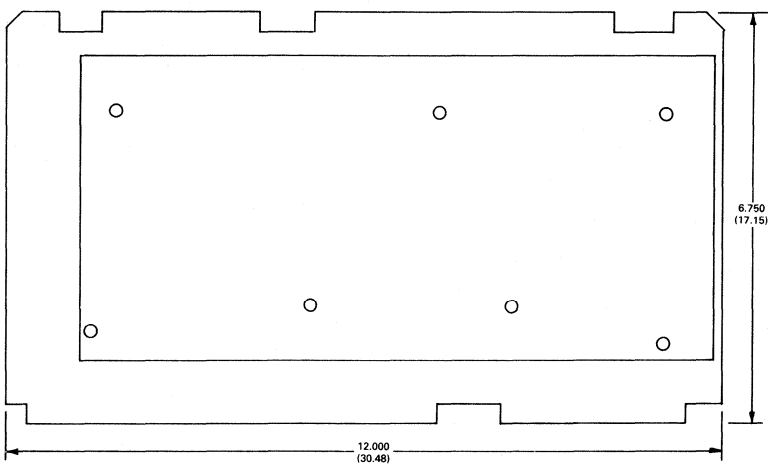
INPUT VOLTAGE (MV)-RMS	TB 1 TERMINAL CONNECTIONS	TB 2 TERMINAL CONNECTIONS
1.7-2.3	1 to 4 and 5 to 8	3 to 4 and 7 to 8
2.1-2.8	2 to 4 and 6 to 8	3 to 4 and 7 to 8
2.6-3.4	3 to 4 and 7 to 8	3 to 4 and 7 to 8
3.1-4.1	1 to 4 and 5 to 8	2 to 4 and 6 to 8
3.8-5.0	2 to 4 and 6 to 8	2 to 4 and 6 to 8
4.6-6.2	3 to 4 and 7 to 8	2 to 4 and 6 to 8
5.6-7.5	1 to 4 and 5 to 8	1 to 4 and 5 to 8
5.8-9.2	2 to 4 and 6 to 8	1 to 4 and 5 to 8
8.3-11.4	3 to 4 and 7 to 8	1 to 4 and 5 to 8

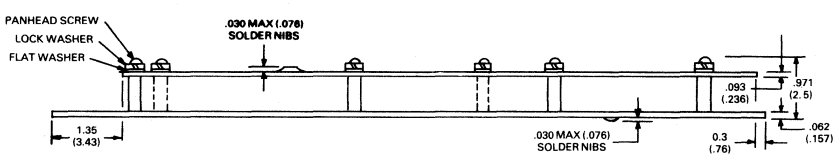
PIN ASSIGNMENT TABLE (P1)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	SIGNAL GND	23	$\overline{\text{XACK}}$ (XFER ACKNOWLEDGE)	45	$\overline{\text{ADR C}}$	67	$\overline{\text{DAT 6}}$
2	SIGNAL GND	24	NOT USED	46	$\overline{\text{ADR D}}$	68	$\overline{\text{DAT 7}}$
3	+5VDC	25	NOT USED	47	$\overline{\text{ADR A}}$	69	$\overline{\text{DAT 4}}$
4	+5VDC	26	NOT USED	48	$\overline{\text{ADR B}}$	70	$\overline{\text{DAT 5}}$
5	+5VDC	27	NOT USED	49	$\overline{\text{ADR 8}}$	71	$\overline{\text{DAT 2}}$
6	+5VDC	28	$\overline{\text{ADR 10}}$	50	$\overline{\text{ADR 9}}$	72	$\overline{\text{DAT 3}}$
7	+12VDC	29	NOT USED	51	$\overline{\text{ADR 6}}$	73	$\overline{\text{DAT 0}}$
8	+12VDC	30	$\overline{\text{ADR 11}}$	52	$\overline{\text{ADR 7}}$	74	$\overline{\text{DAT 1}}$
9	NOT USED	31	$\overline{\text{CCLK}}$ (CONSTANT CLOCK)	53	$\overline{\text{ADR 4}}$	75	SIGNAL GND
10	NOT USED	32	$\overline{\text{ADR 12}}$	54	$\overline{\text{ADR 5}}$	76	SIGNAL GND
11	SIGNAL GND	33	NOT USED	55	$\overline{\text{ADR 2}}$	77	NOT USED
12	SIGNAL GND	34	$\overline{\text{ADR 13}}$	56	$\overline{\text{ADR 3}}$	78	NOT USED
13	NOT USED	35	NOT USED	57	$\overline{\text{ADR 0}}$	79	−12VDC
14	NOT USED	36	NOT USED	58	$\overline{\text{ADR 1}}$	80	−12VDC
15	NOT USED	37	NOT USED	59	NOT USED	81	+5VDC
16	NOT USED	38	NOT USED	60	NOT USED	82	+5VDC
17	NOT USED	39	NOT USED	61	NOT USED	83	+5VDC
18	NOT USED	40	NOT USED	62	NOT USED	84	+5VDC
19	$\overline{\text{MRDC}}$ (MEM READ CMD)	41	NOT USED	63	NOT USED	85	SIGNAL GND
20	$\overline{\text{MWTC}}$ (MEM WRITE CMD)	42	NOT USED	64	NOT USED	86	SIGNAL GND
21	NOT USED	43	$\overline{\text{ADR E}}$	65	NOT USED		
22	NOT USED	44	$\overline{\text{ADR F}}$	66	NOT USED		

MECHANICAL OUTLINE

NOTE: Dimensions shown are in inches (centimeters).



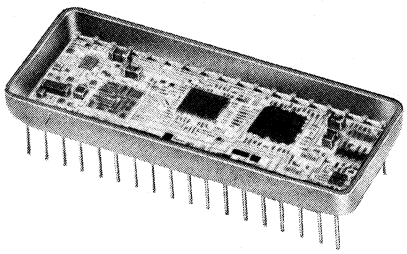


ORDERING INFORMATION

ORDER: DDC-35500-600

NOTE: DDC-4181 Dual Preamplifier and DDC-4182 Isolation Transformer may be ordered as optional accessories.

IDC-14542 AND IDC-14544*



12 AND 14 BIT INDUCTOSYN™ TO DIGITAL CONVERTER

DESCRIPTION

The IDC-14542 and IDC-14544 are high quality, Inductosyn or resolver to digital converters. Their custom monolithic chip design enables them to be packaged in a 36 pin, hermetically sealed DDIP, which significantly reduces size and weight. These converters are available in 12 or 14 bit resolutions with tracking rates of 100 and 25 rps, and accuracies of ±8.5 and ±5.3 minutes respectively.

The signal and reference frequency range is 600 Hz to 11 kHz for 14 bit units and 360 Hz to 22 kHz for 12 bit units. The 2V line to line input is transient protected voltage follower buffer, resolver format (sine and cosine).

Digital outputs include Count (CB), which is useful for turns counting applications. An Inhibit (INH) input provides a means for freezing parallel data in the transparent latch (figure 1), while the converter continues to track the input. Parallel data, which is

3-state natural binary angle is available in two bytes for interfacing with an 8 bit microprocessor bus. Other control logic inputs include MSB and LSB byte, which control the 3-state operation of two output buffers which may be enabled simultaneously or independently (logic "0"), according to the application.

A unique control transformer algorithm enables the IDC-14542 and IDC-14544 to output highly accurate jitter free data, while the internal type II servo tracking loop permits a DC analog velocity output which exhibits no lag up to the specified tracking rate.

APPLICATIONS

These converters are particularly suited for multi-axis machine tool applications, where accurate and repeatable positioning is required. The IDC-14542 and IDC-14544 will resolve an Inductosyn pitch of 0.1 inch to 24.4 and 6.1 microinches respectively.

Inductosyns have been widely used in high accuracy military applications such as fire control systems and satellite tracking systems.

FEATURES

- *MIL-STD-883B OPTIONAL*
- *100 RPS TRACKING (12 BITS)*
- *12 OR 14 BITS*
- *3-STATE LATCHED OUTPUTS*
- *LOW POWER*
- *OPERATES AT UP TO 20 KHz*

*Patented

Note:
Inductosyn™ is a trademark of Farrand Controls Corporation.

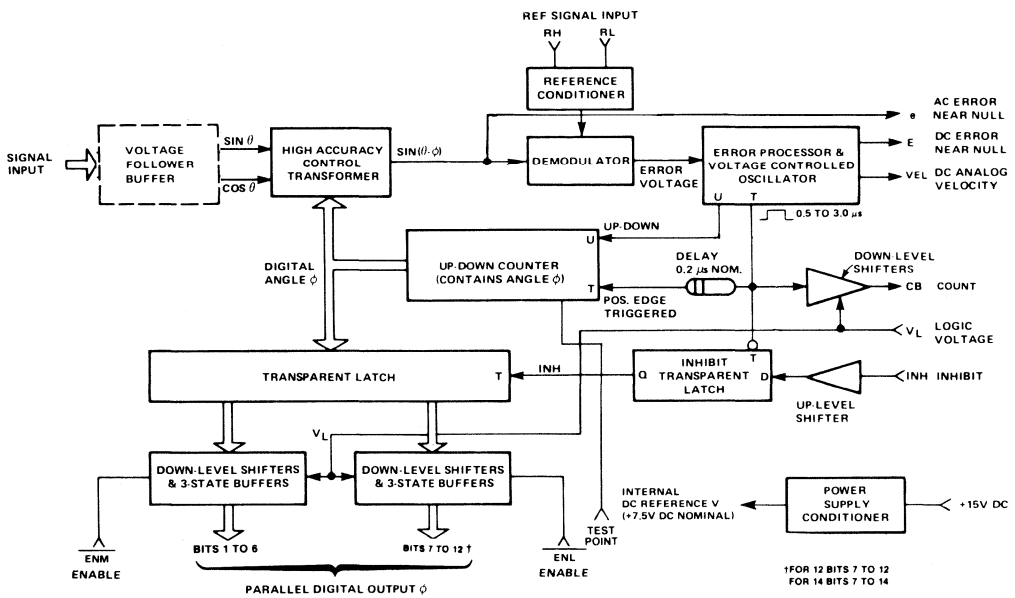


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Apply over temperature range, power supply range, reference frequency and amplitude range, ±10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	UNITS	VALUE	
CONVERTER		**IDC-14542**	**IDC-14544**
RESOLUTION	bits	12	14
ACCURACY	min	±8.5	±5.3
DYNAMIC CHARACTERISTICS			
Input Rate	rps	100	25
Acceleration Constant		K_a=460,000	K_a=370,000
Settling Time (179° step to 1 LSB)	ms	60	90
Velocity Constant		K_v=∞ (No limitation with type II servo loop)	
REFERENCE INPUT			
Carrier Frequency	Hz	360 to 22k	600 to 11k
Voltage Range	V_{rms}	4 to 50 (26 nom)	
Input Impedance			
Single Ended	Ω	50k min	
Differential	Ω	100k min	
Common Mode Range			
(DC Common mode plus recurrent AC peak)	V	60 max	
SIGNAL INPUT CHARACTERISTICS			
Input Signal Type		Sin and cos resolver signals referenced to internal DC reference V	
Voltage Level	V	2 nom, 2.3 max	
Maximum voltage without damage	V	15 rms continuous; 100 peak transient	
Input Impedance	Ω	Z_{in} 20M (transient protected voltage follower)	
DIGITAL INPUT/OUTPUT			
Logic		TTL/CMOS compatible, depending on logic supply voltage	
Inputs			
Inhibit (INH)		Logic "0" inhibits	
Enable Bits 1-6 $\overline{ENM}$		$\overline{ENM}$ and $\overline{ENL}$ [logic "0" Enables, logic "1" high impedance	
Enable Bits 7-12 $\overline{ENL}$			
Enable Bits 7-14 $\overline{ENL}$			
OUTPUTS			
Parallel Data	bits	12 or 14 parallel lines, natural binary angle, positive logic	
Count (CB)		0.7 to 2.0 μsec positive pulse; leading edge initiates counter update	
Drive Capability	TTL	1 std load, 1.6 mA at 0.4 V max (logic "0")	
	TTL	10 std loads, 0.4 mA at 2.8 V min (logic "1")	
	μA	10 max (high impedance)	
ANALOG OUTPUTS			
Internal DC Reference (V)		+15 VDC/2 ~ 7.5V nom	
AC Error (e)		10 mV rms per LSB of error (14 bits) 12.5 mV rms per LSB of error (12 bits)	
Filtered DC Error Voltage (E)		−1 VDC per +LSB of error (±3 LSB range), 14 bits −1.25 VDC per +LSB of error (±3 LSB range), 12 bits	
POWER SUPPLY CHARACTERISTICS			
Nominal Voltage		+15V Supply	Logic Supply
Voltage Range	V	+11 to +16.5	+4.5 to +15
Maximum Voltage Without Damage	V	+18	+18
Current or Impedance		25 mA max	Z_{in}=5kΩ min
TEMPERATURE RANGES			
Operating			
−3XX	°C	0 to +70	
−1XX	°C	−55 to +125	
Storage	°C	−55 to +135	
PHYSICAL CHARACTERISTICS			
Package		36 pin DDIP	
Size	in	0.78 x 1.9 x 0.21 (19.7 x 48 x 5.3 mm)	
Weight	oz	1.0 (28 gm)	

TECHNICAL INFORMATION

DIRECT INPUT

The input of the IDC-14542 and IDC-14544 requires that an external signal conditioner be provided to establish a 2.0 V rms input signal referenced to the converter's internal DC reference (V). Figure 4 suggests a method for amplifying the output of an Inductosyn to meet the required signal input level. The use of this circuit will sufficiently condition the input so resistors R3 and R4 are not needed for most applications.

Trimming should be done by measuring the differential voltage at the input of the op amp closest to the Inductosyn slider (+sin). The output voltage is then measured to determine the gain. The same procedure is performed on the +cos amplifier. A high accuracy digital voltmeter is recommended for the final output readings. Capacitors C1 and C2 are used to create a DC voltage block.

LOGIC INPUT/OUTPUT

Logic outputs consist of 12 or 14 parallel data bits and count (CB). All logic outputs are short-circuit proof to ground and to positive voltages as high as V_L. The CB output is a positive 0.7-2.0μs pulse and data changes about 0.2μs after the leading edge of the pulse, because of an internal delay (figure 1). Data is valid 0.5μs after the leading edge of a CB. Angle is determined by adding bits in the "1" state.

The parallel digital outputs are gated to provide 6 or 8 bit bytes when the MSB byte is enabled ($\overline{ENM}$). The 8 bit byte is reserved for the 14 bit resolution converter only. The LSB byte ($\overline{ENL}$) is gated to provide a 6 bit byte. When the Enables for the gates are at logic "0" the gate outputs are at normal logic "1" or "0", depending on the bit state. When the Enables are at logic "1" the gate outputs are high impedance and the subsystem sees an essentially open line. Outputs are valid 0.5μs after an Enable is driven to logic "0". For 12 and 14 bit parallel output operation, when the 3-state feature is not used, the Enable lines should be tied to logic "0".

The Inhibit (INH) logic input locks the transparent latch so that the bits will remain stable while data is being transferred (see Figure 1). The output is stable 0.5μs after the Inhibit is driven to logic "0". A logic "0" at the T input locks the latch, and a logic "1" allows the bits to change. The purpose of the INH transparent latch is to prevent the transmission of invalid data when there is an overlap between the CB and INH. While the counter is not being updated the CB is at logic "0" and the INH latch is transparent. When the CB goes to logic "1" the INH latch is locked. If a CB occurs after an INH has been applied, the latch will remain locked and its data cannot change until the CB returns to logic "0". If an INH is applied during a CB pulse, the latch will not lock until the CB pulse is over. The purpose of the 0.2μs delay is to prevent a race condition between the CB and the INH in which the up-down counter begins to change just as an INH is applied.

Since the IDC-14542 and IDC-14544 converters contain a CMOS device, standard CMOS handling procedures should be followed.

TIMING

Figure 2 shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. The output data change is initiated by the leading edge of the CB pulse, delayed by the 0.2μs (nominal) delay. The output becomes stable in less than 0.5μs even though the CB pulse may last longer. Data transfer can be made synchronous with the leading edge of CB, delayed by 0.5μs. (See Timing Diagram.)

An Inhibit input, regardless of its duration, does not affect converter update. A simple method of interfacing to a computer, asynchronous to CB pulse, is to (a) apply the inhibit, (b) wait 1.5 μs min., (c) transfer the data and (d) release the inhibit.

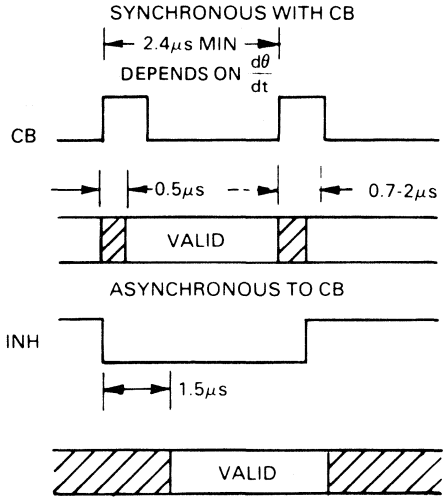
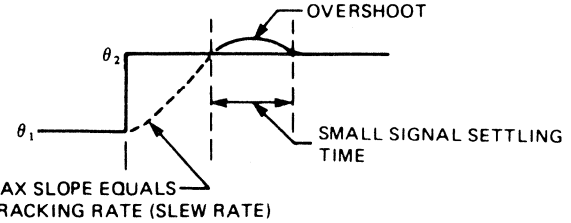


FIGURE 2. TIMING DIAGRAM

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V=\infty$) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltage is not the +15VDC nominal value, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage.

As long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The figure shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to a final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT

ANALOG OUTPUTS

The analog outputs are V, e, E and VEL. V is an internal DC reference, ±7.5 VDC nominal. The outputs e, E and VEL ride on the internal DC reference voltage V, and should be measured with respect to V. Outputs can swing ±5V when the voltage level of the +15V power supply is +15V. The output swing changes proportionally if the level is not a +15V.

AC error (e) is proportional to the error $(\theta-\phi)$ with 10 mV/LSB nominal for the 14 bit unit and 12.5 mV/LSB nominal for the 12 bit units.

E is a filtered DC voltage proportional to the error $(\theta-\phi)$near the null point, with −1 VDC/+LSB of error for the 14 bit unit and −1.25 VDC/+LSB of error for the 12 bit units.

Velocity output (VEL) is a DC voltage proportional to angular velocity $d\theta/dt=d\phi/dt$. The output is positive for an increasing angle.

Maximum loading for each analog output is 1.0 mA. Outputs e, E, and VEL are not required for normal operation of the converter; V is used as internal DC reference.

The outputs e, E and VEL are not closely controlled or characterized. Consult factory for further information.

$$G=\frac{680^2\left(\frac{S}{300}+1\right)}{S^2\left(\frac{S}{3000}+1\right)} \qquad G=\frac{610^2\left(\frac{S}{300}+1\right)}{S^2\left(\frac{S}{3000}+1\right)}$$

12 BIT **14 BIT**

CONVERTER LOOP DYNAMICS

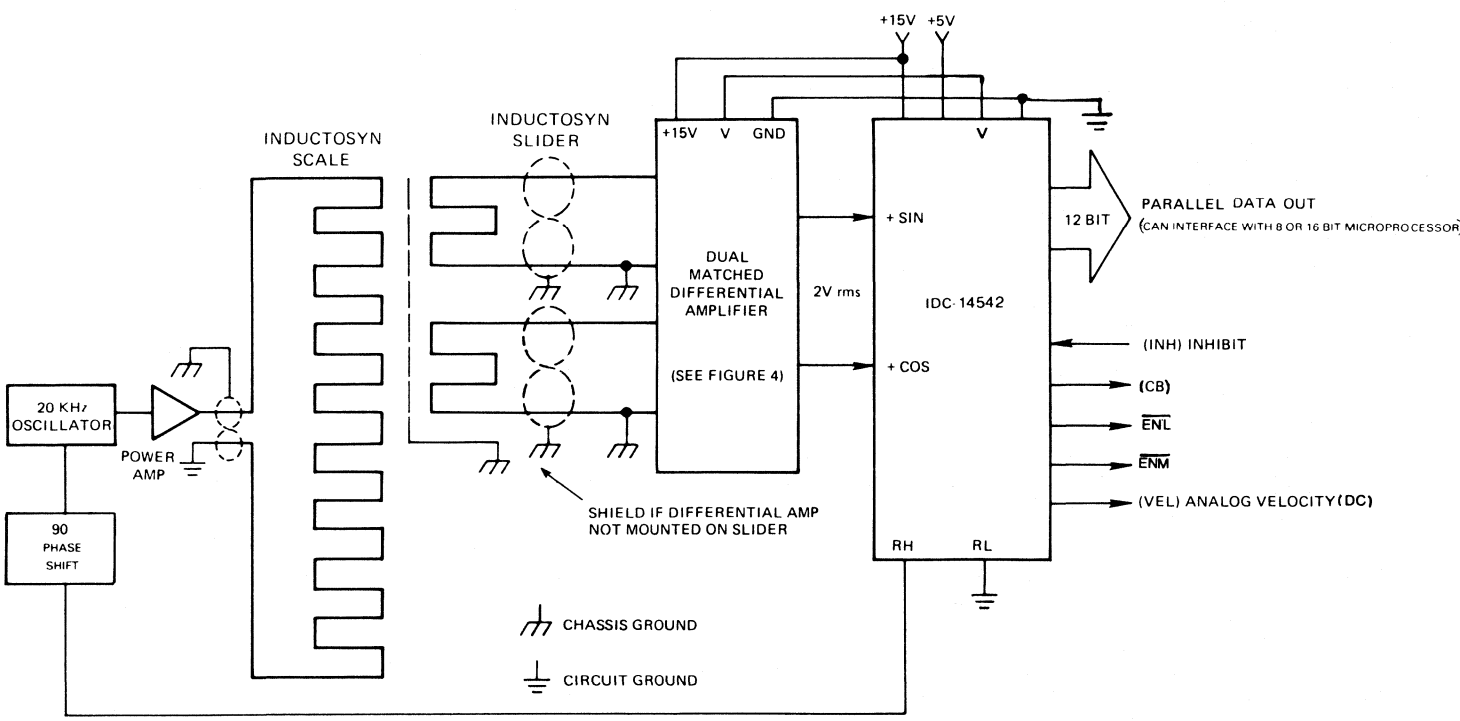
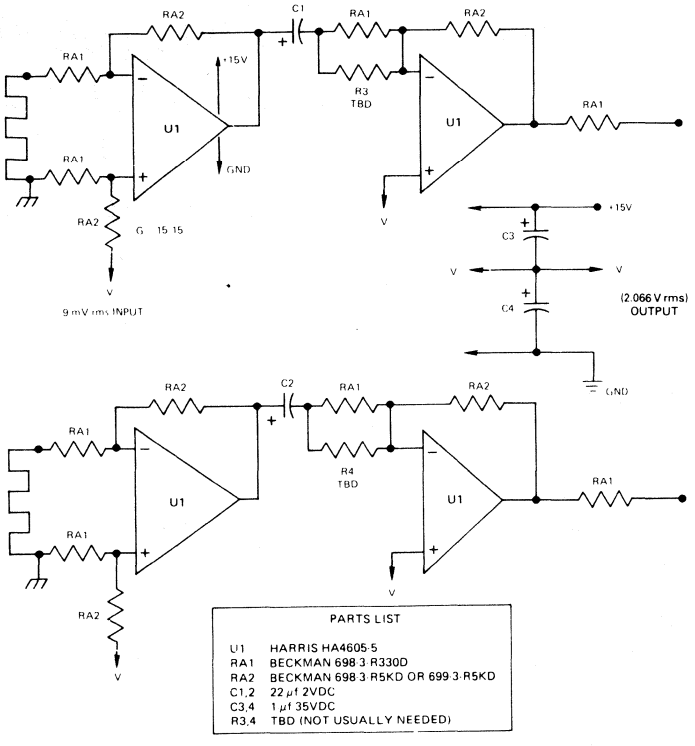


FIGURE 3. INDUCTOSYN CONNECTION DIAGRAM



PARTS LIST	
U1	HARRIS HA4605-5
RA1	BECKMAN 698-3-R330D
RA2	BECKMAN 698-3-R5KD OR 699-3-R5KD
C1,2	22 μf 2VDC
C3,4	1 μf 35VDC
R3,4	TBD (NOT USUALLY NEEDED)

NOTES: 1. For other input levels select RA1 and RA2 as required. Standard values are: 100, 200, 330, 470, 500, 1K, 2K, 2.2K, 4.7K, 5K, 10K, 15K, and 20KΩ.
2. For lower input levels use Harris HA-4625-5

FIGURE 4. DUAL PREAMPLIFIER DIAGRAM

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
	Voltage Follower Buffer	18	Bit 14
		19	RH (Ref High)
1	NC	20	RL (Ref Low)
2	COS	21	N.C.
3	SIN	22	E (Filtered DC Error Out)
4	NC	23	θ (Analog Velocity Out)
5	Bit 1 MSB	24	CB (Converter Busy)
6	Bit 2	25	ENL (Enable, Bits 7 to 14)*
7	Bit 3	26	ENM (Enable, Bits 1 to 6)
8	Bit 4	27	e (AC Error Out)
9	Bit 5	28	V_L (Logic Voltage Input
10	Bit 6	29	GND
11	Bit 7	30	T.P.
12	Bit 8	31	N.C.
13	Bit 9	32	+15V (Power Supply In)
14	Bit 10	33	INH (Inhibit)
15	Bit 11	34	V (Internal DC Ref)
16	Bit 12	35	BC (Buffered Cos)
17	Bit 13	36	BS (Buffered Sin)

NOTES:
BS and BC pins are used in other applications.
*Enable 7 to 12 (IDC-14542)

IN GENERAL

For applications where a square wave is more convenient than the conventional sine wave, the IDC-14542 and IDC-14544 are capable of operating with square waves.

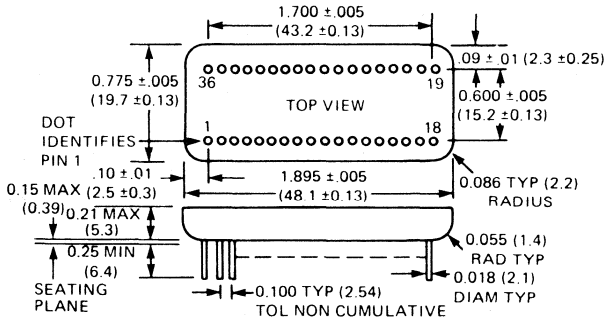
For users who desire a built-in test (BIT) function to detect position error between the input and output, a simple detection circuit can be implemented with the AC error signal provided by the IDC-14542 and IDC-14544 converter. The schematic diagram for the BIT circuit is available from DDC.

RELIABILITY

MTBF values are very high because the use of custom monolithics greatly decreases the number of active components, because thin film resistor networks are used, and because of careful thermal design. Summaries of MTBF calculations are available on request.

All DDC hybrids are built in accordance with requirements of MIL-STD-883B. Screening is based on the requirements of Method 5004/5008 except for burn-in, which is optional. The computed MTBF value for MIL-STD-883B processing (including burn-in) is 6,400,000 hours, Ground Benign, at 25°C.

MECHANICAL OUTLINE
36 PIN DOUBLE DIP



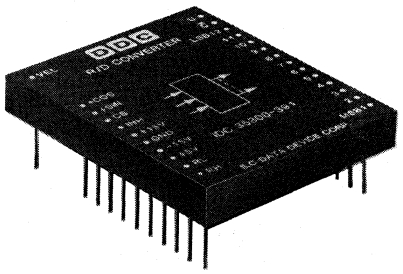
NOTES
1. Dimensions shown are in inches. (millimeters)
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

Specifications are subject to change without notice.

ORDERING INFORMATION

IDC-1454 X-X X X

- Family Code
- Resolution
  - 2=12 bits
  - 4=14 bits
- Temperature (operating)
  - 1=−55°C to +125°C (Case)
  - 3=0°C to +70°C (Case)
- Rel Grade:
  - 0=Std
  - 1=883
- Accuracy:
  - 2=±8.5′ (12 bit only)
  - 3=±5.3′ (14 bit only)



12-BIT INDUCTOSYN™ TO DIGITAL CONVERTER

DESCRIPTION

The IDC-35300 is a low cost 12-bit Inductosyn™ to digital or resolver to digital converter. It has an accuracy of ±8.5 minutes, while maintaining a repeatability of 1 LSB. The reference and signal frequency range is 2 kHz to 22 kHz and the tracking rate is 180 rps (typical). A velocity output (VEL) scaled to 15 rps/V is provided as a standard feature. The IDC-35300 also provides Carry ($\overline{C}$), Count (CB), and Direction (U) outputs for multi-turn and incremental applications.

This converter is a low cost, low profile unit with a unique control transformer algorithm, which provides inherently higher accuracy and jitter free output to 4096 counts per Inductosyn pitch or a resolver revolution. Through the use of a Type II tracking loop these converters do not exhibit velocity lag up to the specified tracking rate. In addition, the output is always fresh and continuously available. Each unit is factory trimmed and does not require field adjustments or calibration. An optional high speed tracking feature is available for higher than specified input rates (consult factory).

APPLICATIONS

The IDC-35300 is particularly suited for multi-axis machine tool applications, where accurate and repeatable positioning is a requirement. An Inductosyn pitch of 0.1 inch or a 360° resolver revolution can be resolved into 24.4 micro inches or 5.3 minutes respectively. When operated at 20 kHz the IDC-35300 provides a 2:1 signal to noise improvement over 10 kHz operation for Inductosyn applications. For multi-turn applications such as for a resolver with lead screw attached, the IDC-35300 provides a Carry ($\overline{C}$) pulse each time the internal counter goes through "0" in either direction. Typical Inductosyn and resolver applications are depicted in figures 3 and 5. Incremental and turns counting connection diagrams are shown in figure 6.

FEATURES

- *LOW COST*
- *OPERATES WITH INDUCTOSYN OR RESOLVER*
- *COUNT (CB), DIRECTION (U) AND CARRY ($\overline{C}$) OUTPUTS*
- *VELOCITY OUTPUT*
- *OPERATES AT 20 KHz*
- *LOW PROFILE*
- *HIGH SPEED TRACKING OPTION*

*Patented

Note: Inductosyn™ is a trademark of Farrand Controls Corporation.

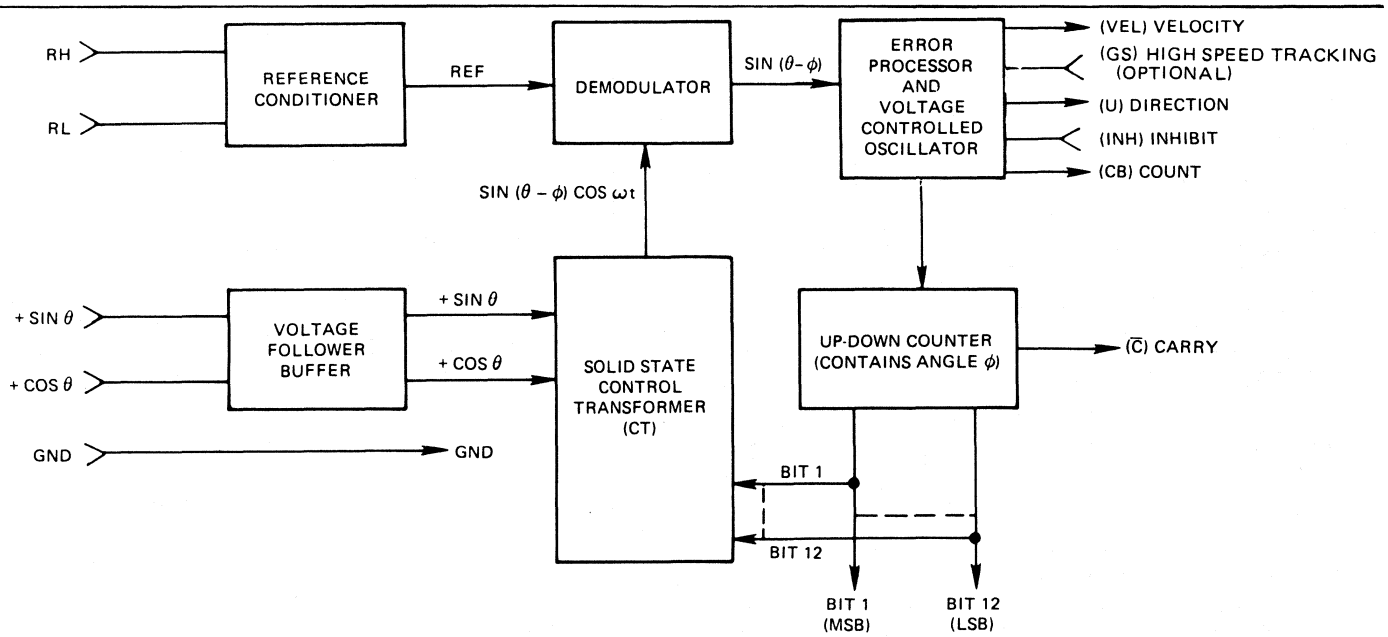


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Apply over temperature range, power supply range, reference frequency and amplitude range, ±10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	12-bits (1 LSB = .088°)
ACCURACY	±8.5 arc-minutes
SIGNAL AND REFERENCE INPUT	
Signal Frequency Range	2 kHz to 22 kHz
Signal Input Impedance	20 MΩ, min
Signal Input	2V rms ± 10% (25V w/o damage)
Reference Voltage Range	2–10V rms (30V w/o damage)
Reference Input Impedance (Resistive)	13 kΩ min (single ended) 26 kΩ min (differential)
DIGITAL INPUT/OUTPUT	
Logic Type	TTL
Inhibit Input (INH) Loading	Logic "0" inhibits 0.2 Std. TTL loads plus 18 kΩ min pull-up to +5V supply
Outputs	
Type	Low power Schottky
12 Parallel Data Bits	Natural binary angle; positive logic
Count (CB)	0.6 to 1.2 μsec positive pulse. Data changes on leading edge.
Carry ($\overline{C}$)	Active low
Direction (U)	Logic "1" = up "0" = down
Drive Capability	2 Std. TTL loads −55°C to +105°C 4 Std. TTL loads 0°C to +70°C
VELOCITY OUTPUT	Derived from an op-amp with low impedance output. Positive output for increasing angle.
DC Velocity Voltage (VEL)	+1V DC per +15 rps
Voltage Range	±10V min
Scale Factor	±150 rps = ±10V
DYNAMIC CHARACTERISTICS	
Input Rate	150 rps min (180 rps typ)†
Acceleration for 1 LSB Lag	8900°/sec² typ
Settling Time	
For Normal Tracking (Up to Specified Input Rate)	No lag error
Settling to 1 LSB	30 msec (typ) } For 179° step change
Settling to Final Value	40 msec (typ) }
Velocity Constant (Type II Servo Loop)	$K_V = \infty$
Acceleration Constant Nominal Value	Ka = 100,000/sec²

†Consult factory for extended tracking rate

POWER SUPPLIES			
Nominal Voltage	+15V Supply	−15V Supply	+5V Logic Supply
Voltage Range	+11 to +16.5V	−11 to −16.5V	+4.5 to +5.5V
Max. Voltage Without Damage	+18V	−18V	+7V
Current	6 mA, typ 10 mA, max	18 mA, typ 30 mA, max	80 mA, typ 120 mA, max

TEMPERATURE RANGE	
Operating (−3XX)	0°C to + 70°C
(−1XX)	−55°C to +105°C
Storage	−55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size (Encapsulated Module)	3.125 x 2.625 x 0.42 inch (79 x 67 x 11 mm)
Weight	4 oz (113 g)

TIMING

Figure 2 shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a count pulse (CB). The CB is a positive pulse 0.6 to 1.2 μsec long. Data changes on the leading edge of the CB pulse, and data can be transferred 0.3 μsec after the leading edge. Other digital signals on the timing diagram are discussed under DIGITAL OUTPUTS.

The simplest method of interfacing with a computer is to transfer data as a fixed time interval after the Inhibit is applied. The converter will ignore an Inhibit applied during the "busy" interval until that interval is over. Timing is as follows: (a) apply the Inhibit, (b) wait 0.3 μsec, (c) transfer the data and (d) release the Inhibit. Extra CB pulses will not occur if the input angle changes while the counter is locked by the Inhibit.

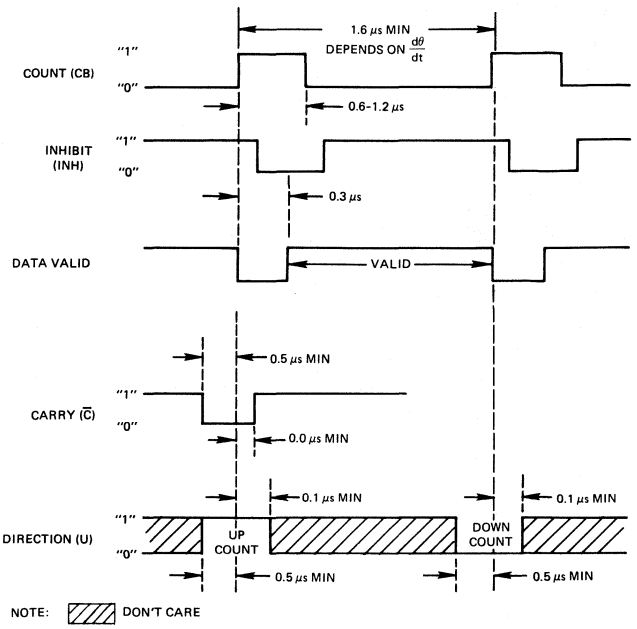


FIGURE 2. TIMING DIAGRAM

VELOCITY OUTPUT (VEL)

Velocity Output is a DC voltage proportional to the angular velocity. A +1VDC output corresponds to + 15 rps. Maximum loading for this analog output is 1 mA.

DIGITAL OUTPUTS

Natural binary angle coding for the 12 digital output lines is given in the bit weight table. Angle is determined by adding bits in the "1" state. The CB output is a positive 0.6 to 1.2 μsec pulse, and data changes on the leading edge of the pulse. At 150 rps the minimum period between pulses is 1.6 μsec as shown in the timing diagram.

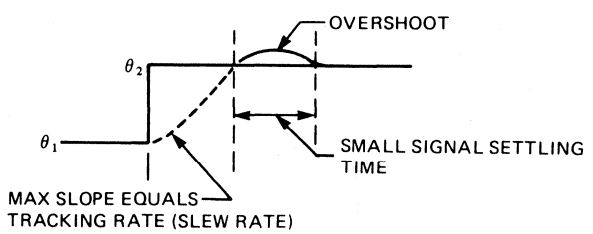
Bit	Deg/Bit	Min/Bit
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.406	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12 LSB	0.0879	5.27

BIT WEIGHT TABLE

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltages are not the +15VDC nominal values, the specified input rates will increase or decrease in proportion to the fractional change in voltage. The +15V supply voltage will determine the positive maximum velocity and the −15V supply voltage will determine the negative maximum velocity.

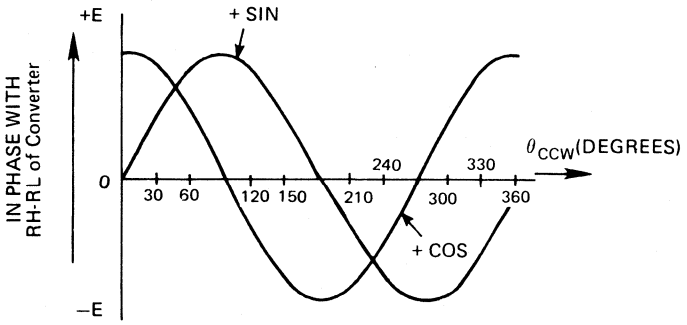
As long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The figure shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT

The nominal open loop transfer function is given by:

$$G = \frac{318^2\left(\frac{S}{147}+1\right)}{S^2\left(\frac{S}{1470}+1\right)}$$



INDUCTOSYN OR RESOLVER OUTPUT SIGNALS

COUNT (CB)

Although the computer usually requires that the data be synchronized, it can be read out asynchronously into a holding register using the trailing edge of the "CB" signal to effect the parallel transfer. In this configuration, the data out of the register will change smoothly from θ to (θ ±1 LSB).

DIRECTION (U)

The direction line is an active low with resistor pull-up. The direction output is valid as shown in the timing diagram. (U) is logic "1" for counting up and logic "0" for counting down. Logic level at the (U) pin is valid up through 0.5 μs before and 0.1 μs after the leading edge of the count (CB) edge.

CARRY ($\overline{C}$)

The Carry output occurs once per pitch or cycle. Its purpose is to mark or indicate when the Inductosyn slider crosses from one pitch to the next. With a one speed resolver, the pulse will occur once per rotation. Carry output is active low and occurs at least 0.5 μs prior to the leading edge of (CB) and ends a minimum of 0 μs after the same leading edge.

POWER SUPPLIES

The main power supplies can vary their specified ranges with no change in the converter specifications except for a proportional change in the maximum tracking rates.

When testing or evaluating the converters, it is advisable to limit the current to each of three power supplies. Set each limit to 50% greater than the maximum current listed for that supply in the specifications table.

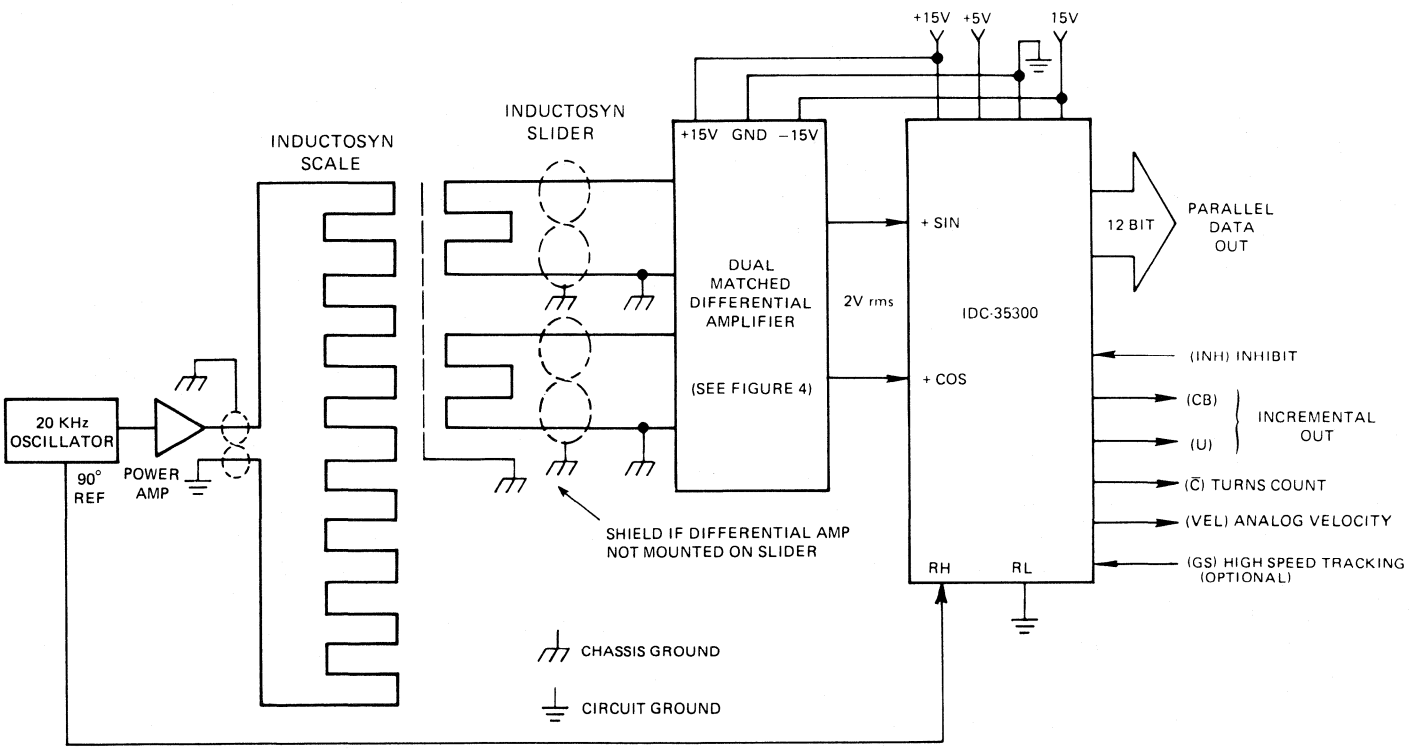


FIGURE 3. TYPICAL INDUCTOSYN CONNECTION

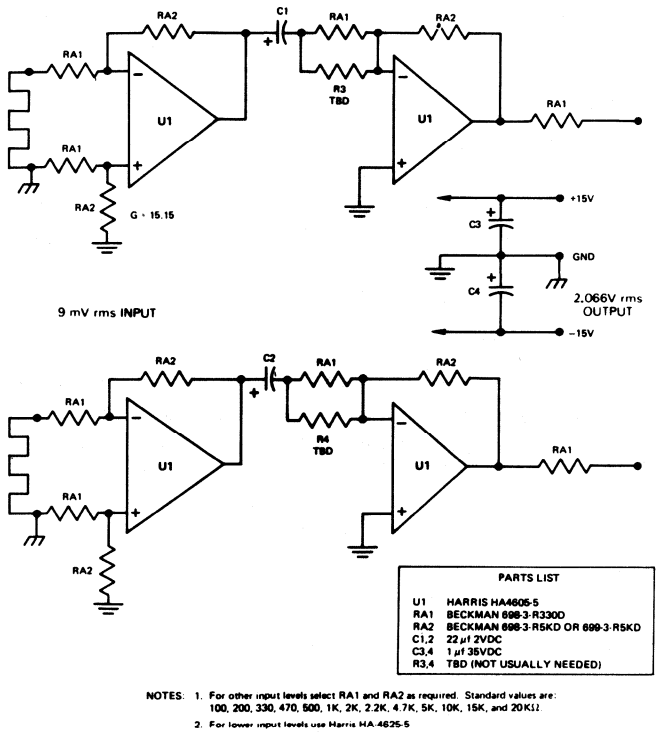


FIGURE 4. DUAL MATCHED DIFFERENTIAL AMPLIFIER

DUAL MATCHED DIFFERENTIAL AMPLIFIER

Figure 4 suggests a method for amplifying the output of an Inductosyn to meet the required signal input level of the IDC-35300 (2V rms, ±10%). The use of this circuit will sufficiently condition the input with only minor trimming of resistors R3 or R4.

Trimming should be done by measuring the differential voltage at the input of op amp closest to the slider (+sin). The output voltage is then measured to determine the gain. The same procedure is performed on the +cos amplifier. Resistors R3 and R4 are selected to match the output voltage of +sin and +cos as closely as possible. A high accuracy digital voltmeter is recommended for the final output readings. Capacitors C1 and C2 are used to create a DC voltage block.

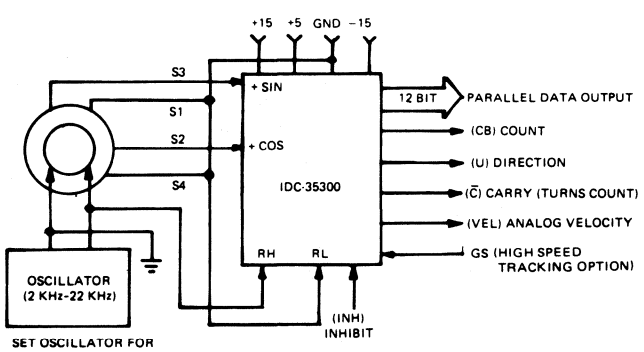


FIGURE 5. TYPICAL RESOLVER CONNECTION

RESOLVER APPLICATIONS

The IDC-35300 may be used with resolvers when connected as shown in figure 5. When using a brushless resolver however; a transmitter type is recommended, because receiver types inherently exhibit degraded accuracy in transmitter applications.

HIGH SPEED OPTION

The IDC-35300 is available with high speed tracking capability (reduced accuracy) which is implemented by a user controlled logic state applied to a modified converter module. The high speed function provides for continuous tracking during slewing when tracking rates may exceed the specified input rate of the standard converter. When activated the high speed option allows the IDC-35300 to track up to 16 times the specified rate of 150 rps. To obtain this optional feature, contact the factory.

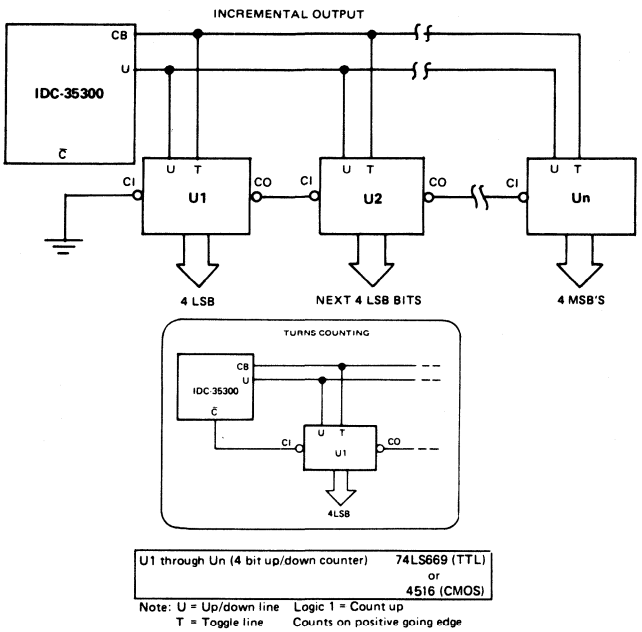


FIGURE 6. INCREMENTAL AND TURNS COUNTING CONNECTION DIAGRAM

MICROPROCESSOR INTERFACE

The circuit shown in Figure 7 illustrates a simple method for interfacing the IDC-35300 to an 8-bit microprocessor for multi-turn applications. The configurations shown interfaces 8-bits of turns count (up to 255 turns) and 12-bits of converter position data to an 8-bit processor.

(1) The reference signal fed to the converter is 90° out of time-phase (leading) to the Inductosyn excitation.

(2) 3-state buffers are used to interface the position and turns count outputs to the microprocessor data bus.

(3) The IDC-35300 features a CARRY ($\overline{C}$) output, used for turns counting. In addition, the converter has INHIBIT ($\overline{INH}$) logic that freezes the parallel data outputs and disables the COUNT (CB) output to avoid a missed CARRY pulse and turns count while an INHIBIT is applied. For the "multi-turn" (multi-pitch distance) Inductosyn application, this feature is an absolute necessity.

(4) The logic circuit consisting of the single-shot and OR gate is used to provide at least one rising edge to the clock inputs of the synchronously loading up/down turns counters during a CLEAR TURNS COUNTER command, which is used for set-up purposes to zero the turns count.

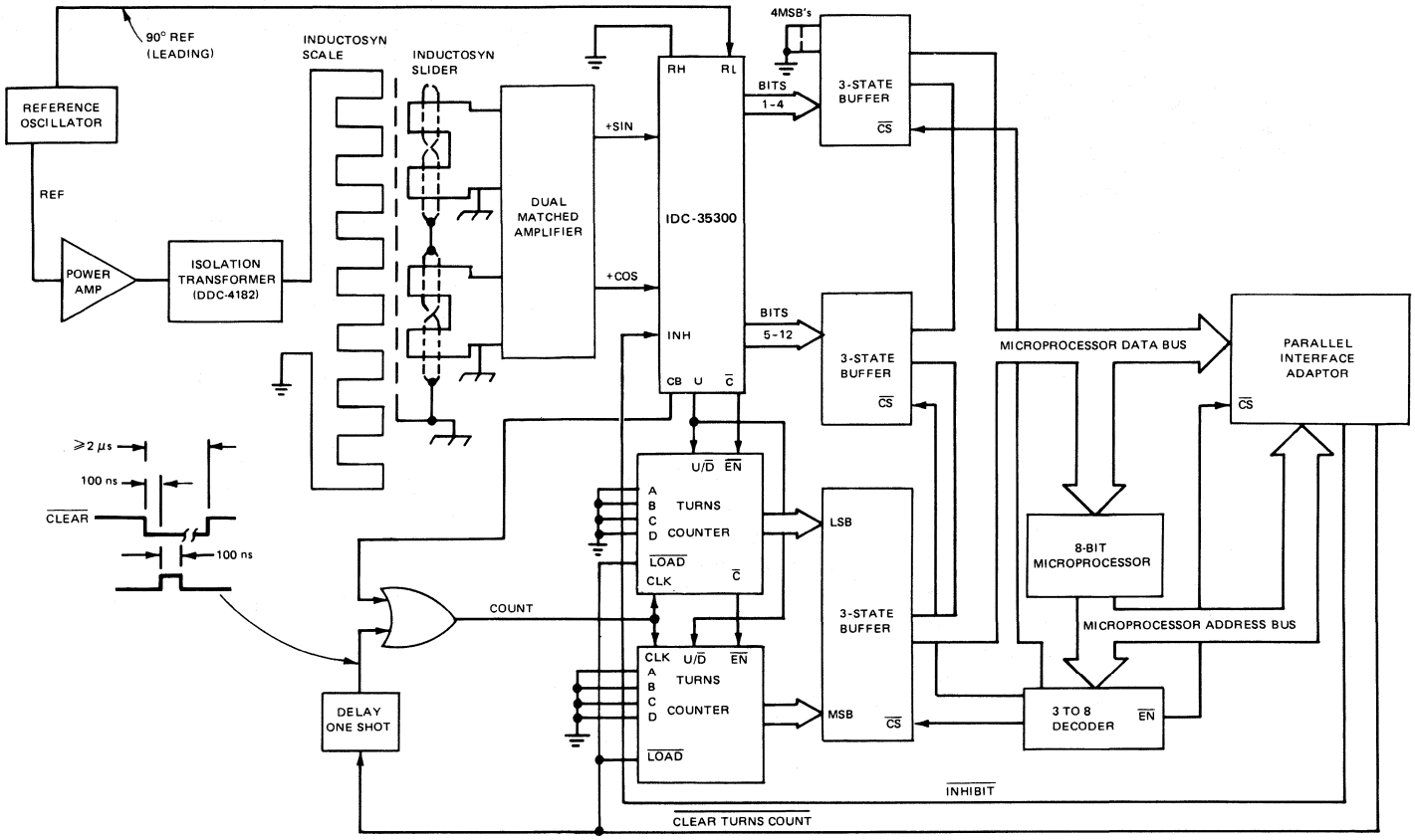
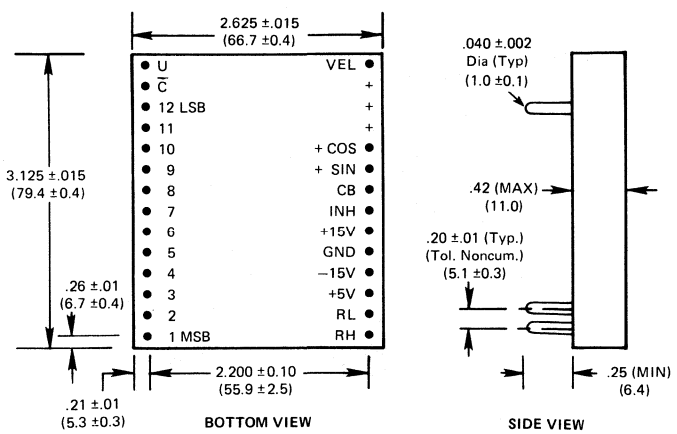


FIGURE 7. MICROPROCESSOR INTERFACE DIAGRAM

MECHANICAL OUTLINE



NOTES:
1. Dimensions are in inches (millimeters).
2. Pin material is electrosoldered brass per MIL-F-14072, M222.
3. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F
4. Pin labels on bottom view are for reference only.

ORDERING INFORMATION

IDC–35300–3 9 2

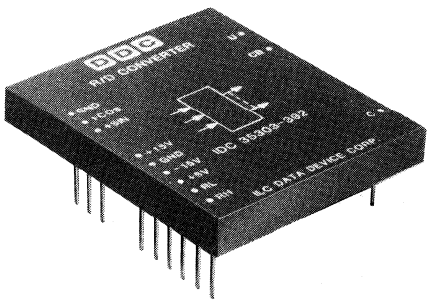
- Accuracy:
  2 = ±8.5 minutes
- Input:
  9 = 2V rms
- Temperature Range (operating):
  1 = –55°C to +105°C
  3 = 0°C to +70°C
- Family Code

NOTE: For High Speed Tracking Option Consult Factory.

IDC-35303*

ILC DATA DEVICE CORPORATION

4000 COUNT INDUCTOSYN™ TO DIGITAL CONVERTER



DESCRIPTION

The IDC-35303 is a low cost 4000 count Inductosyn or resolver to digital converter. It has an accuracy of ±8.5 minutes, with a repeatability of 1 LSB. The reference and signal frequency range is 2 kHz to 22 kHz with a tracking rate of 150 rps (typical). The IDC-35303 also provides Carry (C), and Direction (U) outputs.

This converter is a low cost, low profile unit with a unique control transformer algorithm, which provides inherently higher accuracy and jitter free output of 4000 counts per Inductosyn pitch or a resolver revolution. Through the use of a Type II tracking loop design these converters do not exhibit velocity lag up to the specified tracking rate. In addition, the output is always fresh and continuously available. Each unit is factory trimmed and does not require field adjustments or calibration.

APPLICATIONS

The IDC-35303 is particularly suited for multi-axis machine tool applications, where accurate and repeatable positioning is a requirement. An Inductosyn pitch of 0.1 inch or a 360° resolver revolution can be resolved into 25 micro inches or 5.4 minutes respectively. When operated at 20 kHz, the IDC-35303 provides a 2:1 signal to noise improvement over 10 kHz operation for Inductosyn applications. For multi-turn applications IDC-35303 provides a Carry (C) pulse each time the internal counter goes through "0" in either direction. Typical Inductoysn and resolver applications are depicted in Figures 4 and 7.

FEATURES

- *4000 COUNT INCREMENTAL OUTPUT PER REVOLUTION OR PITCH*
- *ACCURACY: ±8.5 MINUTES*
- *OPERATING FREQUENCY: 2 KHz to 22 KHz*
- *TRACKING RATE: 120 REVOLUTIONS OR PITCHES PER SECOND*
- *DIRECTION AND MAJOR CARRY OUTPUTS*

*Patented

Note: Inductosyn™ is a trademark of Farrand Controls Corporation.

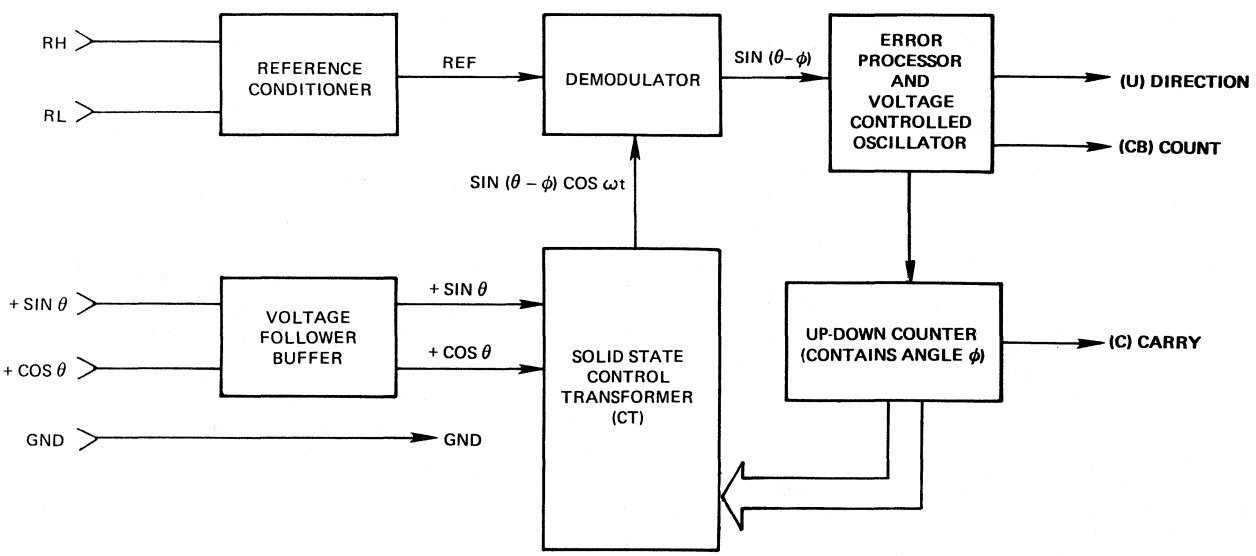


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Apply over temperature range, power supply range, reference frequency and amplitude range, ±10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	4000 counts/revolution or pitch
ACCURACY	±8.5 arc-minutes
SIGNAL AND REFERENCE INPUT	
Signal Frequency Range	2 kHz to 22 kHz
Signal Input Impedance	20 MΩ, min
Signal Input	2V rms ±10% (25V w/o damage)
Reference Voltage Range	2-10V rms (30V w/o damage)
Reference Input Impedance (Resistive)	13 kΩ min (singled ended) 26 kΩ min (differential)
DIGITAL INPUT/OUTPUT	
Logic Type	TTL
Outputs	
Type	Low power Schottky (can drive remote loads)
Count (CB)	0.6 to 1.2 μsec positive pulse.
Carry (C)	Active high
Direction (U)	Logic "1" = up "0" = down
Drive Capability	2 Std. TTL loads −55°C to +105°C 4 Std. TTL loads 0°C to +70°C
DYNAMIC CHARACTERISTICS	
Input Rate	120 rps min (150 rps typ)
Acceleration for 1 LSB Lag	16,700°/sec² typ

PARAMETER	VALUE
Settling Time	
For nomal Tracking (Up to Specified Input Rate)	No lag error
Settling to 1 LSB	30 msec (typ). } For 179° step change
Settling to Final Value	40 msec (typ) } For 179° step change
Velocity Constant (Type II Servo Loop)	$K_V = \infty$
Acceleration Constant	
Nominal Value	Ka = 185,000/sec²
POWER SUPPLIES	
Nominal Voltage	+15V Supply / −15V Supply / +5V Logic Supply
Voltage Range	+11 to +16.5V / −11 to −16.5V / +4.5 to +5.5V
Max. Voltage (Without Damage)	+18V / −18V / +7V
Current	6 mA, typ / 18 mA, typ / 80 mA, typ 10 mA, max / 30 mA, max / 120 mA, max
TEMPERATURE RANGE	
Operating (−3XX)	0°C to 70°C
(−1XX)	−55°C to +105°C
Storage	−55°C to +125°C
PHYSICAL CHARACTERISTICS	
Size (Encapsulated Module)	3.125 x 2.625 x 0.42 inch (79 x 67 x 11 mm)
Weight	4 oz (113 g)

TIMING

Figure 2 shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB, and generates a count pulse (CB). The CB is a positive pulse 0.6 to 1.2 μsec long.

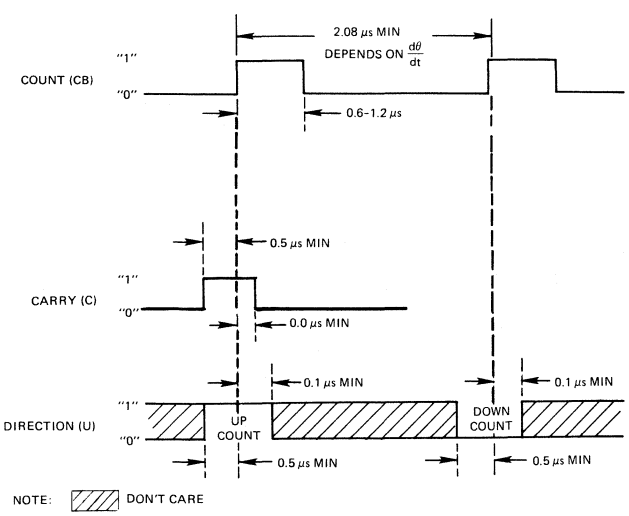


FIGURE 2. TIMING DIAGRAM

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltages are not the +15VDC nominal values, the specified input rates will increase or decrease in proportion to the fractional change in voltage. The +15V supply voltage will determine the positive maximum velocity at the −15V supply voltage will determine the negative maximum velocity.

As long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. Figure 3 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.

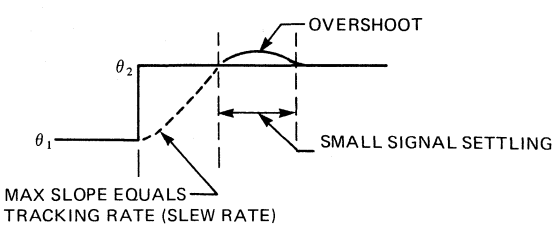
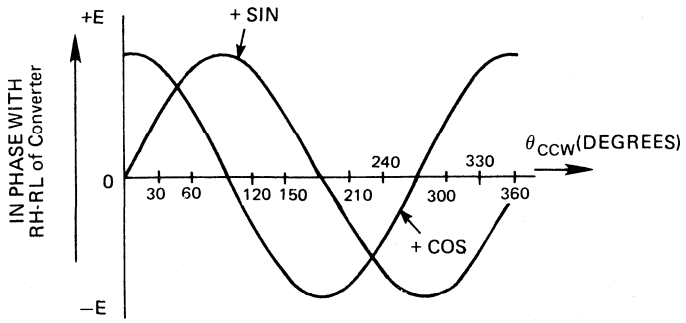


FIGURE 3. RESPONSE TO A STEP INPUT

The nominal open loop transfer function is given by:

$$G = \frac{430^2\left(\frac{S}{215} + 1\right)}{S^2\left(\frac{S}{2150} + 1\right)}$$



INDUCTOSYN OR RESOLVER OUTPUT SIGNALS

COUNT (CB)

The CB output is a positive pulse which occurs 4,000 times per resolver revolution or an Inductosyn pitch. The pulse width of CB is 0.6 to 1.2 μs. The CB period is dependent on velocity, but its minimum duration is 2.08 μs.

DIRECTION (U)

The direction line is an active low with resistor pull- up. The direction output is valid as shown in the timing diagram. (U) is logic "1" for counting up and logic "0" for counting down. Logic level at the (U) pin is valid up through 0.5 μs before and 0.1 μs after the leading edge of the count (CB) edge.

CARRY (C)

The carry output occurs once per pitch or revolution. Its purpose is to mark or indicate when the Inductosyn slider crosses from one pitch to the next. With a one speed resolver, the pulse will occur once per revolution.Carry output is active high and occurs at least 0.5 μs prior to the leading edge of (CB) and ends a minimum of 0 μs after the same leading edge.

POWER SUPPLIES

The main power supplies can vary their specified ranges with no change in the converter specifications except for a proportional change in the maximum tracking rates.

When testing or evaluating the converters, it is advisable to limit the current to each of three power supplies. Set each limit to 50% greater than the maximum current listed for that supply in the specification table.

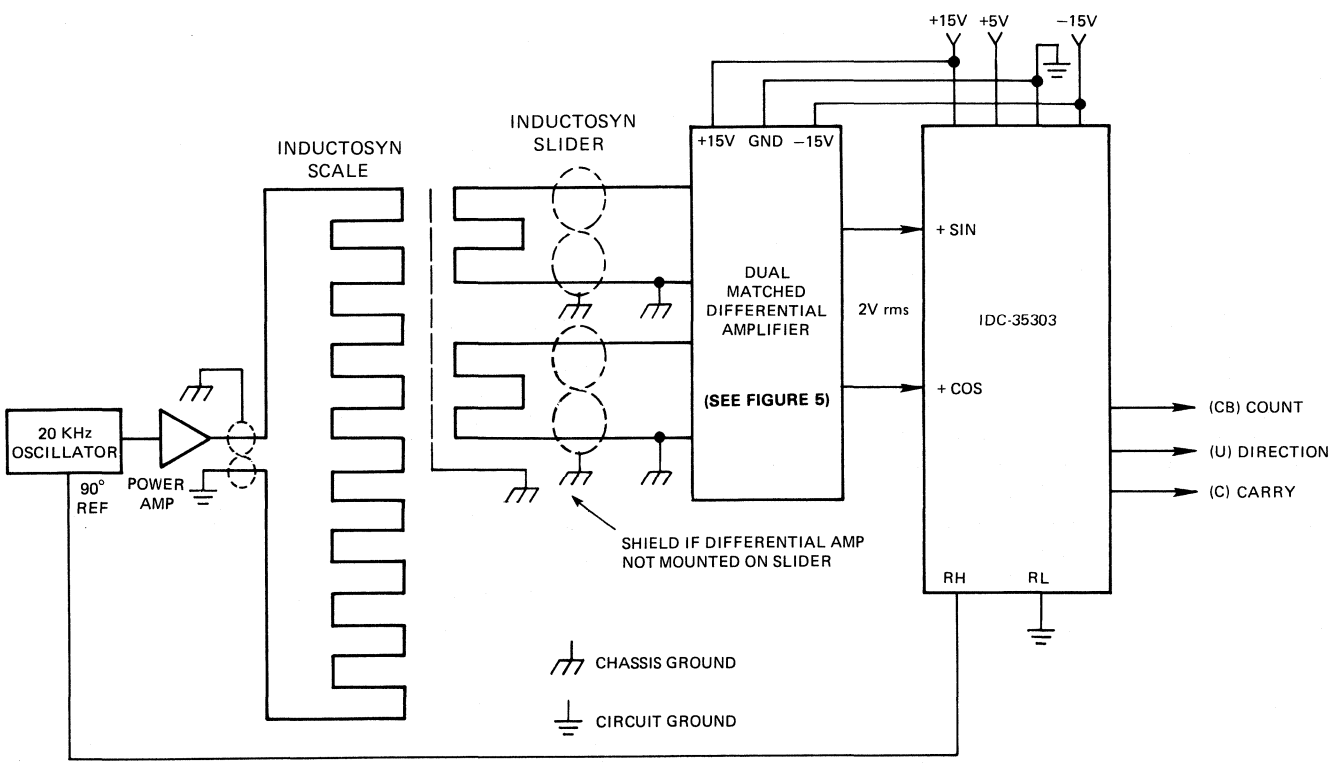
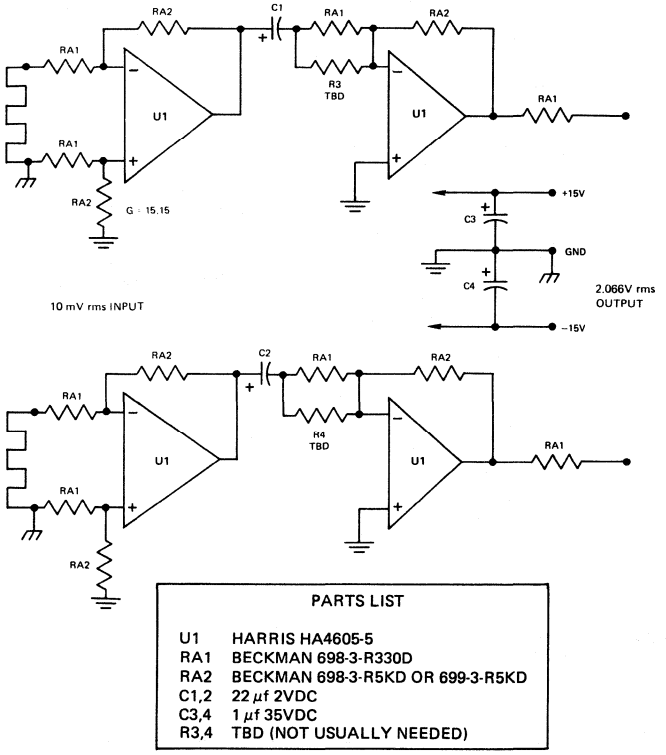


FIGURE 4. TYPICAL INDUCTOSYN CONNECTION



PARTS LIST

U1	HARRIS HA4605-5
RA1	BECKMAN 698-3-R330D
RA2	BECKMAN 698-3-R5KD OR 699-3-R5KD
C1,2	22 μf 2VDC
C3,4	1 μf 35VDC
R3,4	TBD (NOT USUALLY NEEDED)

NOTES: 1. For other input levels select RA1 and RA2 as required. Standard values are: 100, 200, 330, 470, 500, 1K, 2K, 2.2K, 4.7K, 5K, 10K, 15K, and 20KΩ.
2. For lower input levels use Harris HA-4625-5

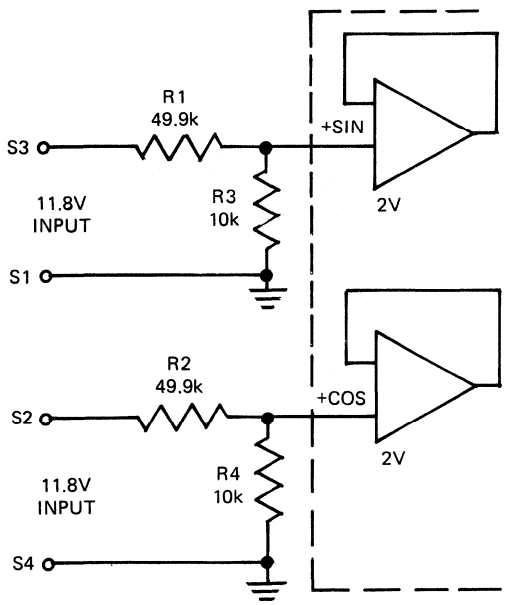
FIGURE 5. DUAL MATCHED DIFFERENTIAL AMPLIFIER

Figure 5 suggests a method for amplifying the output of an Inductosyn to meet the required signal input level of the IDC-35303 (2V rms, ±10%). The use of this circuit will sufficiently condition the input so resistors R3 and R4 are not needed for most applications.

Trimming should be done by measuring the differential voltage at the input of the op amp closest to the slider (+sin). The output voltage is then measured to determine the gain. The same procedure is performed on the +cos amplifier. A high accuracy digital voltmeter is recommended for the final output readings. Capacitors C1 and C2 are used to create a DC voltage block.

EXTERNAL RESISTOR SCALING FOR RESOLVER APPLICATIONS

The IDC-35303 may be operated with resolvers that have signal output levels of 11.8V. A simple voltage divider circuit is shown in figure 6 to implement external resistor scaling of the resolver signals (S1-S4) to 2V rms. Care must be taken to maintain a .05% match between R1-R2 and R3-R4 to insure full accuracy.



SCALING FOR AN 11.8V RESOLVER INPUT
R1 matched to R2 to .05%
R3 matched to R4 to .05%

FIGURE 6. RESOLVER INPUT SCALING

RESOLVER APPLICATIONS

The IDC-35303 may be used with resolvers when connected as shown in Figure 7. When using a brushless resolver however; a transmitter (rotor excited) type is recommended, because receiver (stator excited) types inherently exhibit degraded accuracy when operated as transmitters.

PRINTED CIRCUIT BOARD MOUNTING

When mounting a converter on a printed circuit board, it is very important to keep logic-level signals as far away from the AC and power signals as possible. Under no circumstances should AC or power pins be adjacent to data pins at the connector. It is also prudent to keep the AC and power pins separated from each other. The intent is to make it impossible to short logic inputs/outputs to AC or power pins with scope-probes, etc.

It is strongly recommended that circuit layouts be designed in such a way that plated through-holes are not required when mounting hybrid or discrete modules. If all lands connecting to pins are located on the opposite (dip) side of PC board from the module, there will be no risk of destroying a pin connection by ripping out the plate through-hole connection if the module has to be removed. It will also be much easier to unsolder a module without damaging it.

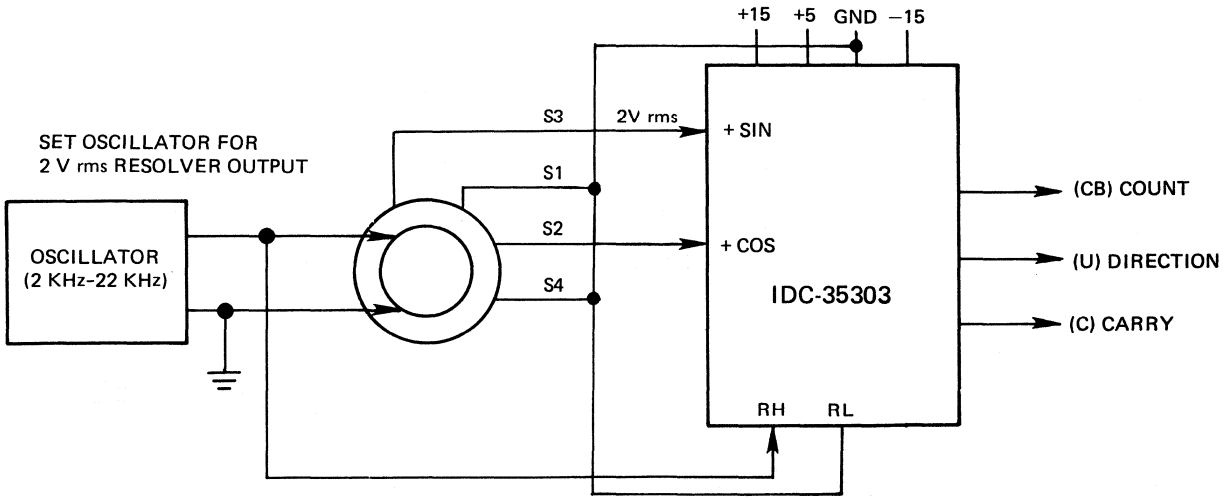
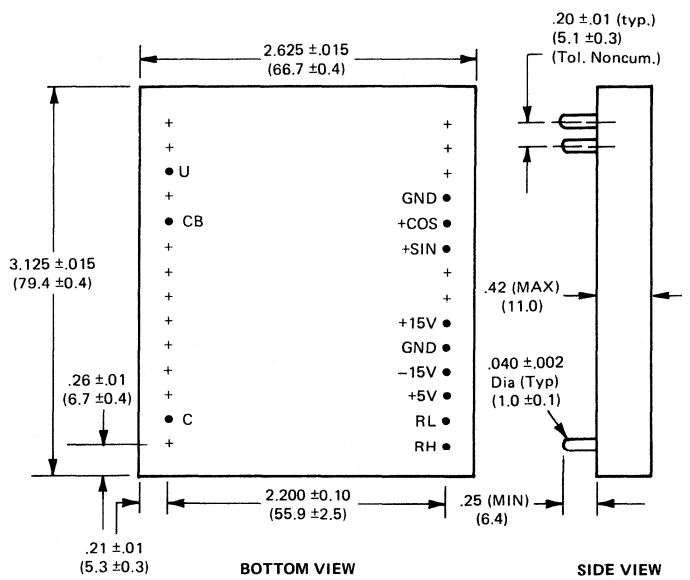


FIGURE 7. TYPICAL RESOLVER CONNECTION

MECHANICAL OUTLINE



NOTES:
1. Dimensions are in inches (millimeters).
2. Pin material is electrosoldered brass per MIL-F-14072, M222.
3. Case material is glass filled Diallyl Phthalate per MIL-M-14, Type SDG-F.
4. Pin labels on bottom view are for reference only.

ORDERING INFORMATION

IDC - 35303 - 3 9 2

- 2 — ACCURACY: 2 = ± 8.5 minutes
- 9 — INPUT: 9 = 2V rms
- 3 — TEMPERATURE RANGE (OPERATING): 1 = -55°C to +105°C; 3 = 0°C to + 70°C
- 35303 — FAMILY CODE

SECTION H

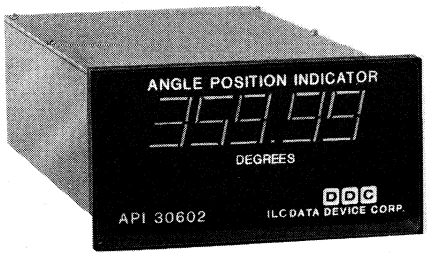
SYNCHRO INSTRUMENTS

PRODUCT SUMMARY TABLE

Name	Form Factor	Features	Page
API-30602	2.03 x 3.84 x 7.50"	5 decade (0.01°) tracking synchro/resolver panel meter. Accuracy of +0.05° or +0.03°. Accepts all standard synchro and resolvers. ±2° offset adjust for system zeroing. 3-state output for microprocessor data bus interfacing.	279
SIM-31200 SERIES	14.5 x 8.12 x 3.47"	Synchro or rsolver angle simulator with high accuracy, wide band operation. Programmable via 16 pad keyboard (local mode), standard parallel I/O or optional IEEE-488 I/O (remote mode). Accurate to ±0.003° (no load) and 0.008° (full load). 5VA drive capability.	283
SPI-30800	4.6 x 6.5 x 9.0"	Microcomputer based solid state selsyn indicator. Ruggedly designed for replacement of electro-mechanical indicators. Fully programmable decimal positioning, selectable counts per turn and number presetting.	288
SPI-30880/ SPI-30881	6.25 x 3.63 x 6"	Solid state remote selsyn indicator for industrial applications. Companion to SPI-30800 microcomputer based master indicator. Available in passive or "talk-back" configuration in a NEMA 12 ruggedized construction. Receives serial data over a two wire twisted shielded communication line.	293
SR-103 or HSR-103	11-3/4 x 8-1/8 x 1-3/4" rack mounted	Programmable angle indicators; convert synchro and resolver signals to BCD angle with LED display and parallel data output with ±0.03° accuracy and 0.01° resolution for the SR-103/ and ±0.005° accuracy and 0.001° resolution for the HSR-103. Both units have remote control operation.	297
SR-203 or HSR-203	14-1/2 x 7-7/8 x 3-15/32	Programmable angle indicators; convert synchro and resolver signals to BCD angle with LED display and parallel data output accuracy and resolution are the same as SR-103/HSR-103. IEEE interface available in both SR-203 and HSR-203. May be bench or rack mounted.	301
MSR-236	12 x 10 x 5" in militarized case	Programmable multispeed angle indicator; converts single speed or dual (1:36 or 2:36) speed synchro or resolver signals to BCD angle with LED display and parallel data output with accuracies to ±0.01°. Front panel control operation.	305
SR-400 or SR-460	14-1/2 x 9-1/2 x 3-1/2" bench mount	Programmable angle simulator; produces standard synchro or resolver outputs. Angle input from either front panel 5 decade BCD angle switches or remote parallel BCD angle input. Both front panel and remote controls; LED angle display; accuracy is ±0.01° no load (±0.03° full load); 47-1000 Hz reference input.	308

API-30602*

0.01° LOW COST TRACKING SYNCHRO AND RESOLVER PANEL METER



DESCRIPTION**

The API-30602 is a small, low cost 5 decade (.01° resolution) synchro/resolver angle indicator. It can be pin programmed to accept synchro or resolver signals at 2, 11.8, 26 or 90V line-to-line. Its broadband (47-1200 Hz) frequency capability and three-state BCD output, for use with a microprocessor data bus, makes the API-30602 a versatile instrument. The unit is available in two accuracy grades: ±0.05° (standard unit) and ±0.03° (high accuracy).

The synchro/resolver to digital tracking converter (Figure 1) is the heart of the panel meter. Using a type II servo loop for continuous tracking, the API-30602 has no velocity lag up to ±180°/sec.

Standard features include ±2° offset adjust, which is convenient for system alignment and lamp test capability for display testing. An optional dimmer control is available for applications requiring varying display intensities. The API-30602 requires no field adjustment or calibration.

APPLICATIONS

The API-30602 can be used wherever accurate angle information is required for display, control, testing purposes or computation. Applications include production testing of synchros and resolvers, information translators in quality control systems, machine tool control, ship and aircraft navigation systems, and antenna positioning.

**API-30604/05/08/09 units are usable only in resolver mode with the 6V reference input provided by the panel meter.

FEATURES

- *VERSATILE: ACCEPTS ALL STANDARD SYNCHRO AND RESOLVERS*
- *±2° ZERO ADJUST FOR SYSTEM ALIGNMENT*
- *RESOLUTION: 0.01° ACCURACY: ±0.05° OR ±0.03°*
- *TYPE II SERVO TRACKING LOOP*
- *3-STATE OUTPUT FOR MICROPROCESSOR DATA BUS*
- *OPTIONAL DIMMER CONTROL*
- *SHAFT ANGLE TRANSDUCER OPTION*

*Patented

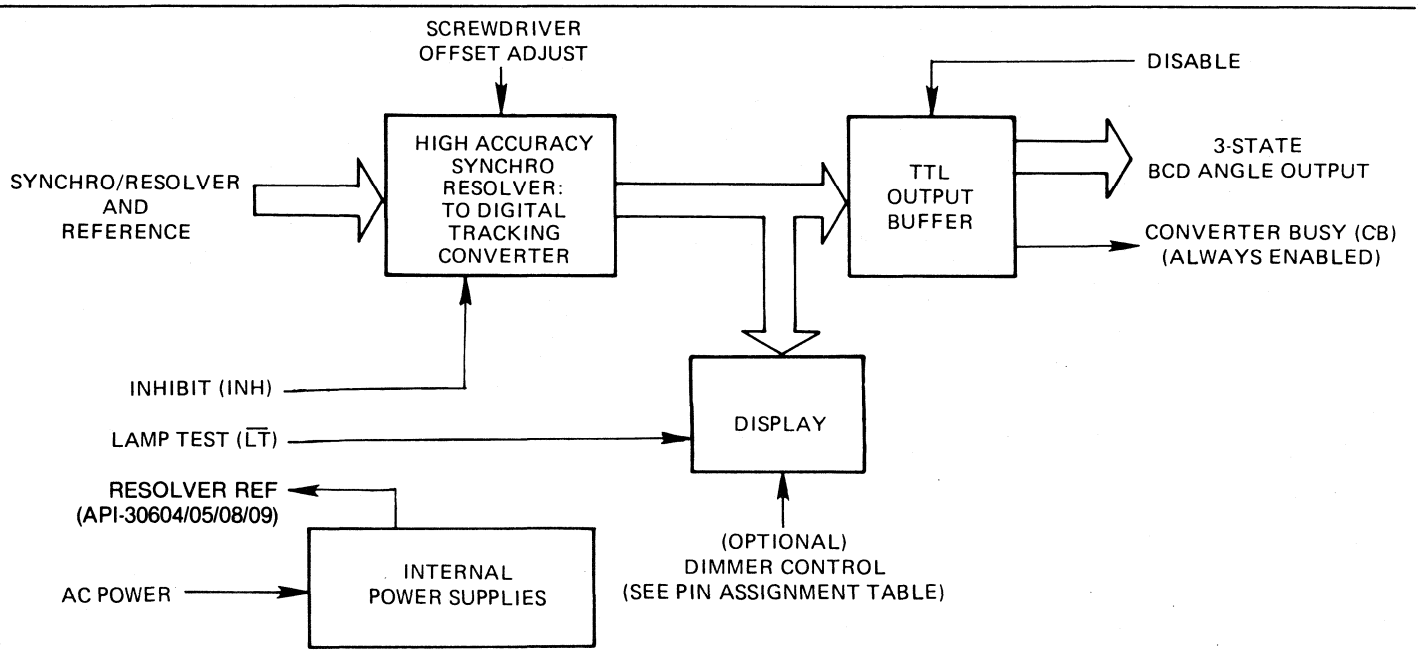


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

PARAMETER	VALUE			
MODEL	**API-30602 and API-30603**	**API-30604 and API-30605**	**API-30606 and API-30607**	**API-30608 and API-30609**
RESOLUTION	0.01° (5 BCD Digits)	0.01° (5 BCD Digits)	0.01° (5 BCD Digits)	0.01° (5 BCD Digits)
ACCURACY				
Standard	±0.05°	±0.05°	±0.05°	±0.05°
Hi Accuracy	±0.03°	±0.03°	±0.03°	±0.03°
REPEATABILITY	Within 0.01°	Within 0.01°	Within 0.01°	Within 0.01°
ANGLE RANGE				
(Continuous Rotation)	0° to 359.99°	0° to 359.99°	0° to 359.99°	0° to 359.99°
DISPLAY				
7 Segments 0.43 inch LED	5 Digits	5 Digits	5 Digits	5 Digits
REFERENCE INPUT				
(Solid State)				
Voltage	10 to 126V rms	6V rms	10 to 126V rms	6V rms
Frequency	47 to 1200Hz	47 to 63Hz	47 to 1200Hz	47 to 63Hz
Impedance	148KΩ min, Single Ended 296KΩ min, Differential	148KΩ min, Single Ended 296KΩ min, Differential	148KΩ min, Single Ended 296KΩ min, Differential	148KΩ min, Single Ended 296KΩ min, Differential
Harmonic Content	±10% max	±10% max	±10% max	±10% max
SIGNAL INPUT				
Input Type	Synchro or Resolver, Transformer Isolated	Resolver, Direct/Single Ended	Synchro or Resolver, Transformer Isolated	Resolver, Direct/Single Ended
Voltage Level (L-L)	11.8, 26 or 90V rms ±10%	2V rms ±10%	11.8, 26 or 90V rms ±10%	2V rms ±10%
Frequency	47 to 1200Hz	47 to 63Hz	47 to 1200Hz	47 to 63Hz
Allowable Phase Shift	±10° Relative to Ref	NA	±10° Relative to Ref	NA
Input Impedance	Resistive Balanced, Transformer Isolated 170KΩ min (Resolver) 148KΩ min (Synchro)	10M Ω min	Resistive Balanced, Transformer Isolated 170KΩ min (Resolver) 148KΩ min (Synchro)	10M Ω min
Breakdown Voltage	500V min to logic ground	NA	500V min to logic ground	NA
DYNAMIC CHARACTERISTICS				
Tracking Rate	180°/sec min			
Settling Time (To 1 LSB) for 179° Step	3 sec			
Open Loop Transfer Function	$G = \frac{18.6^2\left(\frac{S}{9}\right)+1}{S^2\left(\frac{S}{90}\right)+1}$			
DIGITAL INPUTS (TTL Compatible)				
Loading	0.5 std TTL loads max (0.8 mA)			
Inhibit (1NH)	"1" or open = track "0" or GND = inhibit			
Lamp Test (LT)	"1" or open = normal operation "0" or GND = all LED segments on			
Disables	"1" or open = three state outputs high impedance "0" or GND = enable			
DIGITAL OUTPUTS (TTL COMPATIBLE)				
Drive Capability	Three state, 10 TTL loads (16 mA)			
Synchro or Resolver Angle	Parallel data bits; BCD angle; positive logic, 5 decades 18 lines and one common ground line.			
Converter Busy (CB)	4 to 10 usec positive pulse; counts on leading edge			
POWER INPUT				
Voltage	115V / 26V	115V	220V / 100V	220V / 100V
Frequency	47 to 440Hz / 360 to 440Hz	47 to 63 Hz	47 to 440 Hz / 47 to 440Hz	47 to 63Hz / 47 to 63Hz
Current	70 mA / 0.3 A	70 mA	35 mA / 80 mA	37 mA / 80 mA
Isolation	Transformer Isolated	Transformer Isolated	Transformer Isolated	Transformer Isolated
Power	9VA max, 6.5VA typ	9VA max, 6.5VA typ	9VA max, 6.5VA typ	9VA max, 6.5VA typ
Breakdown Voltage	1000VDC min to logic ground	1000VDC min to logic ground	1000VDC min to logic ground	1000VDC min to logic ground
TEMPERATURE RANGE				
Operating	0°C to +70°C			
Storage	−65°C to +125°C			
PHYSICAL CHARACTERISTICS				
Size (see mechanical outline)	2.03 X 3.84 X 7.50 inch (52 X 98 X 191 mm)			

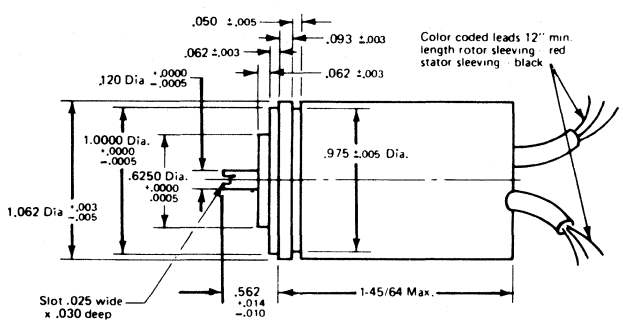
PIN ASSIGNMENTS

PIN	API-30602	API-30603	API-30604	API-30605	API-30606	API-30607	API-30608	API-30609
1	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd
2	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd
3	Connect to 27 for 26V L-L		NC	NC	Connect to 27 for 26V L-L		NC	NC
4	Converter Busy		Converter Busy		Converter Busy		Converter Busy	
5	Connect to 27 for 11.8V L-L		NC	NC	Connect to 27 for 11.8V L-L		NC	NC
6	Ref Lo	Ref Lo	Ref Lo	Ref Lo	Ref Lo	Ref Lo	Ref Lo	Ref Lo
7[1]	6V AC Ref Hi Out		6V AC Ref Hi Out		6V AC Ref Hi Out		6V AC Ref Hi Out	
8	Ref Hi	Ref Hi	Ref Hi	Ref Hi	Ref Hi	Ref Hi	Ref Hi	Ref Hi
9	NC	NC	NC	NC	NC	NC	NC	NC
10	.1	.1	.1	.1	.1	.1	.1	.1
11	.01	.01	.01	.01	.01	.01	.01	.01
12	.2	.2	.2	.2	.2	.2	.2	.2
13	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
14	.4	.4	.4	.4	.4	.4	.4	.4
15	.02	.02	.02	.02	.02	.02	.02	.02
16	.8	.8	.8	.8	.8	.8	.8	.8
17	100	100	100	100	100	100	100	100
18	.04	.04	.04	.04	.04	.04	.04	.04
19	S3′	S3′	NC	NC	S3′	S3′	NC	NC
20	Disable .1° Decade		Disable .1° Decade		Disable .1° Decade		Disable .1° Decade	
21	NC	NC	NC	NC	NC	NC	NC	NC
22	Digital Gnd	Digital Gnd	Digital Gnd	Digital Gnd	Digital Gnd	Digital Gnd	Digital Gnd	Digital Gnd
23	200	200	200	200	200	200	200	200
24	8	8	8	8	8	8	8	8
25	Disable 100° Decade		Disable 100° Decade		Disable 100° Decade		Disable 100° Decade	
26	20	20	20	20	20	20	20	20
27	L-L Programming		S1, S4 (Resolver Input) (-Sin, -Cos)		L-L Programming		S1, S4 (Resolver Input) (-Sin, -Cos)	
28	4	4	4	4	4	4	4	4
29	.08	.08	.08	.08	.08	.08	.08	.08
30	40	40	40	40	40	40	40	40
31	Dimmer Option	Dimmer Option	Dimmer Option	Dimmer Option	Dimmer Option	Dimmer Option	Dimmer Option	Dimmer Option
32	2	2	2	2	2	2	2	2
33	Disable .01° Decade		Disable .01° Decade		Disable .01° Decade		Disable .01° Decade	
34	80	80	80	80	80	80	80	80
35	+5V Dimmer Option		+5V Dimmer Option		+5V Dimmer Option		+5V Dimmer Option	
36	1	1	1	1	1	1	1	1
37	$\overline{LT}$ (Lamp Test)		$\overline{LT}$ (Lamp Test)		$\overline{LT}$ (Lamp Test)		$\overline{LT}$ (Lamp Test)	
38	10	10	10	10	10	10	10	10
39	S	S	NC	NC	S	S	NC	NC
40	Disable 1° Decade		Disable 1° Decade		Disable 1° Decade		Disable 1° Decade	
41	S1 (Synchro/Resolver Input)		NC	NC	S1 (Synchro/Resolver Input)		NC	NC
42	Disable 10° Decade		Disable 10° Decade		Disable 10° Decade		Disable 10° Decade	
43[2]	Power Lo	Power Lo	Power Lo	Power Lo	Power Lo	Power Lo	Power Lo	Power Lo
44	S3 (Synchro/Resolver Input)		S3 (+Sin/Resolver Input)		S3 (Synchro/Resolver Input)		S3 (+Sin/Resolver Input)	
45	26V Power Hi	26V Power Hi	26V Power Hi	26V Power Hi	100V Power Hi	100V Power Hi	100V Power Hi	100V Power Hi
46	S4 (Resolver Only)		NC	NC	S4 (Resolver Only)		NC	NC
47	115V Power Hi	115V Power Hi	115V Power Hi	115V Power Hi	220V Power Hi	220V Power Hi	220V Power Hi	220V Power Hi
48	S2 (Synchro/Resolver Input)		S2 (Resolver Input:+Cos)		S2 (Synchro/Resolver Input)		S2 (Resolver Input:+Cos)	
49	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd	Chassis Gnd
50	SS	SS	NC	NC	SS	SS	NC	NC

Notes:
(1) Used only for API-30604/8 and -30605/9.
(2) Chassis Gnd (Pin 1,2 or 49) should be connected to Power Lo (pin 43).
(3) Connections required for optional operating configurations are described in our API-30602 Series Instruction Manual.

SHAFT ANGLE TRANSDUCER OPTION

API-30604/05/08/09 are dedicated units to be operated at 2V line-line resolver signal. The reference input of 6V to the resolver is provided by the panel meter. Any standard 400 Hz, 26V/12.6V or 26V/11.8 resolver can be used. A standard 6 minute resolver is available from DDC: Order P/N 521000140000



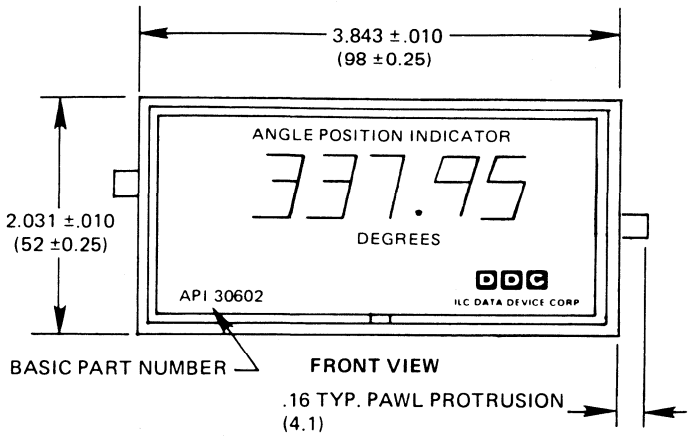
RESOLVER CONNECTION TABLE FOR API-30604/05/08/09

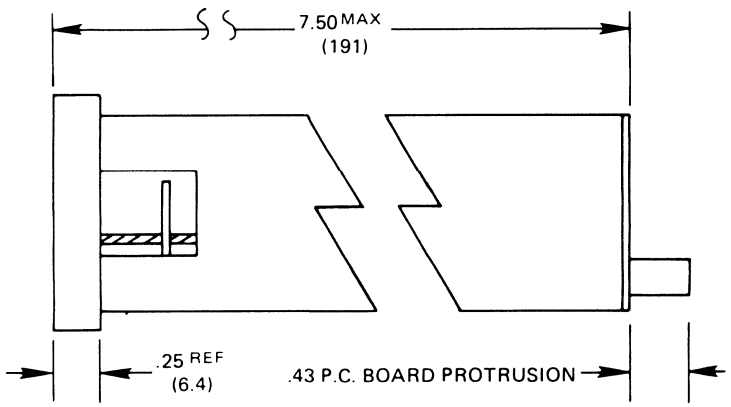
RESOLVER LEADS		PANEL METER CONNECTOR	
SYMBOL	COLOR	CONNECT TO PIN NO.	FUNCTION
R1	RED/WHITE	JUMPER 7	6V HI
R3	BLACK/WHITE	JUMPER 8	REF HI
R2	YELLOW/WHITE	JUMPER 43	POWER LO
		JUMPER 6	REF LO
S1	RED	27	-SIN
S2	YELLOW	48	+COS
S3	BLACK	44	+SIN
S4	BLUE	27	-COS

NOTE: This connection is for CCW rotation of the resolver for increasing angle sense. For CW rotation, representing increasing angle, interchange S1 and S3.

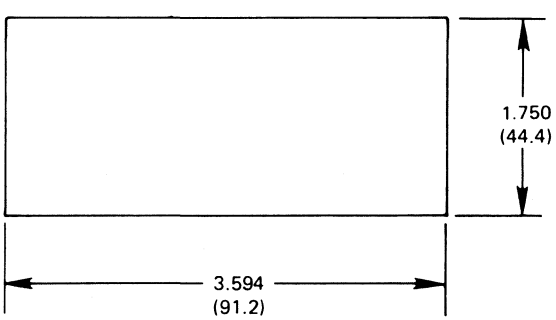
MECHANICAL OUTLINE

NOTE: Dimensions are in inches (millimeters)

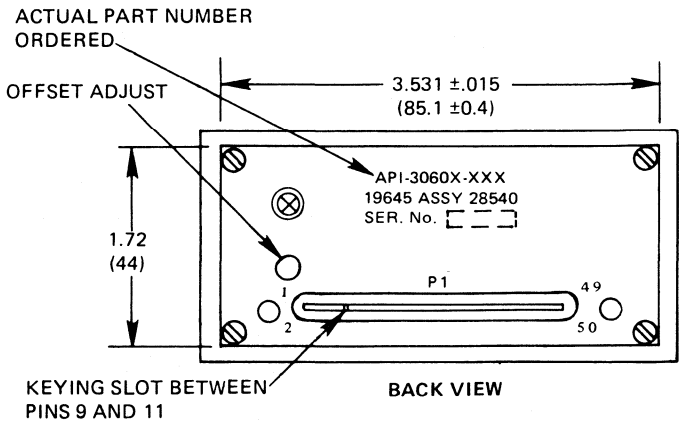




SIDE VIEW



MOUNTING CUTOUT



MOUNTING PROCEDURE

1. Cut out mounting hole.
2. Removing lens: insert screwdriver into notch at the bottom of the bezel and gently pry out lens.
3. Insert Panel Meter into cutout.
4. Retract pawls to rear position by turning screws counter clockwise.
5. Lock Panel Meter into position by turning screws clockwise.
6. Replacing lens: Slightly bend lens and snap into side channels of bezel.

ORDERING INFORMATION

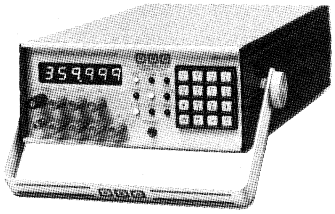
API – 3060X – 3 0 X

- Accuracy:
  - 1 = ±0.05°
  - 2 = ±0.03°
- Input:
  - 0 = Standard
- Temperature Range (operating):
  - 3 = 0°C to +70°C
- Options:
  - 2 = 115V Standard
  - 3 = 115V Dimmer option
  - 4 = 115V Transducer option (note 3)
  - 5 = 115V Dimmer and transducer options
  - 6 = 220V Standard
  - 7 = 220V Dimmer option
  - 8 = 220V Transducer option (note 3)
  - 9 = 220V Dimmer and transducer option
- Family Code

NOTES:

1. All instruments are supplied with mating connector, keying plug, and connector locking hardware.
2. Additional connectors and keying plugs may be ordered as follows:
   Connector: P/N 5313 3300 0000
   Keying Plug: P/N 5313 3400 0000
3. Standard 6 minute resolver for use with API-30604/05/08/09 may be ordered separately as P/N 15760.

SIM-31200 SERIES



SYNCHRO AND RESOLVER ANGLE SIMULATORS

DESCRIPTION

The SIM-31200 Series are high quality synchro and resolver simulators, which incorporate microprocessor control of digital input multiplexing, front panel display, internal 20-bit digital to resolver converter and status/fault flag outputs. The internal 20-bit binary converter provides resolution of .001° BCD or .00034° binary, with accuracy up to ±.003° (10 arc seconds). The angle input may be entered locally via the keyboard, or remotely through the rear panel parallel data connector. The remote input format (BCD or binary) is selectable via a rear panel switch. An optional IEEE-488 interface is available for using the SIM-31200 with instruments connected to a General Purpose IEEE Parallel Data Bus.

The front panel keyboard is for local programming of output formats, increment/decrement, output voltage levels, angle entry and calibration/test functions.

The reference input (26 or 115V rms) is broadband (47 Hz to 11 KHz) and may be supplied to the rear panel connector or front panel terminals.

The outputs are transformer isolated synchro or resolver signals programmable to 11.8, 26, or 90V rms line-to-line.

The microprocessor provides control for analog signal output formats and levels. In addition, the microprocessor works in conjunction with a nonvolatile memory and a counting circuit to measure the reference frequency which is used to generate a digital correction and calibration scheme.

The instrument is powered by 115V or 230V rms, and has internal EMI/RFI filtering. Bench top and rack mounted configurations with or without front panel keyboard or display are available.

APPLICATIONS

Applications for SIM-31200 Series include production testing, quality control inspections and laboratory instrumentation. Due to its I/O flexibility, the SIM-31200 functions well for testing navigation equipment, antenna position and calibration systems.

FEATURES

- *5 VA DRIVE CAPABILITY*
- *HIGH ACCURACY:*
  ±.003° NO LOAD
  ±.008° FULL LOAD
- *WIDEBAND: 47 Hz TO 11 KHz*
- *IEEE INTERFACE (OPTIONAL)*
- *PROGRAMMABLE OUTPUT STANDARD SYNCHRO AND RESOLVER LEVELS*
- *OVERLOAD PROTECTED*
- *DIGITAL CALIBRATION FOR IMPROVED MAINTAINABILITY*

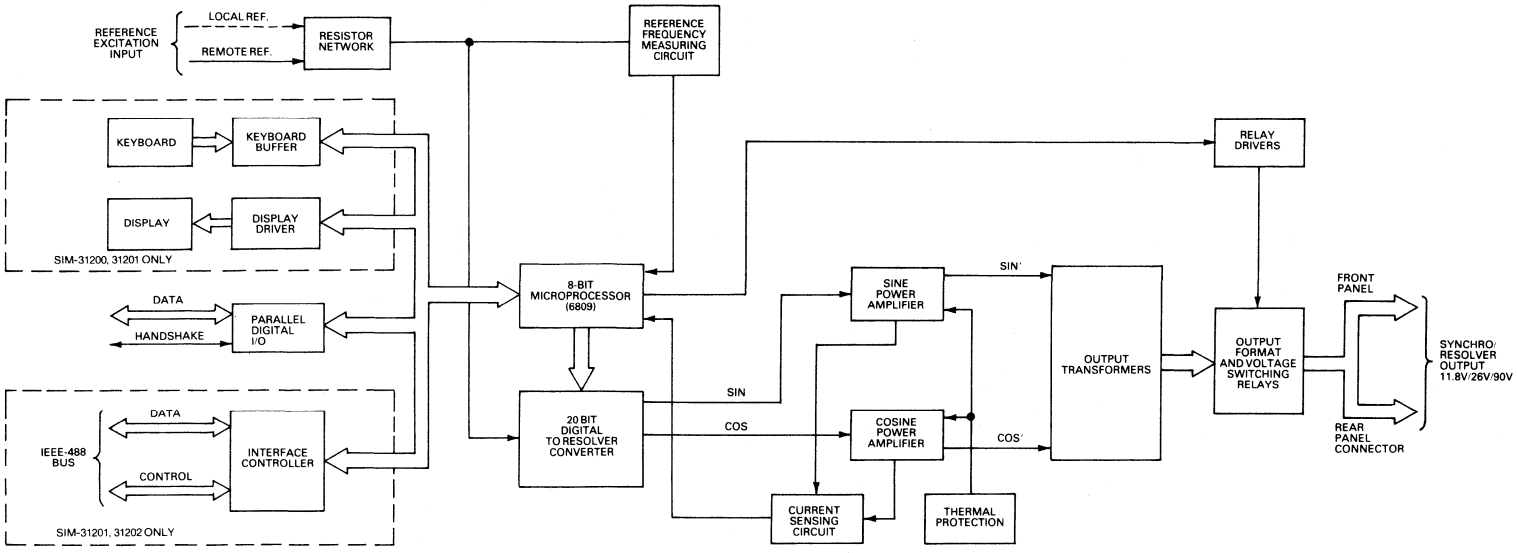


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Apply over temperature range, ±10% reference voltage and frequency variation, and ±10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	.001° BCD; .00034° Binary
ACCURACY*	
47Hz-2KHz	±.003° (no load); ±.004° 1.5VA load; ±.008° 5VA load
10KHz	±.015° (no load); ±.03° 1.5VA load.
*Accuracy degrades as a linear function of frequency from 2KHz to 11KHz. For higher accuracy consult factory	
ANGLE RANGE	000.000° To 359.999° (BCD) 000.000° To 359.99966° (Binary); continuous rotation
DISPLAY	
Output Angle	6-digit, 7-segment LED with polarized filter
Status Indications	Local, Remote, Synchro, Resolver, 11.8V, 26V., 90V., Overload, Reference Missing LEDs.
DIGITAL INPUT/OUT	
Parallel I/O	TTL Compatible
Type	Open = Logic 1; Ground = Logic 0
Inputs	
Loading	1 LS TTL Load
BCD/Binary	Switch selectable format; 22 data lines;
Angle Input	6 decades BCD, or 20-bit binary; 200°, 100°, 180/80°, 90/40°, 45/20°, 22.5/10°, 11.25/8°, 5.625/4°, 2.812/2°, 1.406/1°, .703/.8°, .351/.4°, .176/.2°, .088/.1°, .044/.08°, .022/.4°, .011/.2°, .0055/.01°, .0027/.008°, .0014/.004°, .00069/.002°, .00034/.001°
Other Inputs	Synchro/$\overline{\text{Resolver}}$, 11.8 volt, $\overline{\text{90 volt}}$, Data Track/$\overline{\text{Hold}}$, $\overline{\text{MPU Reset}}$
Outputs	
Drive Capability	5 Standard TTL loads
Signal	Reference Missing, Overload, Parallel Input $\overline{\text{Ready}}$, Binary/$\overline{\text{BCD}}$, GPIB/$\overline{\text{Parallel}}$
GPIB IEEE Interface	Optional, See Below
REFERENCE INPUT	
Input Type	Transformer Isolated
Voltage Levels	26 VRMS/115 VRMS; Others Special: Consult Factory
Frequency	47Hz.-11KHz.
Input Impedance	26V-50K min.; 115V-230K min.
Harmonic Content	10% maximum allowable
Location	Through either front panel or rear connector for both local and remote modes.
Max. Allowable Voltage	
Operating	127V for 115V nominal 29V for 26V nominal
Max. Allowable Voltage No Damage	35V for 26V nominal 150V for 115V nominal
Breakdown Voltage	±500 VDC to Logic Ground
FACTORY CALIBRATION FREQUENCIES & RANGES	
Synchro	90V, 47-150Hz (Cal at 60Hz); 151-1000Hz (Cal 400Hz); 11.8V-151-2000Hz (Cal at 400Hz)
Resolver	11.8V-151-2000Hz (Cal at 400Hz), 2000Hz-11KHz (Cal at 10KHz) 26 and 90V-151-2000Hz (Cal at 400Hz)
User calibration frequencies	Anywhere within specified ranges.

PARAMETER	VALUE
SYNCHRO/RESOLVER OUTPUT	
Type of Output	Synchro (S1, S2, S3 outputs) or resolver (S1, S2, S3, S4 outputs) with transformer isolation.
Line-to-Line Output Voltages	Programmable 11.8. 26 and 90 VRMS ±0.5% nominal due to all causes
Output Locations	Front Panel and rear connector, active in both local and remote modes.
Minimum L-L Load impedance Z_{L-L}	$90V_{L-L}$ / $26V_{L-L}$ / $11.8V_{L-L}$
Synchro (47-2000Hz)	1215 ohms / - - / 21 ohms
Resolver (47-2000Hz)	1620 ohms / 135 ohms / 28 ohms
Resolver (2-11KHz)	—— / —— / 93 ohms
Drive capability	Will drive loads with any phase angle from −90° to +90°.
Time phase	±.4° max, up to 2 KHz; ±1° at 11KHz with respect to reference input
Scale factor variation	±.025% simultaneous amplitude variation in all output lines as a function of digital angle
Protection	Momentary and continuous overcurrent protection; Output overload and reference input missing indications to user; Over temperature shutdown protection
Breakdown voltage	±500 VDC to GND
RESPONSE TIME	20ms. max. upon receipt of input from parallel I/O or IEEE bus.
WARM UP TIME	30 sec. max.
FRONT PANEL CONTROLS	
Power	On/Off switch
Keyboard	Local/Remote, Synchro/Resolver, 11.8/26/90 volt Lamp Test, Angle "Delta" Entry, Increment/Decrement Angle, clear entry, decimal point, calibrate, angle entry
FRONT PANEL I/O	Reference Input (115R, 26R, RL): Synchro/Resolver Output (S1, S2, S3, S4); Case Ground; Digital Ground
REAR PANEL	
Connectors	J1 (50-Pin Analog/Digital I/O) Standard** J2 (24-pin GPIB I/O) optional** J3 (3-pin Power)
Control Switches	GPIB/Parallel (Optional) BCD/Binary GPIB Address-5 bits (Optional) 115/230 volt-Power Input
POWER INPUT	
Connector	Rear Connector including internal EMI/RFI filter; separate line cord supplied
Voltage	Switch selectable 115/230V rms ±10%
Power frequency	47 to 440Hz
Fuse (on rear panel)	Buss, GMW-2, 2 Amp
Isolation	Transformer
PHYSICAL CHARACTERISTICS	
Size	8 1/8 x 3 1/2 x 14 1/2 Inches (20.6 x 8.9 x 36.8 cm.)
Weight	14 lbs (6.4 kg.)
Mounting**	Half-rack; full-rack
TEMPERATURE RANGE	
Operating	0° to 50°C
Storage	−65°C to +100°C

**See Ordering Information

TECHNICAL INFORMATION

INTRODUCTION

The SIM-31200 Series Simulator is a third generation unit featuring μP control and calibration. It is available in three configurations:

1. SIM-31200 is the standard bench top unit with front panel controls and a parallel digital output at the rear for remote operation.
2. SIM-31201 is the same as the SIM-31200 but with optional IEEE GPIB interface.
3. SIM-31202 is a unit optimized for ATE applications. It has a blank front panel to prevent inadvertent operation. The interface is solely through the rear panel IEEE GPIB port or parallel digital I/O.

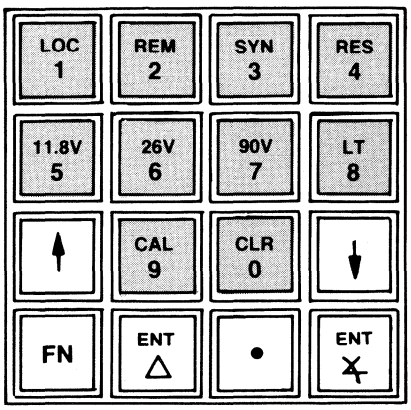
All versions may be bench operated or rack mounted with appropriate mounting hardware.

KEYBOARD OPERATION

Local operation of the SIM-31200 Series is through a 16 pad keyboard, which allows for selection of operating mode, output level and format, test and calibration functions, six digit numerical angle programming, digital angle input enable and angle increment/decrement with programmable delta angle. The keyboard has 10 dual-function keys (highlighted in grey in Figure 2) which are identified by the presence of numerals in the lower case position. The remaining keys are single function keys. A description of the keyboard functions is provided in Table 1.

FRONT PANEL CONNECTIONS

Front panel signal output terminals (S1, S2, S3 and S4) permit direct access to selected signal levels in synchro or resolver format. The reference input terminals may be used for local or remote operation to provide the instrument with 115V or 26V reference excitation. Care must be taken to operate with only *one* reference source (rear connector or front panel terminals). Accidental duplication of reference input signals will not damage the instrument, but will cause errors in angular information in the display (SIM-31200 and SIM-31202) and synchro and resolver outputs on all models.



Indicates dual function key

FIGURE 2. SIM-31200 SERIES KEYBOARD (LOCAL OPERATION)

CALIBRATION

The internal microprocessor operates in conjunction with a non-volatile RAM and the reference measuring circuit (Figure 1) to implement a calibration scheme. This allows compensation for angular errors caused by the output transformers. The procedure will allow calibration to a total error that is equal to or less than ±.003°. A detailed calibration procedure is in the Instruction Manual supplied with each instrument.

KEYBOARD FUNCTIONS

KEY-BOARD PAD	FN ENABLED FUNCTION*	FUNCTION**
FN	When depressed, enables user to select upper functions of the dual function keys.	N/A
LOC 1	Selects local mode.	Enters numerical value of "1".
REM 2	Selects remote mode.	Enters numerical value of "2".
SYN 3	Selects synchro output.	Enters numerical value of "3".
RES 4	Selects resolver output.	Enters numerical value of "4".
11.8V 5	Selects 11.8V output level.	Enters numerical value of "5".
26V 6	Selects 26V output level.	Enters numerical value of "6".
90V 7	Selects 90V output level.	Enters numerical value of "7".
LT 8	Initiates lamp test for approximately 1 second displaying 888.888 and causing all front panel indicators to light.	Enters numerical value of "8".
▲	N/A	Increments input angle by the delta value.
CAL 9	Used for instrument calibration.	Enters numerical value of "9".
CLR 0	Clears angular display.	Enters numerical value of "0".
ENT ▲	N/A	Enters selected delta angle into instrument
▼	N/A	Decrements input angle by delta value.
ENT ✕	N/A	Enters displayed angle into instrument
•	N/A	Enters numerical value representing a fractional part of an angle entry.

*FN enabled functions are called out in red alphanumerics and are collocated with angle entry digits, which are blue.

**Functions are activated after FN configuration has been selected.

DIGITAL PARALLEL I/O

Operating any of the Simulator models through the rear parallel digital I/O port requires that the instrument be connected according to the connection scheme shown in the Parallel I/O (J1) Pin Function Table. The user must also position the rear panel switch (PRL) to select the parallel interface and then select the proper angle format with the Binary or BCD (BIN/BCD) switch. The user must manually set the remote mode, since all models, except the SIM-31202, initialize to the local mode when power is turned on.

PARALLEL I/O J1 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	Spare Pin	17	.0027/.008°	38	DATA T/$\overline{H}$ Handshake Input
2	Spare Pin	18	115R } Remote Ref		"1" = Track Parallel Angle Input Data
3	Case GND	19	RL } Input		"0" = Hold Parallel Angle Input Data
4	J1 Return	20	26R }	39	BIN/$\overline{BCD}$
5	SYN/RES Input(1)	21	GPIB/$\overline{PARALLEL}$ Input/Output(4)		"0" = Binary I/O
	"1" = Synchro	22	Signal Output Programming(2)		"1" = BCD I/O
	"0" = Resolver	23	NU/100°	40	NU/200°
6	Output Level Programming(2)	24	180/80°	41	45/20°
7	90/40° (3)	25	1.406/1°	42	2.812/2°
8	22.5/10°	26	11.25/8°	43	.352/.4°
9	5.625/4°	27	.088/.1°	44	Spare
10	.703/.8°	28	$\overline{Spare}$	45	Analog GND
11	$\overline{.176/.2°}$	29	$\overline{REF\ MISSING\ Output}$	46	Converter SIN
12	$\overline{MPU\ RESET}$ Input	30	$\overline{PARALLEL\ INPUT\ RDY\ Output}$(1)	47	Converter COS
	"1" = Normal Operation	31	Spare	48	.044/.08°
	"0" = Resets Microprocessor	32	.0055/.01°	49	Spare
13	OVERLOAD Output	33	.0014/.004°	50	.0003/.001°
	"1" = Overcurrent Sensed	34	S2		
	"0" = No Overcurrent	35	S3 } Synchro/Resolver		
14	.022/.04°	36	S4(5) } Output		
15	.011/.002°	37	S1 }		
16	.0007/.002°				

Notes: (1) Pins used in all parallel I O modes only.
(2) Signal output programming is as follows:

J1-6 Logic	J1-22 Logic	L-L Voltage Level
"0"	"0"	90 Volts
"0"	"1"	26 Volts
"1"	"0"	Illegal
"1"	"1"	11.8 Volts

(3) J1 Connector pins 7-11, 14-17, 23-27, 32-33, 40-43, 48 and 50 are Binary/BCD (NU = not used Binary)
(4) Switch Selectable (rear panel)
"1" = IEEE-488 Bus controlled
"0" = Parallel I/O controlled
(5) S4 used for resolver operation only.

REMOTE OPERATION VIA THE IEEE GPIB

When operating via the IEEE-488 Interface, a remote mode command signal is provided by the Interface (SIM-31201 and SIM-31202). The front panel indicator lights will illuminate, even though the instrument is controlled remotely (except SIM-31202). They will function as if in the local operating mode, by indicating synchro or resolver signal output and line-to-line voltage level. In the event of a fault condition, such as current overload or reference voltage drop below 5V rms (26V reference) or 22V rms (115V reference) the front panel lights (OVLD or REF LOSS) will illuminate in either local or remote mode.

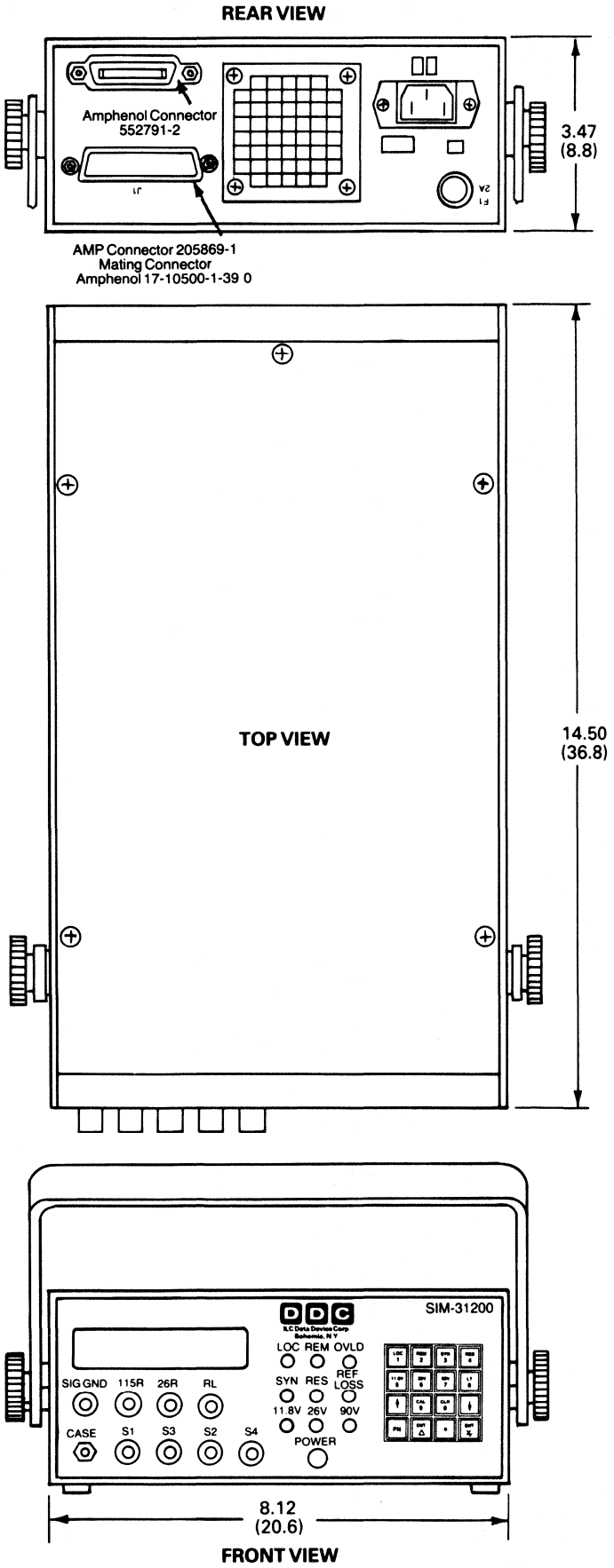
The SIM-31202 requires that all signals access the device through the J1 Interface Connector (rear panel). The user must further insure that the rear panel function switches are set for proper signal and power input (see Mechanical Outline). If operating SIM-31201 or SIM-31202 with IEEE-488 General Purpose Interface Bus (GPIB), the user must program the appropriate 5-digit device address, select the GPIB position and BCD or Binary code on the rear panel to facilitate communication via the IEEE-488 data bus. All GPIB signals are provided to the J2 Interface Connector with the exception of the Reference input, which must be supplied through the J1 Connector or the appropriate front panel binding post.

IEEE-488 PIN FUNCTIONS

Pin	Function
1	D101 Data I/O Line
2	D102 Data I/O Line
3	D103 Data I/O Line
4	D104 Data I/O Line
5	EOI
6	DAV
7	RFD
8	DAC
9	IFC
10	SRQ
11	ATN
12	Case GND
13	D105 Data I/O Line
14	D106 Data I/O Line
15	D107 Data I/O Line
16	D108 Data I/O Line
17	REN
18-24	GND

MECHANICAL OUTLINE

Dimensions in inches (centimeters).



DRIVE CAPABILITY

SIM-31200 Series Simulators can drive up to 5 VA over the frequency range of 47 Hz to 2 kHz and 1.5 VA at frequencies up to 10 kHz. When driving tuned loads the tuning capacitors should not exceed .01μF on 90 V L-L synchros or resolvers, .15μF on 26V L-L resolvers, .75μF on 11.8V L-L synchros or resolvers or .4μF on 11.8V resolvers operating over 2 kHz. These are beyond the range of most tuning capacitors and so should not be a problem.

ORDERING INFORMATION

All instruments are supplied with detachable line cord, mating connector (J1) and instruction manual.

SIM-31200

└ Options:

- 0 = Bench top with keyboard
- 1 = Bench top with keyboard and IEEE-488
- 2 = Blank front panel with IEEE-488

Notes:

1. SIM-31200 and SIM-31201 are supplied with carry support handle. For ½ rack mounting brackets order P N 33395. For full rack mounting brackets order P N 33396.
2. SIM-31202 is supplied with ½ rack mounting brackets. For full rack mounting brackets order P N 33396.

DDC
ILC DATA DEVICE CORPORATION

SOLID STATE SELSYN™ INDICATOR
Programmable Microcomputer Based Indicator

DESCRIPTION

The SPI-30800 is the first microcomputer based Solid State Selsyn Indicator to replace electromechanical (EM) Selsyn torque receivers driving mechanical productimeters or encoders. Solid state circuitry and oil-tight construction provides long term reliability and accurate operation in heavy industrial areas such as the steel, aluminum, copper and paper mill industries. The large viewable 5 decade, .8 inch light emitting diode (LED) display and "up/ down" count indicators permit ideal local remote viewing.

The SPI-30800 interfaces directly to a Selsyn (Synchro) transducer and its associated reference, from which it will obtain shaft angle data and derive its operating power. The instrument fully accommodates field programming of the scale factor, scale factor multiplier for extended range, decimal position and preset number to fit a variety of applications.

The internal microcomputer features a built-in on line self test, which extensively exercises key functions of the instrument. In addition to having built-in voltage transient protection, the unit is also equipped with power interrupt and automatic restart circuitry, which will detect short power outages so that correct position data will be preserved (Figure 1).

The SPI-30800 is available with a wide complement of options; such as a two wire serial output, parallel digital output and an interface for remote preset number programming. Also available is a remote indicator, which interfaces with the serial output of the SPI-30800. It will facilitate remote position indication and interface with control systems or computers with an optional parallel digital output. These options and accessories for remote reporting and control allow for improvements in industrial control systems at an attractive price.

APPLICATIONS

The SPI-30800 can be used in virtually any rugged industrial application requiring an accurate display control, or computer interface. One application is the position display of roller gap or side guide opening in cold or hot strip steel mills. The SPI-30800 can output position information as required by a computer or process controller. Other examples are monitoring fuel levels in storage tanks or complete replacement of a Selsyn torque receiver-mechanical gearbox- and Gray Code encoder combination. The serial and digital output options permit interface with remote displays, computers and process controllers for complete system automation.

FEATURES

- *RUGGEDIZED: NEMA 12 CONSTRUCTION*
- *RELIABLE: ALL SOLID STATE*
- *BUILT IN TEST*
- *FULLY FIELD PROGRAMMABLE*
- *LARGE LED DISPLAY WITH "UP/DOWN" INDICATORS*
- *OPTIONAL PARALLEL AND/OR SERIAL I/O'S*
- *HIGH TRACKING SPEED 1800 RPM*

Note: Selsyn™ is a trademark of General Electric Corporation.

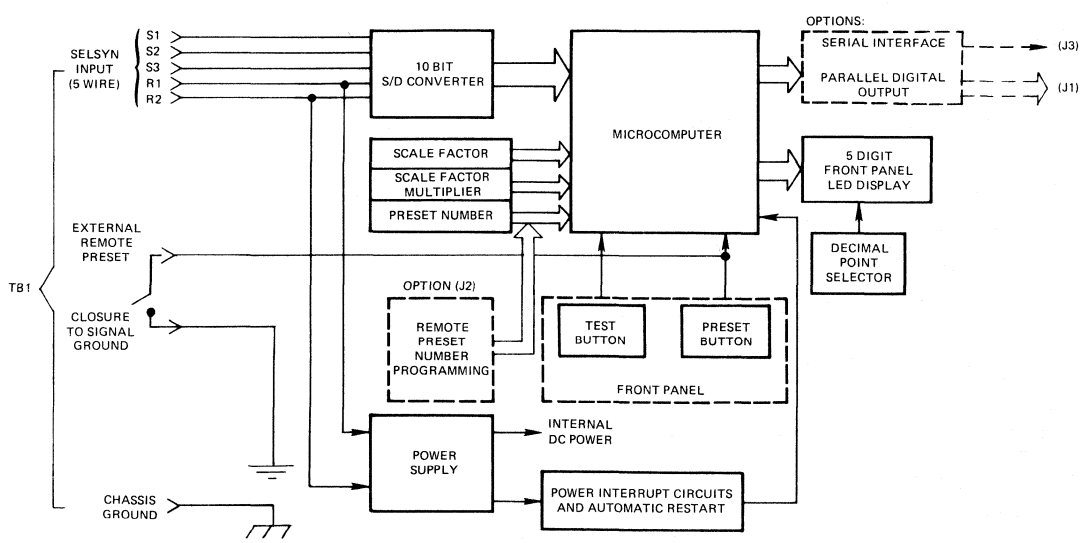


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

PARAMETER	VALUE
DISPLAY	
Type	Roll-over
5 Digits (Red LED)	7 segment (.8 inch high)
Up/Down Indicators	2 LED's
ACCURACY	
Converter	10 bit (Type II tracking) See ACCURACY discussion
SELSYN INPUT	
Signal	
Format	3 wire
Input Impedance	148 kΩ, L-L min
Voltage Range	48 to 90V rms
Reference Input	
Format	2 wire
Input Power	.40 VA max
Frequency	60 Hz
Voltage Range	90 to 130V rms
Tracking	
Speed (1)	30 rps (1800 rpm)
Programming	Internal programming is accomplished with individual 8 position sealed DIP switches
Scale Factor Range	0.0039 to 255.996
Scale Factor Multiplier	8X, 16X, 32X
Decimal Point Position	10's, 100's, 1,000's and 10,000's
Preset Number Range	00000 to 99999
REMOTE PROGRAMMING OPTION	See J2 connection detail
Preset Number	00000 to 99999
Preset Closure (2)	External connection to ground

PARAMETER	VALUE
SERIAL OUTPUT OPTION	
Format	Pulse width modulated, differential, half duplex
Baud Rate	6.25 k BPS
Drive	0.5 mile, typ
DIGITAL OUTPUT OPTIONS	
BCD (Positive Logic)	20 wire plus up/down flags
BCD (Negative Logic)	20 wire plus up/down flags
Binary	17 bit
Gray Code	14 bit
Other Codes (1)	Consult Factory
POWER INTERRUPT CIRCUIT	
Duration	400 msec
BUILT IN TEST DISPLAY	
Display Time	2.5 sec, typ (each display)
Cycle Time	9.2 sec, typ (total of 4 displays)
TEMPERATURE RANGE	
Operating	0°C to +60°C
Storage	−55°C to +105°C
PHYSICAL CHARACTERISTICS	
Size	6.25" x 4.63" x 9" (159 x 118 x 229 mm)
Weight	4 lbs (1.8 kg)

Plus converter busy, and 3-state enable

Notes: (1) Others available upon request.
(2) TB-1, Remote Preset is supplied on all units

TECHNICAL INFORMATION

INTRODUCTION

The Solid State Selsyn Indicator SPI-30800 is designed to connect directly to a Selsyn transducer, via large rear panel terminal screws. The instrument incorporates a DDC solid state tracking Selsyn to digital (S/D) converter which digitizes a Selsyn signal. The tracking characteristics are such that high speeds and accelerations will not cause any degradation of the unit's accuracy. It also greatly extends the life of the Selsyn transducer because of the high input impedance of the S/D. High noise immunity and speed result in a display that precisely indicates mechanical position of the Selsyn in real time.

Internal, dual-in-line switches permit field programming. The instrument can be adapted to various applications because of the scale factor, decimal and preset number programming features. The SPI-30800 features safeguards against improper programming. This includes the Built-In Test (BIT) function, which scans and displays the information internally (or externally) programmed; the preset number fault detection routine which is described in the preset number section.

ACCURACY

SPI-30800 system error is application dependent and is defined by the formula shown. As expressed in this formula, the error consists of two factors. The first factor represents the basic instrument error. The second factor is a cumulative error, which results when the programmable scale factor is different than the exact required scale factor. This cumulative error will be zero or negligible for most applications.

$$\text{SYSTEM ERROR} = \pm K(E_{RO} + E_{S/D}) + \frac{E_{SF}}{SF_{TOT}} (K \cdot TN)$$

WHERE:

K = System displacement per turn

TN = Total number of selsyn turns

E_{RO} (Round-off error) $= \frac{.5}{SF_{TOT}}$ turns; $SF_{TOT} = SF \cdot SFM$

E_{SF} (Scale Factor error) $= SF_{TOT} - SF_{IDEAL}$

$E_{S/D}$ (S/D ERROR) $= .00414$ turns

SF = Scale Factor programmed by internal dip switches

SFM = Scale Factor Multiplier selection

SF_{TOT} = Total Scale Factor programmed including SFM

SF_{IDEAL} = Ideal total Scale Factor calculated

EXAMPLE:

Consider an application with 100 selsyn turns and a scale factor of 8.333. The display for this application must represent position to the nearest hundredth of a foot (000.00). Gearing is such that one selsyn turn equals one inch. Therefore,

K = 1 inch/turn (.08333 ft/turn)

SF_{IDEAL} = 8.333 to display feet in hundredths of a foot

SFM = 1x (no selection required)

SF_{TOT} = 8.3320 (closest that can be programmed)

TN = 100 turns full scale

THEN:

$$E_{RO} = \frac{.5}{8.332} = 6.0009 \times 10^{-2}$$

$E_{S/D}$ = .00414 turns (standard SPI-30800)

$E_{SF} = 8.333 - 8.332 = 1x\ 10^{-3} = .001$

System error = $\pm .08333\ (6.0009 \times 10^{-2} + .00414) + \frac{.001}{8.3320}\ (.08333 \times 100)$

System error = $\pm 5.3455 \times 10^{-3} + 1.0001 \times 10^{-3}$
= ±.0063456 ft. (worst case)

The instrument's displayed position will never vary from its actual displacement by more than this computed system error. In this example the display would still be accurate to within ±1 LSB after 100 turns.

PRESET FRONT PANEL CONTROL

The front panel oil-tight preset button activates the instrument when power is first applied. Once depressed the SPI-30800 will be returned to the internally (or externally) programmed preset number. It is possible to preset multiple instruments simultaneously. This is accomplished by interconnecting the preset control terminals provided on the real panel of the instrument(s). The preset function takes precedence over the BIT function. It is used to enter scale factor and preset number programming changes to the microcomputer.

SCALE FACTOR (SF)

The scale factor (SF) is field programmable so that each rotation of the Selsyn or synchro is converted to display a specific "counts/turn".

The instrument has a roll-over display that will accumulate counts to 99, 999, then go to all zeros or vice versa. Above or below zero display is available as an option. In this option, the standard up/down LED's are used as plus and minus indication.

SCALE FACTOR MULTIPLIER (SFM)

The SPI-30800 is equipped with a field programmable scale factor multiplier. This is for applications where resolution is not critical and a larger scale factor (counts/turn) is required. It is normally 1X and expands the SF by 8X, 16X or 32X, as shown in the following examples:

SAMPLE SCALE FACTOR MULTIPLIER TABLE

SELECTED COUNTS/TURN	SELECTED MULTIPLIER	DISPLAYED COUNTS/ TURN FOR ONE ROTATION
157.500	1X (Normal)	00158
45.0039	8X	00360
255.996	8X	02048
255.996	16X	04096
255.996	32X	08192

PRESET NUMBER

A preset number of zero or any other value can be field programmed by internal dual-in-line switches. This is often required to offset the displayed information. This offset can be useful when the serial or parallel digital output options interface directly with computers or control processors (see Remote Preset Number Option). The SPI-30800 has an internal fault detection routine which will flash any digit programmed to exceed 9.

DECIMAL POINT

The SPI-30800 is programmed by a dual-in-line switch for locating the decimal point after any decade.

BUILT-IN TEST (BIT)

The front panel oil-tight test button, may be energized at any time during operation to indicate the instruments status. Normal operation is not hampered during the test cycle. Preset always has precedence over test.

The BIT sequence is as follows:

1. Display of all 8's and "up/down" indicator LED's to determine operation of all segments.
2. Display programmed preset number.
3. Display programmed integer part of the SF.
4. Display programmed fractional part of the SF.
5. Return to the present real time position.
6. The decimal point is constantly being displayed.

AVAILABLE OPTIONS

REMOTE PRESET NUMBER

A convenient rear panel connector permits interface to external thumbwheel switches or logic, which can be used to externally set the preset number.

DIGITAL OUTPUT OPTIONS

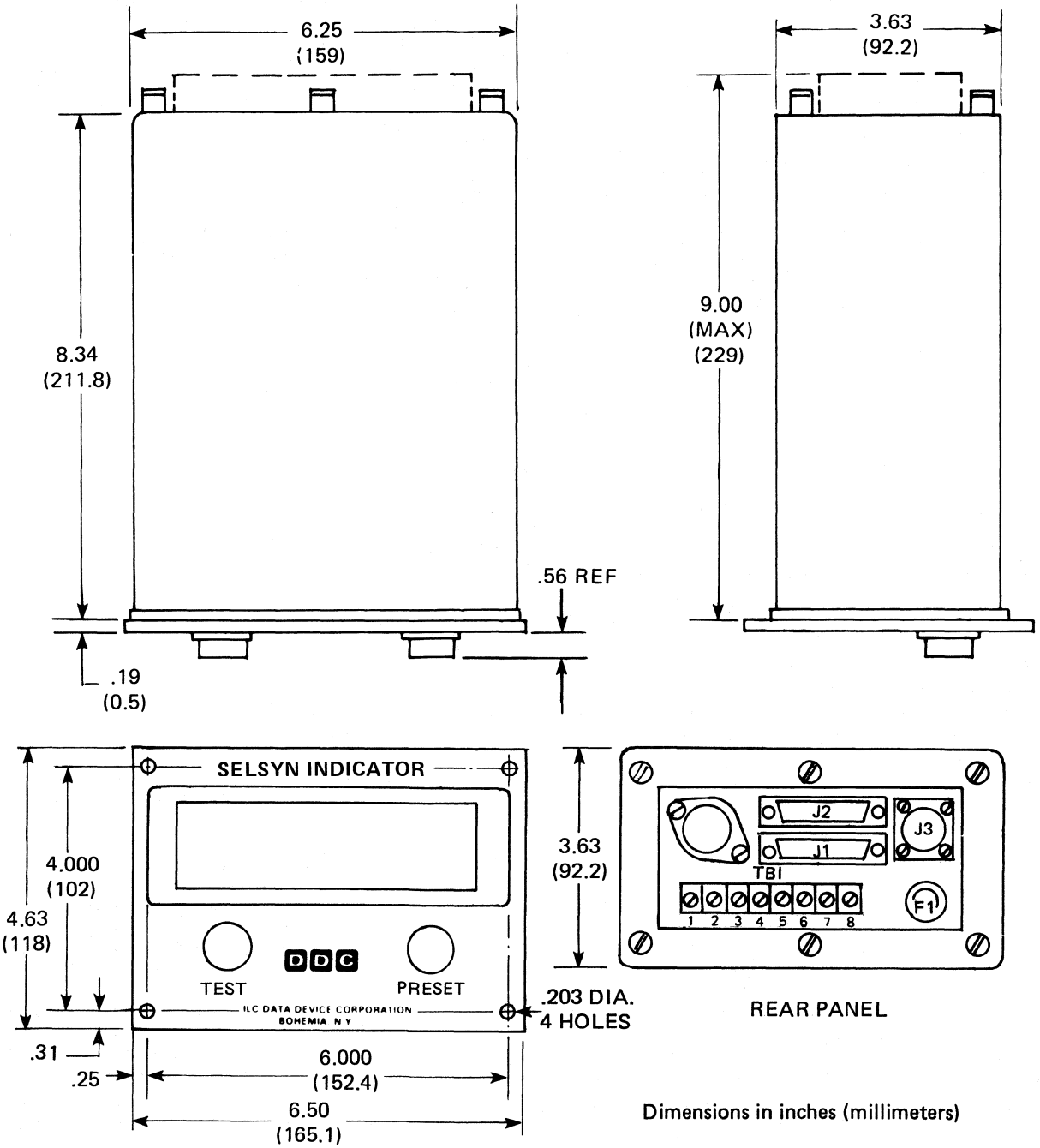
The SPI-30800 has been provided with the capability for an optional "plug-in" digital output module, which interfaces to a rear panel connector. The typical is a parallel, BCD, positive TTL logic, three state output, which includes the up/down flags and converter busy signal. The internal microcomputer and other "plug-in" modules can facilitate a great many output types, such as Binary, Gray Code or other BCD codes as well as inverted or open collector type outputs.

SERIAL OUTPUT

A serial output option was designed for the SPI-30800. It has the capability of driving position information for a half mile over a twisted shielded cable. This is ideal for long runs to remote* indicators or computer rooms. The serial output is a balanced pulse modulated code and is well suited for industrial applications with high EMI environments.

*Intended for use only with DDC remote indicator Model SPI-30880 and SPI-30881.

MECHANICAL OUTLINE



Dimensions in inches (millimeters)

J1 CONNECTOR DIGITAL OUTPUT	
PIN	FUNCTION
J1 – 1	40,000B
2	10,000B
3	4,000B
4	1,000B
5	400B
6	100B
7	40B
8	10B
9	8B
10	UP COUNT FLAG
11	1B
12	GROUND
13	CONVERTER BUSY
14	20,000B
15	8,000B
16	2,000B
17	800B
18	200B
19	80B
20	20B
21	4B
22	2B
23	80,000B
24	DOWN COUNT FLAG
J2 –25	BCD OUTPUT ENABLE INPUT (GND = HI-Z, 5V = ENABLE)

NOTE:
Shown for BCD 3-State TTL Output.

J2 CONNNECTOR EXTERNAL PRESET INPUT OPTION	
PIN	FUNCTION
J2 – 1	N.C.
2	SPARE INPUT 1
3	4,000P
4	PRESET INPUT
5	10P
6	40P
7	1P
8	100P
9	40,000P
10	4P
11	20,000P
12	800P
13	GROUND
14	SPARE INPUT 2
15	2,000P
16	1,000P
17	8,000P
18	20P
19	80P
20	80,000P
21	2P
22	200P
23	8P
24	400P
J2 –25	10,000P

J3 CONNECTOR SERIAL INTERFACE OPTION	
PIN	FUNCTION
J3 - A	SERIAL DATA (+)
J2 - B	SERIAL DATA (–)
J3 - C	SHIELD

TB-1	
TERMINAL	FUNCTION
TB1 -1	RH
2	RL
3	S1
4	S2
5	S3
6	CASE GROUND
7	EXT. PRESET
TB1 -8	SIGNAL GROUND

ORDERING INFORMATION

SPI – 308XX

Parallel output option
- 0 = No parallel output
- 1 = TTL positive logic
- 2 = TTL negative logic
- 3 = Open collector positive logic
- 4 = Open collector negative logic
- 5 = Opto-isolated positive logic
- 6 = Opto-isolated negative logic

Preset/Serial output options

Non Ruggedized
- 0 = No remote preset, no serial output
- 1 = No remote preset, with serial output
- 2 = Remote preset, no serial output
- 3 = Remote preset, with serial output

Ruggedized
- 4 = No remote preset, no serial output
- 5 = No remote preset, with serial output
- 6 = Remote preset, no serial output
- 7 = Remote preset, with serial output

NOTES:
1. Consult factory for other options, such as Binary, Gray Code and above and below zero display.
2. Mating connectors supplied with J1, J2 and J3 options.

SOLID STATE REMOTE SELSYN™ INDICATOR
Used With Master Indicator

DESCRIPTION

The SPI-30880 and SPI-30881 are rugged solid state remote selsyn indicators designed to operate with DDC's microcomputer based master selsyn indicator SPI-30800. These remote indicators provide accurate 5 digit LED display of selsyn data up to one half mile from the master indicator. The data is transmitted by the master to a maximum of 10 remotes via a twisted/shielded pair communication line.

The SPI-30880 operates as a display of the information transmitted to it by the master, while the SPI-30881 has the additional capability of communicating with the master and retransmitting the data in parallel format, from the master to a computer.

APPLICATION

These remote indicators contain conformally coated components and are constructed to meet NEMA 12 requirements for reliability in severe environments. Applications include position display of roller gap or side guide opening in cold or hot strip steel mills.

FEATURES

- *ALL SOLID STATE*
- *NEMA 12 CONSTRUCTION*
- *LARGE LED DISPLAY WITH UP/DOWN INDICATORS*
- *LINKS WITH MASTER VIA 2 WIRE SERIAL DATA LINE*
- *SPI-30881 INCLUDES PRESET AND TEST SEQUENCE COMMAND FUNCTIONS AND PARALLEL DATA OUTPUT*

Note: Selsyn™ is a trademark of General Electric Corp.

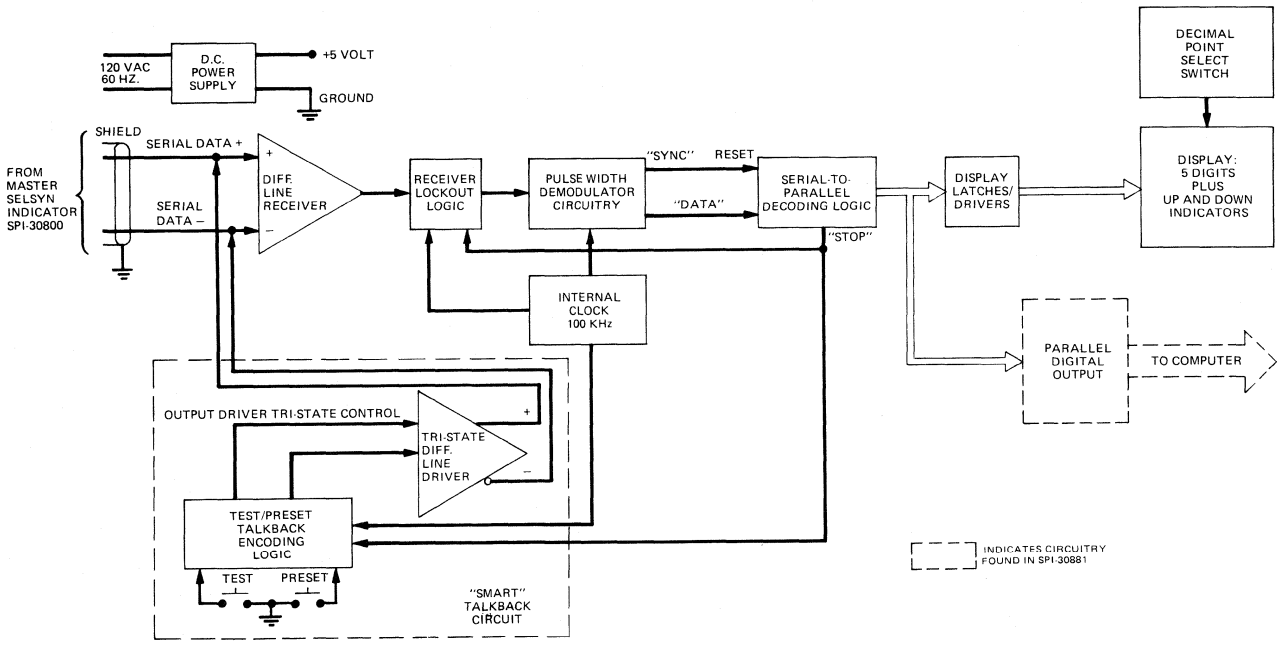


FIGURE 1. BLOCK DIAGRAM SPI-30880/30881

SPECIFICATIONS	
PARAMETER	**VALUE**
DISPLAY	
5 Digits (Red LED)	7 segment (0.8 inch high)
Up/Down Indicators	2 LED's
Decimal Point Position	Programmable
Update Rate	100 Hz
Information Displayed	Position data and up/down indication from master. Test data when master in test mode.
SERIAL DATA	
Communication Line	2 wire twisted/shielded pair
Transmission Format	Half duplex, pulse width modulated data.
Data Rate	6.25K bits per second
Maximum Loading (Slaved from one master)	10 min (including one talkback option max.)
Maximum Distance from master	0.5 mile max
RECEIVER	
Type	Differential TTL
Input Threshold Voltage	±0.05V with V_{cm} = 0 ±1V with V_{cm} = ±15 max
Invert Input Resistance	3.6 kΩ min, 5.0 kΩ typ
Non-Inverting Input Resistance	1.8 kΩ min, 2.5 kΩ typ
DRIVER*	
Type	Differential TTL
Output Voltage	
Logic "1" (I_O = 40 mA)	1.8V min, 2.5V typ
Logic "0" (I_O = 40 mA)	0.5V max, 0.29V typ
PARALLEL DIGITAL OUTPUT OPTION	
Type	
3-state TTL Open Collector Opto-Isolated Open Collector	Consult Factory For Parallel Output Option
Number of Lines	22 parallel lines, Converter Busy and 3-state control input.
Data	Indicates position data from master unit driving both normal operating and test mode.
Format	20 bit positive true BCD and up/down lines (standard)**
Update Rate	100 Hz
Maximum Loading	10 TTL loads
POWER INPUT	110VAC ±20%, 47–440 Hz 115VA, max
PHYSICAL CHARACTERISTICS	
Size	
Case	6.25 x 3.63 x 6 inch (159 x 92 x 152 mm)
Front Panel	6.5 x 4.63 (165 x 118 mm)
Temperature Range	0°C to +70°C

*Specifications apply only to SPI-30881

**Negative true BCD, Binary and Gray Codes are available. This requires a modification to the SPI-30800 master unit only.

TECHNICAL INFORMATION

The remote indicators, SPI-30880 and SPI-30881, are both linked to the master selsyn indicator SPI-30800* via a two wire twisted/shielded communication line.

Interfacing the remotes and the master indicator to the serial transmission line is accomplished with amphenol connector #69-3106E10SL-3P fitted at J1 (remotes) or J3 (master). This connector couples the center conductors and the shield of the "twisted pair" to the serial input of the SPI-30880 or the bidirectional I/O port of the SPI-30881. The communication line should be standard twisted shielded cable such as Belden #8451 (See figure 2).

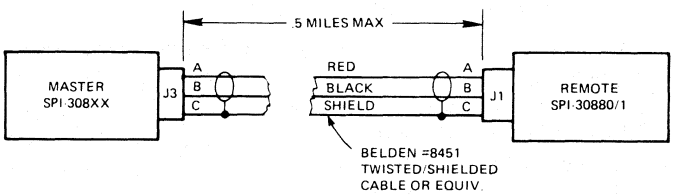


FIGURE 2. INTERCONNECT BETWEEN MASTER AND REMOTE SELSYN INDICATORS

SPI-30881 OPTIONS

The parallel data output, Remote Preset command and Test command functions are standard features of the SPI-30881 remote indicator. The parallel output from the remote indicator is 22 lines of data, Converter Busy and 3-state control. It will always reflect the master indicator's existing position, updated every 10 milliseconds, regardless of what display routine the master is cycling through. This is possible because the master continuously tracks the selsyn and outputs the data via the serial data line every 10 ms in both normal and test modes. For this reason the LED display of both remotes and the master may be interrupted if either the SPI-30881 (remote) or the SPI-30800 (master) initiates a TEST or PRESET Command. The TEST routine consists of sequenced LED display of all 8's and up/down LED's, preset number, programmed scale factor (integer), scale factor (fractional part), master S/D converter position, number of microcomputer interruptions and finally the existing position.

SERIAL I/O

This information to the remote indicators is transmitted in a differential, half-duplex pulse width modulated serial format. Figure 3 illustrates the bit format transmitted over the two-wire twisted/shielded serial data line.

The remote indicators receive their serial information in the following pattern:

The *sync field* may consist of a maximum of three positive-going 140 μs pulses transmitted by the master indicator. If one pulse is received the remotes auto display the data following the sync field (SPI-30881's parallel output will always output existing position data).

*Master indicator SPI-30800 data sheet available upon request.

The presence of two positive-going pulses indicates Test Display Data Sync. The remotes are enabled for the display of predetermined test data supplied by the master indicator. The parallel output of the SPI-30881 is not effected.

The presence of three positive-going sync pulses indicates that the master is updating its position data during the "Test routine". The sync pulse configuration causes the decoded serial to parallel data to be distributed only to the parallel output port. The display continues to cycle the test routine.

The *position data* is transmitted as 20 pulses (4 pulses for each digit). Figure 3 shows the pulse width for logic "0" and "1" (20 μs = "0" and 80 μs = "1").

The 21st data pulse begins the up/down indication sequence, which consists of four pulses, the second of which determines the "down" count (figure 3). The third "up/down" pulse correlates to the up indication. The first and fourth pulses meet the criteria for logic "0" and are intended to have no effect on the display.

Checksum Data is intended to create a system for the remote indicator to check the validity of a received word. The master indicator transmits BCD data and up/down indication data that will vary in the number of logical "1's", based upon the changes in position. It therefore, sets the checksum pulses high or low in compliance with the following guideline: Checksum data when added to the five BCD 4 Bit "nibbles" and up/down data bring the total to zero (0000).

The *stop pulse* is a logic "0" (20 μs), which marks the end of the master indicator's transmission and provides the SPI-30881 with a signal to initiate its transmit sequence (80 μs after stop goes low).

The *talkback function* (SPI-30881) follows the Stop pulse. The communication line goes to a high impedance state for about 40 μs. The SPI-30881 then takes control of the transmission line and after an 80 μs delay it transmits one of the following positive-going pulses:

80 μs pulse width = neither test nor preset command. (The absence of a pulse, when no SPI-30881 is on the line, will also indicate neither test nor preset command.)

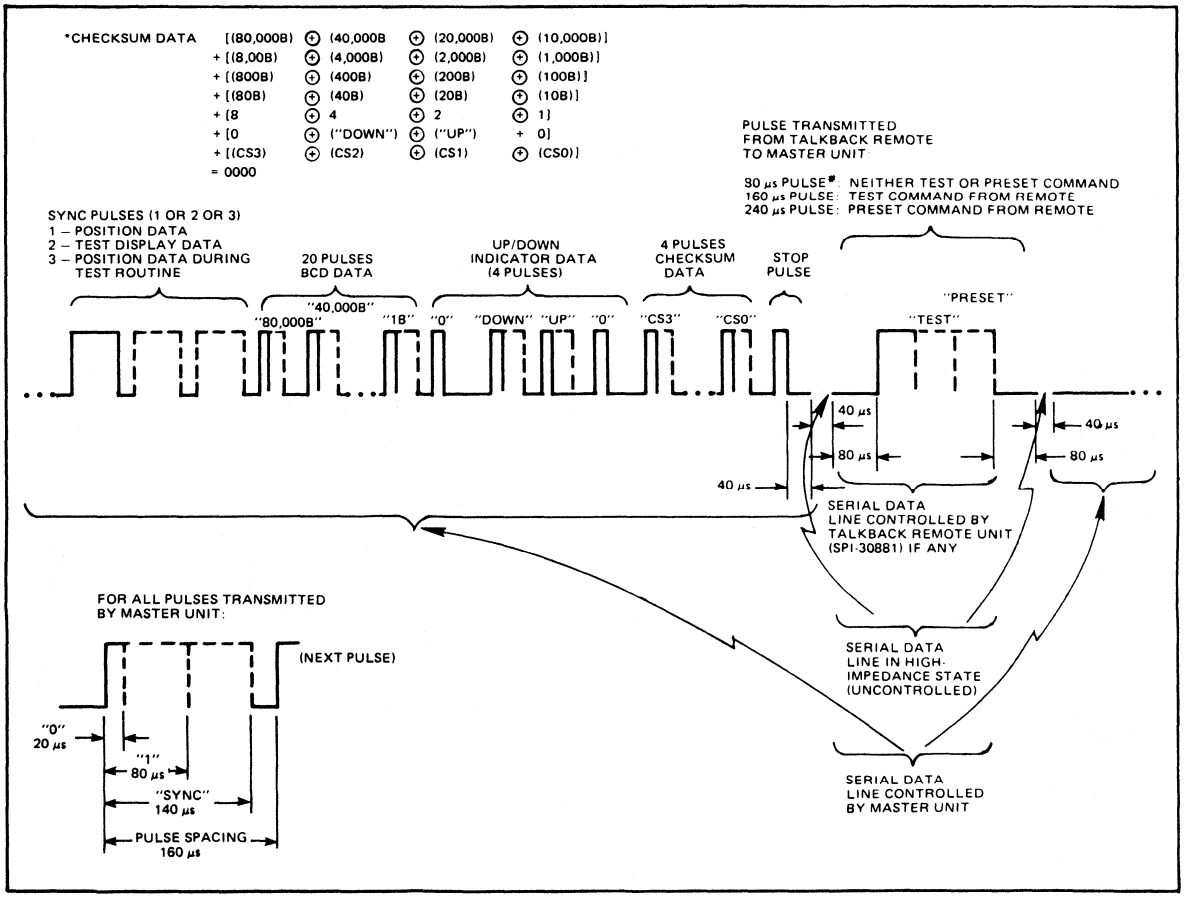
160 μs pulse width = Test command from remote indicator to the master unit.

240 μs pulse width = preset command from remote unit.

All commands from the SPI-30881 are initiated by closure of front panel push buttons (see mechanical outline).

CONVERTER BUSY

A *Converter Busy* signal is internally generated (SPI-30881) when a serial data transmission is received. It consists of a



*OR NO PULSE, IF NO TALKBACK REMOTE UNIT IS ON LINE

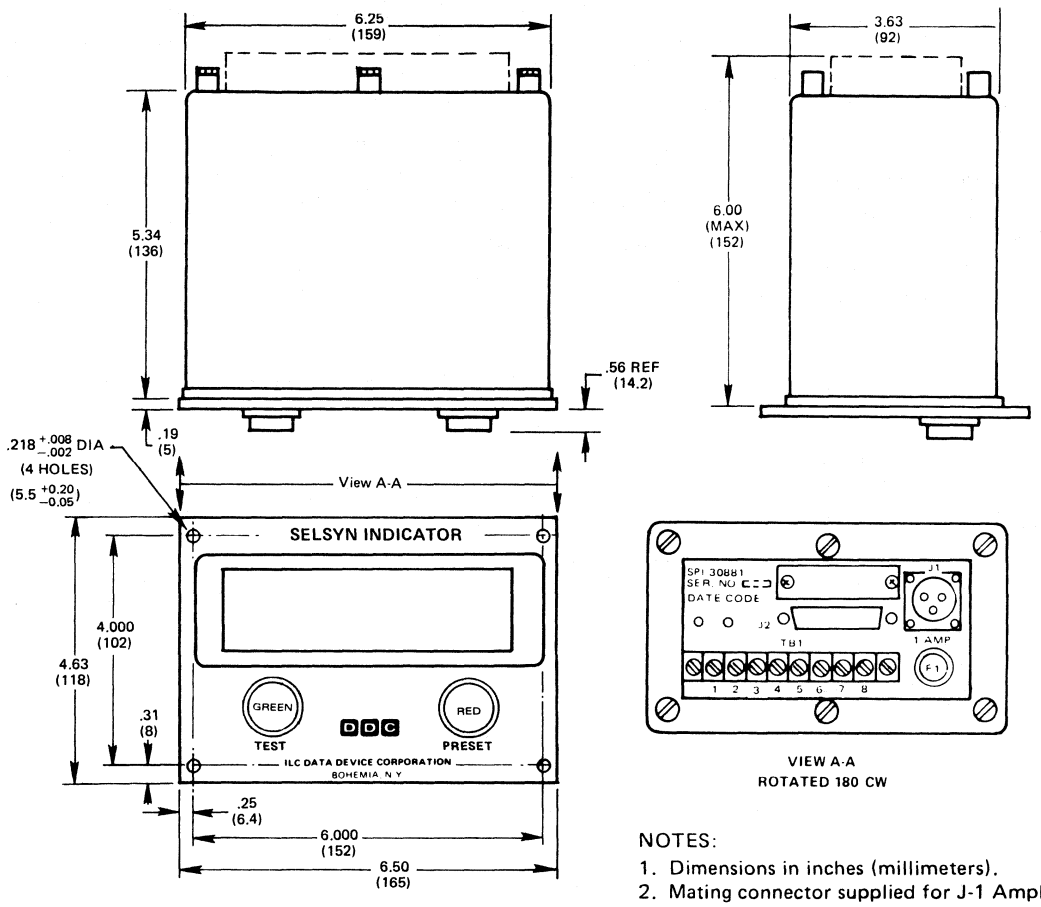
FIGURE 3. SERIAL I/O INTERFACING TIMING.

positive pulse starting at the leading edge of the first Position Data pulse. It remains high until the leading edge of the first checksum data pulse (approximately 4 ms.)

POWER REQUIREMENTS

The SPI-30880 and SPI-30881 require a power input of 100 VAC ±20% @ 47-440 Hz (15 VA max), which must be provided to a rear panel mounted terminal block. A connection table for the eight position terminal block (TB-1) is found in the Mechanical Outline. The power inputs should conform to the polarity shown in this table.

MECHANICAL OUTLINE



J1 CONNECTOR SERIAL I/O	
PIN	FUNCTION
J1-A	SERIAL DATA (+)
J1-B	SERIAL DATA (–)
J1-C	SHIELD

TB-1	
TERMINAL	FUNCTION
TB1-1	120V POWER HI
TB1-2	20V POWER LO
TB1-3	CASE GROUND
TB1-4	SIGNAL GROUND
TB1-5	SHIELD
TB1-6	↕
TB1-7	↕
TB1-8	NC

NOTES:
1. Dimensions in inches (millimeters).
2. Mating connector supplied for J-1 Amphenol #69-3106E10SL-3P

J2 CONNECTOR DIGITAL OUTPUT	
PIN	FUNCTION
J2- 1	40,000B
2	10,000B
3	4,000B
4	1,000B
5	400B
6	100B
7	40B
8	10B
9	8B
10	UP COUNT FLAG
11	1B
12	GROUND
13	CONVERTER BUSY
14	20,000B
15	8,000B
16	2,000B
17	800B
18	200B
19	80B
20	20B
21	4B
22	2B
23	80,000B
24	DOWN COUNT FLAG
J2- 25	BCD OUTPUT ENABLE INPUT (GND=HI-Z; OPEN=ENABLE)

NOTE: Shown for BCD 3-State TTL Output

ORDERING INFORMATION

SPI-3088 X

- Options:
  - 0 = Remote indicator only
  - 1 = Remote indicator with parallel data output and talkback capability.
- Family Code

±.005° SYNCHRO AND RESOLVER ANGLE INDICATOR
Converts Synchro and Resolver Signals to BCD Angle

DESCRIPTION

The SR-103 and HSR-103 are improved high quality angle indicators used in precision synchro and resolver test equipment. They accept synchro or resolver signals at the rear connector and provide BCD angle output which is also displayed on the front panel. Intended primarily for dedicated applications, the SR-103 and HSR-103 are logic programmable via the rear connector and easily interfaced with computers and digital control equipment. An IEEE-488 bus adaptor is a standard option. Because they can accept a broad range of voltages and frequencies without programming and signal-to-reference phase shifts of up to ±50°, the SR-103 and HSR-103 are ideal for situations in which a variety of different inputs must be accommodated quickly.

Using a Type II servo loop for continuous tracking, these instruments have no velocity lag up to the specified tracking rates. There can be no hangup 180° away from the input angle. A fault indicator shows when the unit is not tracking the input signal, and an ambiguity indicator shows when the output data is changing. The SR-103 and HSR-103 require no adjustments or calibrations and logic is TTL compatible.

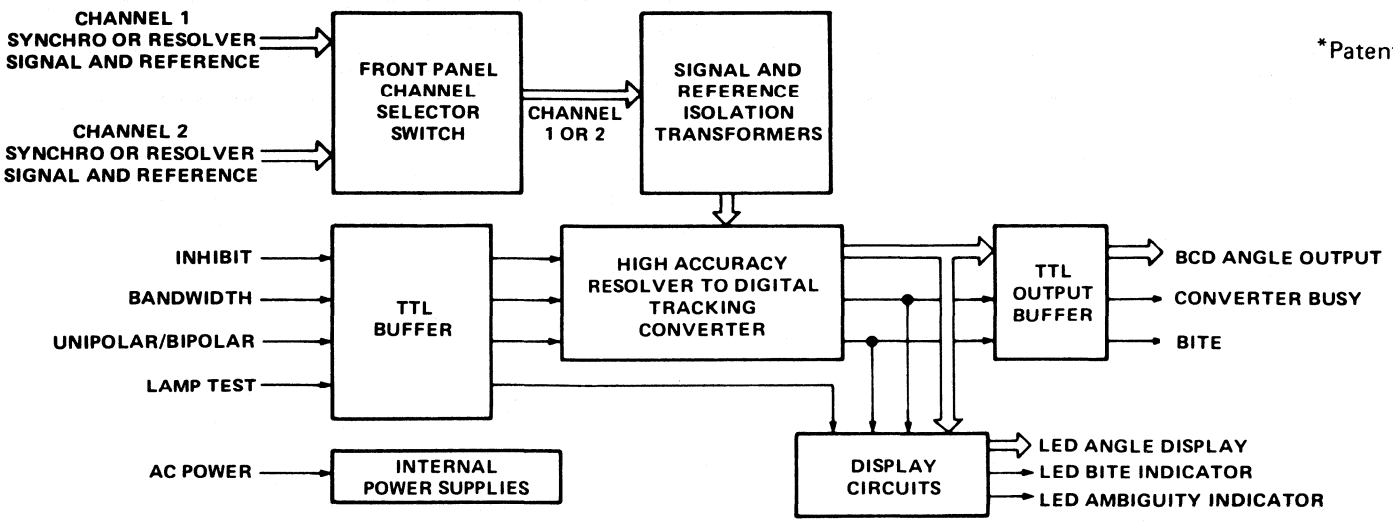
APPLICATIONS

The SR-103 and HSR-103 can be used wherever accurate angle information is required for display, control, testing purposes, or computation. Applications include production testing of synchros and resolvers, information translators in quality control systems, machine tool control, ship and aircraft navigation systems, and antenna positioning. The IEEE-488 adaptor option is convenient for interfacing these units with other instruments, for automatic test equipment (ATE) (see DBA-488 data sheet).

FEATURES

- *DOES NOT REQUIRE VOLTAGE OR FREQUENCY PROGRAMMING:*
  Automatically adjusts to reference levels of 10–150V and signal levels of 10–100V
  Broadband 47–1000 Hz frequency range
- *RESOLUTION AND ACCURACY:*
  SR-103 has 0.01° resolution and ±0.03° accuracy
  HSR-103 has 0.001° resolution and ±0.005° accuracy
- *TRANSFORMER ISOLATION FOR SIGNAL AND REFERENCE INPUTS*
- *TYPE II SERVO TRACKING LOOP:*
  No velocity lag and continuously available output for rates up to 2 rps (720°/sec)
- *LOGIC CONTROLS:*
  Converter Busy, Inhibit, High/Low Bandwidth, Unipolar/Bipolar display, Lamp Test
- *FAULT MONITOR INDICATES FAILURE TO TRACK*
- *DUAL SYNCHRO/RESOLVER INPUT CHANNELS WITH FRONT PANEL SELECTOR SWITCH*
- *TRANSFORMER ISOLATION FROM LINE VOLTAGE:*
  115/230V and 47–440 Hz power input

*Patented



SR-103 OR HSR-103 BLOCK DIAGRAM

SPECIFICATIONS

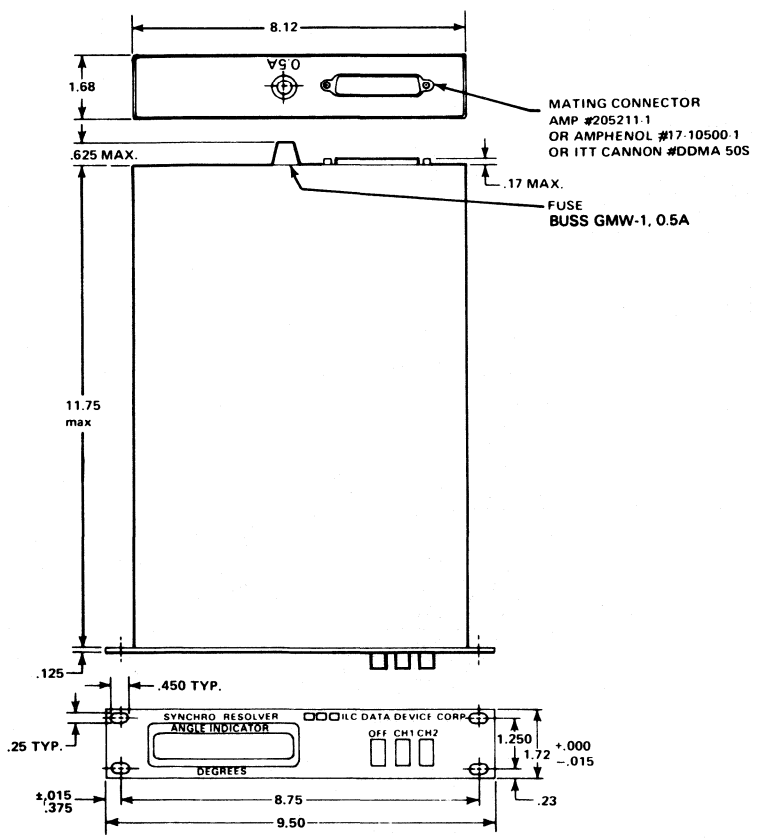
PARAMETER	VALUE	
	SR-103	HSR-103
RESOLUTION	0.01° (5 BCD digits)	0.001° (6 BCD digits)
ACCURACY (All Causes)	±0.03°	±0.005°
REPEATABILITY	Within 0.01°	Within 0.002°
ANGLE RANGE (Continuous Rotation)		
Unipolar	0° to +359.99°	0° to +359.999°
Bipolar	0° to ±179.99°	0° to ±179.999°
DISPLAY		
7-Segment 0.43" LED	5 digits	6 digits
REFERENCE INPUT		
Input Type	Transformer isolation	
Voltage Level	10–150V rms	
Frequency	47–1000 Hz	
Input Impedance	100 KΩ min	
Breakdown Voltage	1000V min to logic ground	
Harmonic Content	±10% max	
SIGNAL INPUTS		
Input Type	Synchro or Resolver, transformer isolated	
Line-to-Line Voltage	Auto-leveling, 10–100V	
Frequency	Same as reference	
Allowed Phase Shift	±50° max, relative to reference	
Input Impedance		
SR-103	150 KΩ min at 47 Hz 250 KΩ min between 60 and 1000 Hz	
HSR-103	1 MΩ min	
Breakdown Voltage	1000V min to logic ground	
DYNAMIC CHARACTERISTICS	SR-103	HSR-103
		TRACKING / SLEW
Tracking Rate (Full Accuracy)		
400 Hz	720°/sec	72° /sec / 720° /sec max
50–60 Hz	180°/sec	18° /sec / 180° /sec max
Settling Time (To Within 1 LSB)		
Lo Bandwidth (47–1000 Hz)	1.7 sec	2 sec
Hi Bandwidth (360–1000 Hz)	0.6 sec	1.5 sec
Open Loop Transfer Function		
$G = \frac{A^2(\frac{S}{B}+1)}{S^2(\frac{S}{10B}+1)}$		
Lo Bandwidth (47—1000 Hz)	A = 18; B = 10	A = 13; B = 10
Hi Bandwidth (360—1000 Hz)	A = 86; B = 46	A = 42; B = 21

PARAMETER	VALUE
DIGITAL INPUTS (TTL Compatible)	
Loading	0.5 Std TTL loads max
Inhibit (INH)	"1" or open = track "0" or GND = inhibits
Bandwidth Selector (BW)	"1" or open = Lo Bandwidth (47–1000 Hz) "0" or GND = Hi Bandwidth (360–1000 Hz)
Unipolar/Bipolar Selector (U/B)	"1" or open = unipolar operation (0° to 360°) "0" or GND = bipolar operation (–180° to +180°)
Lamp Test	"1" or open = normal operation "1" or GND = all LED segments on
DIGITAL OUTPUTS (TTL Compatible)	
Drive Capability	4 Std TTL loads, buffered output
Synchro or Resolver Angle	Parallel data bits; BCD angle; positive logic MSB becomes minus sign for bipolar operation SR-103 has 5 decades, 18 lines HSR-103 has 6 decades, 22 lines
Converter Busy (CB)	4 μsec positive pulse; leading edge initiates conversion
BITE	Indicates tracking failure from any cause (including excessive speed or equipment malfunction). "1" = fault
FRONT PANEL CONTROLS	
CH1/CH2	Selects input channel to be displayed
ON/OFF	Main power control
TEMPERATURE RANGES	
Operating	0° C to +50° C
Storage	–65° C to +125° C
POWER INPUT	
Voltage	115V or 230V rms, selected by switch on chassis
Power	10 VA max
Frequency	47–500 Hz
Isolation	Transformer isolated
Breakdown Voltage	1000 VDC min to logic ground
PHYSICAL CHARACTERISTICS	
Size	11-3/4 x 9-1/2 x 1-3/4 inch (29.8 x 24.1 x 4.45 cm)
Weight	4 lbs (1.8 kg)

REAR CONNECTOR PIN ASSIGNMENTS

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	AC power high	20	Bandwidth control "1" or open = LO BW = 47-1000 Hz "0" or GND = HI BW = 360-1000 Hz	37	Spare pin
2	AC power low			38	Lamp Test control "1" or open = normal operation "0" or GND = all LED segments on
3	Case GND				
4	Digital GND (can be connected to case GND)				
5	S1 } Channel 1 inputs.	21	S1 } Channel 2 inputs.	39	Unipolar/Bipolar control "1" or open = unipolar operation "0" or GND = bipolar operation
6	S2 } S4 for resolver	22	S2 } S4 for resolver		
7	S3 } use only.	23	S3 } use only.		
8	S4 }	24	S4 }		
9	Ref high } Channel 1	25	Ref high } Channel 2	40	BITE output "1" = not tracking (fault) "0" = normal tracking
10	Ref low } ref input	26	Ref low } ref inputs		
11	Converter Busy output "1" = converter busy "0" = data stable	27	Inhibit input "1" or open = track "0" or GND = hold (freeze)	41	.008° } For HSR-103 units only
				42	.004° }
				43	.002 }
				44	.001 }
12	.04°	28	.02°	45	20°
13	.01°	29	.08°	46	40°
14	.8°	30	.1°	47	80°
15	.2°	31	.4°	48	10°
16	4°	32	2°	49	100°
17	1°	33	8°	50	Unipolar: 200° Bipolar: "1" = minus sign
18	S-Ch 2. For channel 2 synchro operation only, connect pin 18 to pin 35.	34	S-Ch1. For channel 1 synchro operation only, connect pin 34 to pin 35.		
		35	SS Scott-T center tap		
19	Spare pin	36	Spare pin		

MECHANICAL OUTLINE FOR SR-103 AND HSR-103



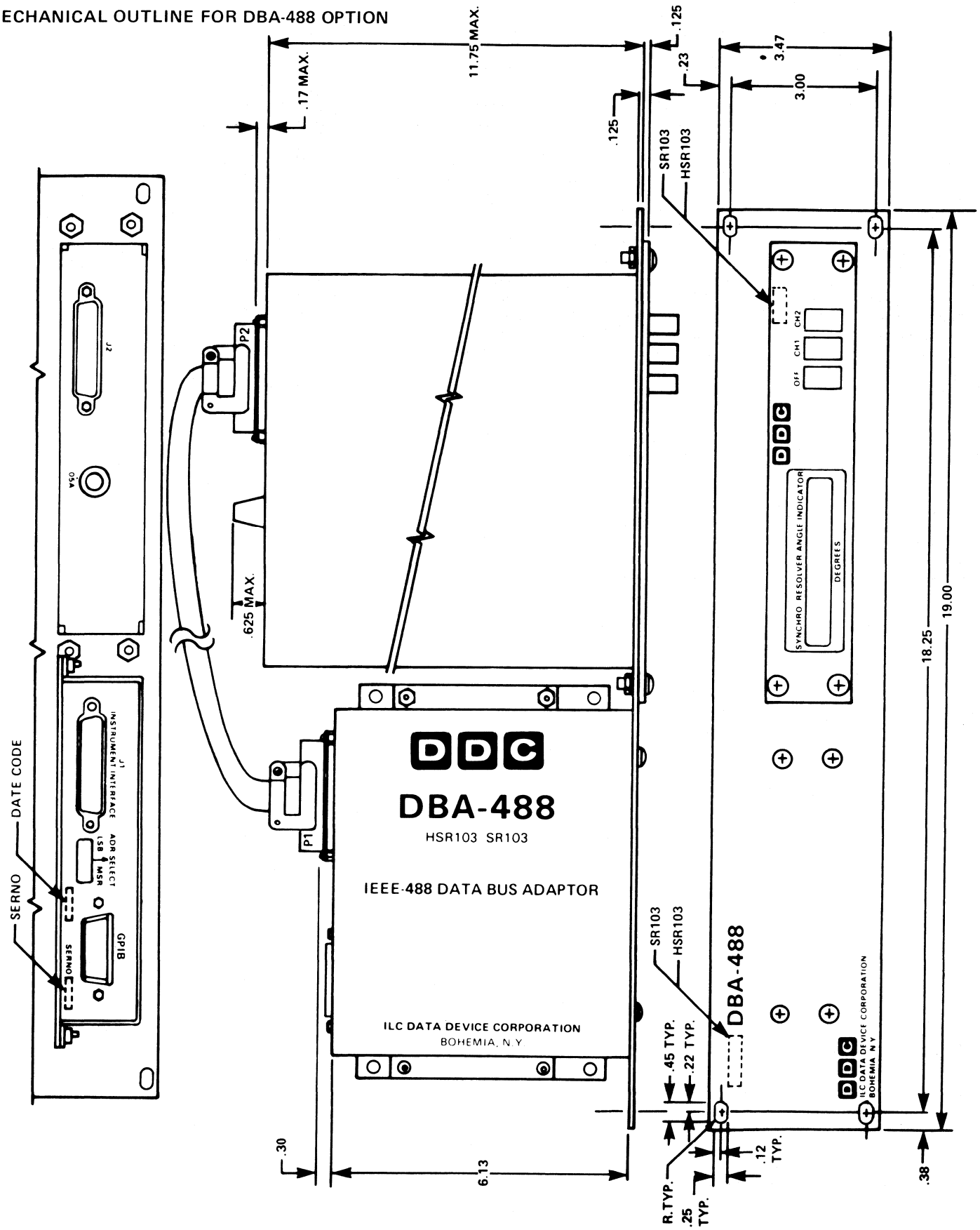
ORDERING INFORMATION

All instruments are supplied with a mating connector and an instruction manual.

SR – 103 – 2 – DBA – 488

- IEEE-488 Data Bus Adaptor:
  - Blank = SR-103 or HSR-103 only
  - DBA-488 = SR-103 or HSR-103 mounted together with a DBA-488 on a 3-1/2" high, 19" wide rack mounting panel, including cable connections
- Options:
  - Blank = SR-103
  - 2 = Option 2 (half rack mount)
  - 3 = Option 3 (center rack mount)
- Resolution and Accuracy:
  - SR = .01° resolution and ±.03° accuracy
  - HSR = .001° resolution and ±.005° accuracy

MECHANICAL OUTLINE FOR DBA-488 OPTION



The diagram on this page shows an SR-103 or HSR-103 instrument mounted together with a DBA-488 on a rack-mounting panel.

SYNCHRO AND RESOLVER ANGLE INDICATOR

DESCRIPTION AND APPLICATIONS

The SR-203 and HSR-203 are improved high quality angle indicators used in precision synchro and resolver test equipment. They accept synchro or resolver signals from a front panel input channel or either of two rear connector input channels. Output data, formated to BCD angle information, is provided and displayed on the front panel. Both models are enclosed bench-type instruments, with a carry handle, which may be used as a tilt stand. Control functions, such as input channel select, input type, bandwidth, unipolar/bipolar, lamp test and inhibit, may be controlled either manually by front panel switches or remotely with control logic to the rear connector. A single switch multiplexes control between local and remote sources and front panel and rear connector input channels. An internal IEEE-488 data bus interface is available as an option. The SR-203 and HSR-203 instruments differ only in their accuracy and resolution. The SR-203 is accurate to ± 0.03°, while the HRS-203 is accurate to ±.005°. Resolution for the devices is ±0.01° and ±0.001° respectively (see Specifications). Because they can accept a broad range of voltages and frequencies, without programming, and signal to reference phase shifts of ± 50° (max), the SR-203 and HSR-203 are ideal for situations where a variety of inputs must be quickly accomodated. Using a type II servo loop for continuous tracking, these instruments have no velocity lag up to the specified tracking rates. There can be no hangup 180° away from the input angle. A fault indicator shows when the unit is not tracking the input signal, and an ambiguity indicator shows when the output data is changing. The SR-203 and HSR-203 require no adjustments or calibrations and logic is TTL compatible. The SR-203 and HSR-203, in addition to serving as high performance bench instruments, can be used wherever accurate angle information is required for display, control, testing purposes, or computation. Applications include production testing of synchros and resolvers, information translators in quality control systems, machine tool control, ship and aircraft navigation systems and antenna positioning. The IEEE-488 adapter option is convenient for interfacing these units with other instruments for automatic test equipment (ATE).

FEATURES

- *RESOLUTION TO .001°*
- *FRONT PANEL CONTROLS*
- *OPTIONAL IEEE-488 I/O*
- *FAULT INDICATOR*
- *PHASE SHIFT COMPENSATION*
- *BROADBAND (47-1000 Hz)*

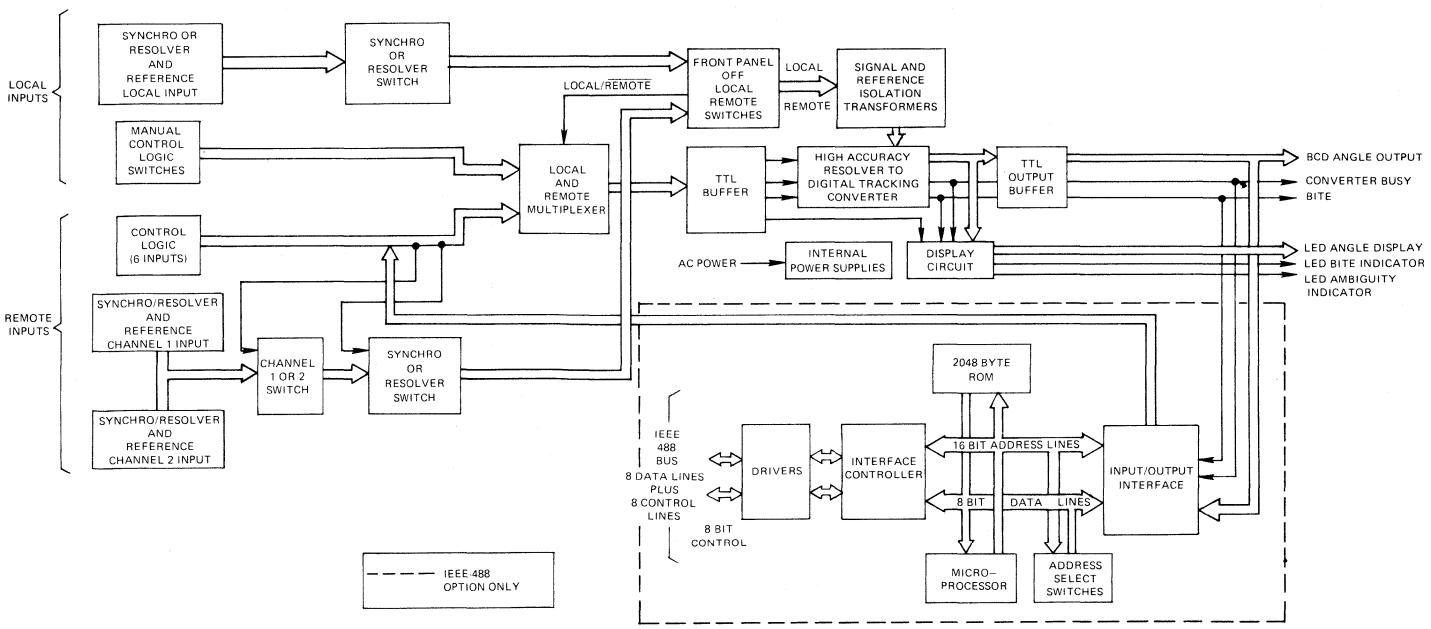


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

PARAMETER	UNITS	VALUE	
		SR-203	HSR-203
RESOLUTION	deg	0.01 (5 BCD digits)	0.001 (6 BCD digits)
ACCURACY (all causes)	deg	±0.03	±0.005
REPEATABILITY	deg	Within 0.01	Within 0.002
ANGLE RANGE (Continuous Rotation)			
Unipolar	deg	0 to +359.99	0 to +359.999
Bipolar	deg	0 to ±179.99	0 to ±179.999
DISPLAY			
7 Segment 0.43" LED		5 Digits	6 Digits
REFERENCE INPUT			
Input Type		Transformer isolation	
Voltage Level	V	10 to 150 rms	
Frequency	Hz	47 to 1000	
Input Impedance	Ω	100k min	
Breakdown Voltage	V	1000 min to logic ground	
Harmonic Content	%	±10 max	
SIGNAL INPUTS			
Input Type		Synchro or resolver, transformer isolated	
Line-to Line Voltage	V	Auto-leveling, 10 to 100	
Frequency	Hz	Same as Reference	
Allowed Phase Shift	deg	±50 max, relative to reference	
Input Impedance			
SR-203	Ω	150k min at 47 Hz	
	Ω	250k min between 60 and 1000 Hz	
HSR-203	Ω	1M min	
Breakdown Voltage	V	1000 min to logic ground	

DYNAMIC CHARACTERISTICS		SR-203	HSR-203 TRACKING	HSR-203 SLEW
Tracking Rate (Full Accuracy)				
400 Hz	deg/sec	720	72	720 max
50 to 60 Hz	deg/sec	180	18	180 max
Setttling Time (To Within 1 LSB)				
Lo Bandwidth (47 to 1000 Hz)	sec	1.7	2	
Hi Bandwidth (360 to 1000 Hz)	sec	0.6	1.5	
Open Loop Transfer Function				

$$G = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

Lo Bandwidth (47 to 1000 Hz)	A = 18, B = 10	A = 13, B = 10
Hi Bandwidth (360 to 1000 Hz)	A = 86, B = 46	A = 42, B = 21

DIGITAL INPUTS (TTL Compatible)	
Loading	0.5 std TTL loads max
Inhibit (INH)	"1" or open = track "0" or GND = inhibits
Bandwidth Selector (BW)	"1" or open = 47 to 1000 Hz (Lo Bandwidth) "0" or GND = 360 to 1000 Hz (Hi Bandwidth)

PARAMETER	UNITS	VALUE
DIGITAL INPUTS (TTL Compatible)		
Loading		0.5 std TTL loads max
Inhibit (INH)		"1" or open = track "0" or GND = inhibits
Bandwidth Selector (BW)		"1" or open = 47 to 1000 Hz (Lo Bandwidth) "0" or GND = 360 to 1000 Hz (Hi Bandwidth)
Unipolar/Biopolar Selector (U/B)		"1" or open = unipolar operation (0° to 360°) "0" or GND = bipolar operation (−180° to +180°)
Lamp Test		"1" or open = normal operation "0" or GND = all LED segments on
Remote Channel Select		"1" or open = channel 2 "0" or GND = channel 1
Remote Synchro/Resolver Select		"1" or open = resolver "0" or GND = synchro
DIGITAL OUTPUTS (TTL Compatible)		
Drive Capability		4 std. TTL loads, buffered output.
Synchro or Resolver Angle		Parallel data bits; BCD angle; positive logic MSB becomes minus sign for bipolar operation SR203 has 5 decades, 18 lines. HSR203 has 6 decades, 22 lines.
Converter Busy		4 μsec positive pulse; leading edge initiates conversion indicates tracking failure from any cause (including excessive speed or equipment malfunction) "1" = fault.
FRONT PANEL FUNCTIONS		
Local/Remote Select		Select input panel from front panel or rear connector.
On/Off		Main power control
Lamp Test		ALL LED segments on
Inhibit		Inhibits converter tracking
Synchro/Resolver		Synchro or Resolver select
Bandwidth		Select between HI and LO bandwidths.
Readout		Selects between unipolar and bipolar display and output
		} Controls applicable for local mode (front panel inputs) only
FRONT PANEL INPUTS TERMINALS		
Local Signal Inputs		
S1		Synchro/Resolver
S2		Synchro/Resolver
S3		Synchro/Resolver
S4		Resolver only
Local Reference Inputs		
RH		Reference HIGH
RL		Reference LOW
DIG GND and CASE		Digital and case ground respectively
POWER INPUT		
Voltage	**Vrms**	**115/230; selectable via two internal switches (set for 115V unless otherwise specified).**
Power	**VA**	**20 max**
Frequency	**Hz**	**47 - 500**
Isolation		**Transformer**
Breakdown Voltage (To Logic Gnd)	**VDC**	**1000**
TEMPERATURE RANGES		
Operating	°C	0 to +55
Storage	°C	−55 to +125
PHYSICAL CHARACTERISTICS		
Size	in	14.5 x 7.9 x 3.5 (368 x 201 x 89 mm)
Weight	lbs	11.0 (4.9 Kg)

REAR CONNECTOR

PIN CONNECTION TABLE

PIN	FUNCTION
1	Spare Pin
2	Spare Pin
3	Case GND
4	Digital GND (may be connected to case GND)
5	S1
6	S2 } Remote Channel 1 inputs
7	S3 } (S-4 for Resolver use only
8	S4
9	REF HI }
10	REF } Channel 1 Ref input
11	Converter Busy Output
	1 = Data Stable
	0 = Converter Busy
12	.04°
13	.01°
14	.8°
15	.2°
16	4°
17	1°
18	Spare Pin
19	Lamp Test Input*
	1 = Normal Operation
	0 = Lamp Test (Remote Mode)
20	Channel 1/Channel 2 Inputs*
	1 = Channel 2
	0 = Channel 1

PIN	FUNCTION
21	S1 }
22	S2 } Channel 2 inputs
23	S3 } (S4 for Resolver use only)
24	S4 }
25	REF HI } Channel 2 Ref Input
26	REF LO }
27	Inhibit Input*
	1 = Track
	0 = Inhibit
28	.02°
29	.08°
30	.1°
31	.4°
32	2°
33	8°
34	Reset Input (TTL logic)
	1 = Normal Operation } IEEE Interface
	0 = Reset }
35	Unipolar/Bipolar Output
	1 = Unipolar } Remote Mode
	0 = Bipolar }
36	Local/Remote Output
	1 = Local Mode
	0 = Remote Mode
37	Synchro/Resolver Input*
	1 = Resolver } Remote Mode
	0 = Synchro }

PIN	FUNCTION
38	Unipolar/Bipolar Input*
	1 = unipolar } Remote Mode
	0 = bipolar }
39	Bandwidth Input*
40	BITE Output
	1 = Not Tracking (fault)
	0 = Normal Tracking
41	.008°
42	.004°
43	.002°
44	.001°
45	20°
46	40°
47	80°
48	10°
49	100°
50	Unipolar = 200°
	Bipolar = 1 = minus sign (-)

* The User must supply digital input signals for standard (Non-I-EEE-488) units. For units including the IEEE-488 interface option, these pins *must not* have external connections.

TECHNICAL INFORMATION

Both SR-203 and HSR-203 instruments are available with an IEEE-488 Data Bus Interface circuit built in (see Figure 1). This option must be specified when the instruments are ordered. Add "-488" to the part number as shown in ORDERING INFORMATION.

The IEEE-488 option provides the capability to process signals received from or transmitted to a parallel data bus as described in the IEEE-488 Data Bus Standard of 1975. When programmed to operate with the "488" Data Bus Controller, the SR/HSR-203-488 will perform the command sequences shown in Figures 2 and 3.

In the talk routine (Figure 2), the instrument transmits a sign byte (+, – or E for error) followed by 5 (for SR-203) or 6 (HSR-203) BCD ASCII data bytes, followed by CR (carriage return), followed by LF (line feed), with EOI (End or Identify), when interrogated by the controller.

Figure 4 indicates the possible ASCII control words that would be transmitted from a controller to the instrument as shown in the listen routine (Figure 3).

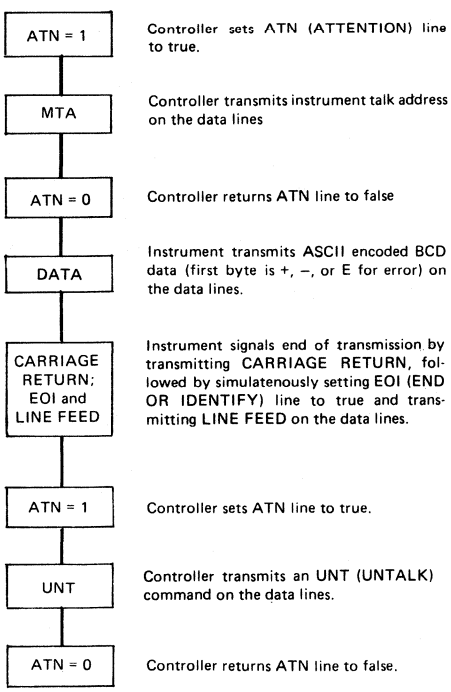


FIGURE 2. COMMAND SEQUENCE FOR TALKING

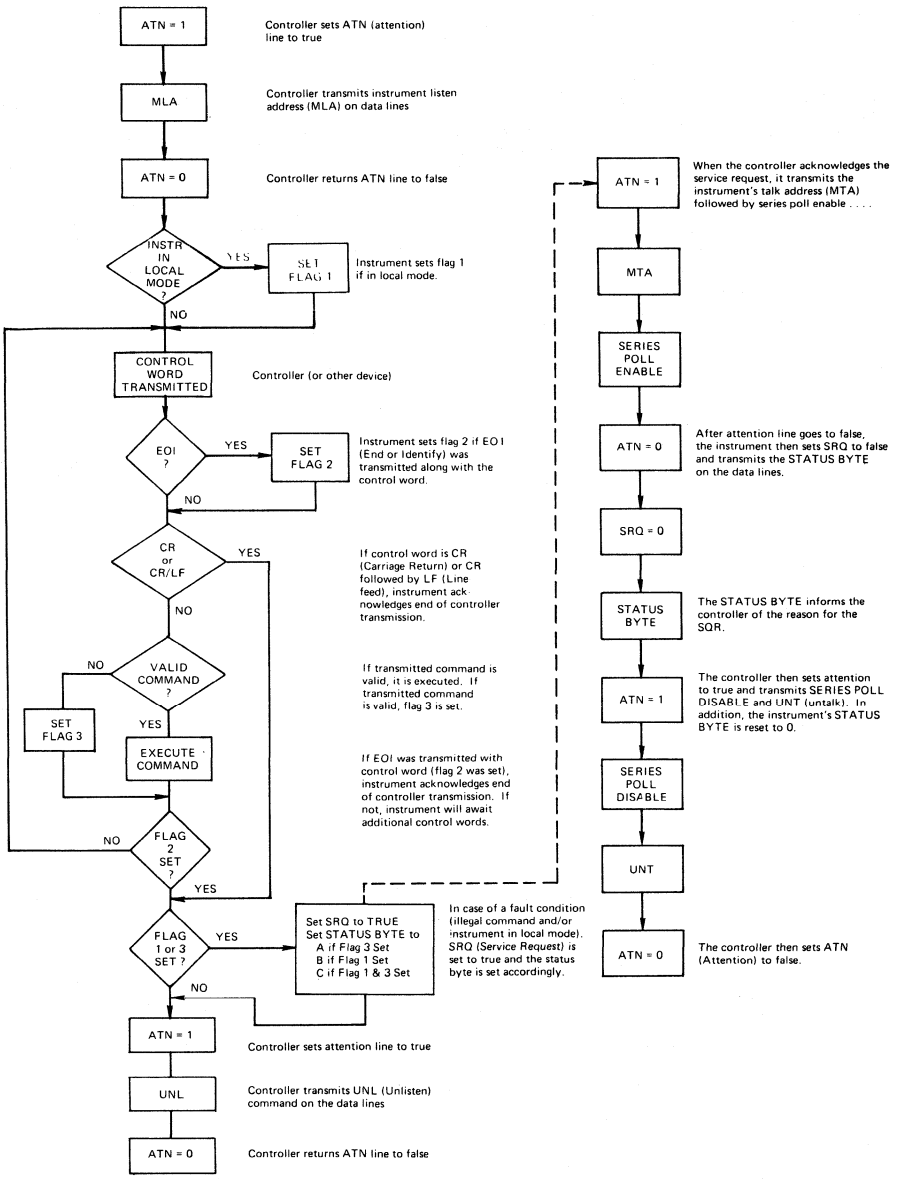


FIGURE 3. COMMAND SEQUENCE FOR LISTENING

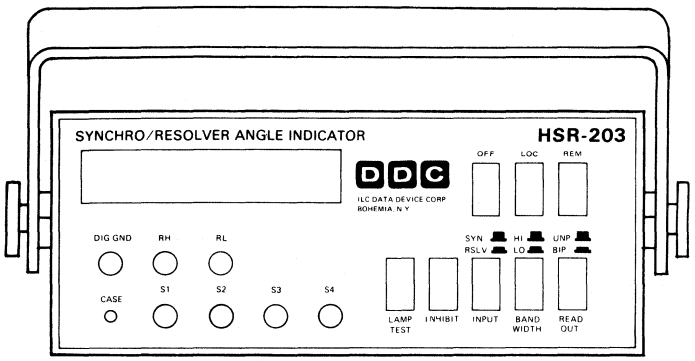
COMMAND FUNCTIONS FOR IEEE-488 OPTION

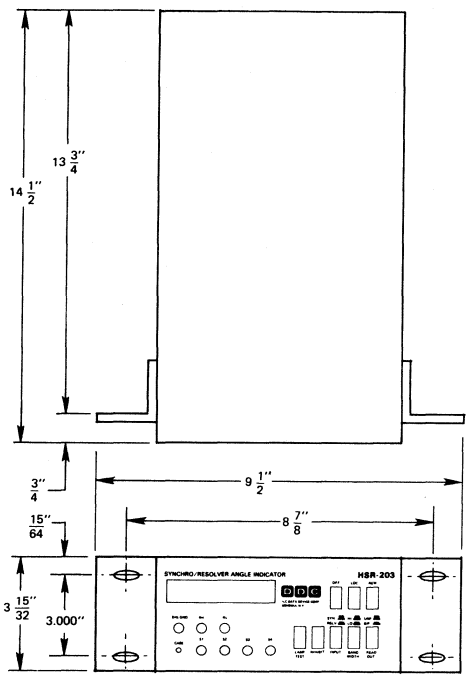
NOTE: 1. IEEE-488 Interface will accept all input commands, regardless of input mode selected (local or remote). When the instrument is switched to Remote mode, the last commands received will take effect.

2. The SR–203 is controlled exclusively by front panel switching when local mode is selected. Lamp test switch will illuminate all LED segments regardless of input mode.

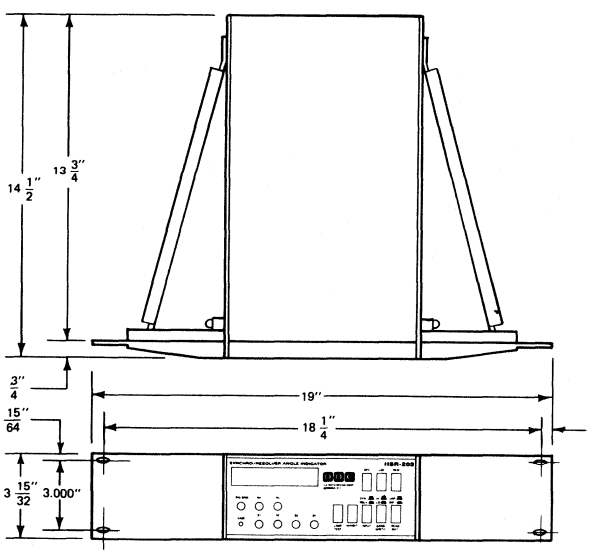
CONTROL WORD (ASCII)	FUNCTION
P (Preset)	Preset to: Channel 1, Synchro input, No inhibit, No lamp test, High bandwidth, Unipolar Output
S (Synchro)	Sets Synchro or Resolver input mode
R (Resolver)	
1 (Channel 1)	Selects between remote Input channels 1
2 (Channel 2)	and 2 on rear connector
H (High)	Select high or low bandwidth
L (Low)	
U (Unipolar)	Selects unipolar or bipolar readout and
B (Bipolar)	output
I (Inhibit)	Inhibits the converter or allows it to
F (Follow)	follow (track) the input
T (Test)	Tests lamps (T) or display data (D)
D (Data)	

FIGURE 4. CONTROL CODE FUNCTIONS



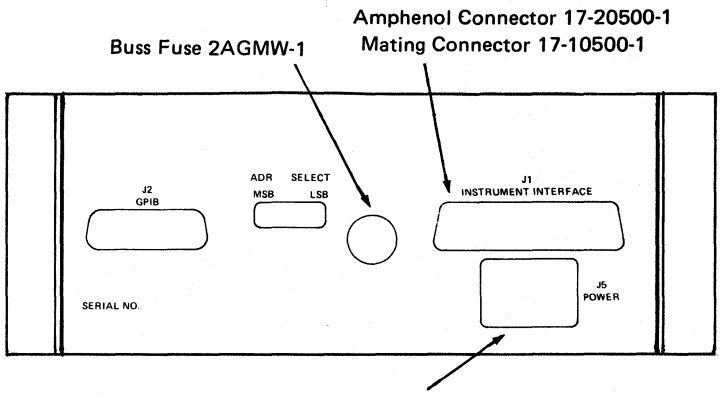


OPTION 2 Half Rack Mount



OPTION 3 Center Mount 19" Panel

POWER CONNECTOR EAC 301 SWITCHCRAFT



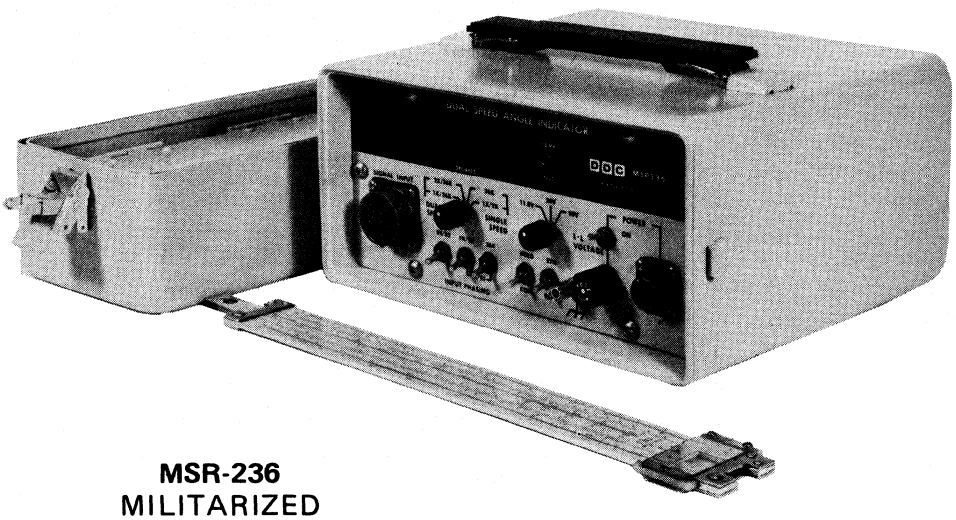
ORDERING INFORMATION

SR – 203 – 1 – DBA-488

- DBA-488 — IEEE-488 Option:
  - 488 = Built-in IEEE-488 Interface
- 1 — Configuration Options:
  - Blank = SR-203
  - 1 = Standard option 1 carryhandle
  - 2 = Option 2 half-rack mount
  - 3 = Option 3 center mount on 19" panel
- SR — Accuracy (worst case, all causes)
  - SR = ± 0.03°
  - HSR = ± 0.005°

All instruments are supplied with a mating connector, a detachable line cord and instruction manual.

MULTISPEED SYNCHRO/RESOLVER ANGLE INDICATOR
Measures Single/Dual Speeds in Dual Speed Systems



MSR-236
MILITARIZED
PACKAGE

DESCRIPTION

The MSR-236 is a versatile angle indicator instrument for dual speed synchro and resolver systems. Front panel switches can be used not only to select the input (synchro or resolver, L-L voltage level, speed ratio) and to control (inhibit, lamp test) but also to change the measurement after the system has been connected (dual speed or single speed at either input; reverse direction of rotation). The MSR-236 is housed in a rugged, militarized MIL-T-21200 type drip-proof combination case designed for shipboard use. The instrument can be used to display angle, to test synchro or resolver systems, and to interface single or dual speed systems with a computer. No adjustments or calibrations are required, and there is no warm-up period, drift, or jitter.

APPLICATIONS

Designed as a rugged, all-purpose multispeed angle indicator, the MSR-236 can be used wherever the accuracy of two-speed conversion is required. It can be used as test and measuring equipment, or it can be installed as part of a system control loop, serving as a converter with a display. Since the single speed of each two-speed input can be measured independently, the MSR-236 is useful for system alignment. Applications are found in radar antenna systems, fire control systems, navigation sensors, and automatic machine tool control monitoring.

FEATURES

- *MEASURES ANGLE IN SINGLE OR DUAL SPEED MODES IN 1:36 AND 2:36 SPEED SYSTEMS*
- *DISPLAYS 5 DECADE ANGLE WITH .01° RESOLUTION AND PRODUCES PARALLEL BCD DIGITAL OUTPUT*
- *ACCURACY:*
  ±0.01° in multispeed mode
  ±0.1° ±1 LSB in single speed mode
- *SIGNAL AND REF INPUT:*
  Transformer isolation
  All common synchro and resolver L-L voltage levels and frequencies
  Front panel switches can change reference and signal phasing to reverse sense of rotation
- *LOGIC:*
  TTL compatible
  Converter Busy and Inhibit
- *OPERATES FROM STANDARD LINE VOLTAGES, 115/230V WITH TRANSFORMER ISOLATION, AND 47–440 Hz*

SPECIFICATIONS	
PARAMETER	**VALUE**
RESOLUTION	0.01°
ACCURACY (All Causes)	
Dual Speed Mode	±0.01°
Single Speed Mode	±0.1° ±1 LSB
ANGLE RANGE	000.00° to 359.99°, continuous rotation for 1X and 1:36 speed modes ±89.99° in 2X and 2:36 speed modes
CONVERSION RATE	Greater than 30 times/sec Harmonic oscillator type converter
FRONT PANEL DISPLAY	5 digit, 7 segment, LED display
REFERENCE INPUT	
Input Type	Transformer isolation
Voltage	10 to 130V
Frequency	47 to 500 Hz
Input Impedance	25K ohms min
Allowed Phase Shift	±20° relative to signal, for full accuracy
Breakdown Voltage	±500 VDC to Logic GND
SIGNAL INPUT	
Input Type	Transformer isolation Dual speed synchro or resolver input
Voltage	11.8V, 26V, or 90V Line-to-Line
Frequency	Same as Reference
Impedance	100 KΩ min
Tolerances:	
Voltage	±20%
Harmonics	±10%
Breakdown Voltage	±500 VDC to Logic GND
DIGITAL INPUT/OUTPUT (TTL Compatible)	
Digital Angle Output	5 BCD decades, 18 data lines total, positive true logic, continuously available: 200°, 100°, 80°, 40°, 20°, 10°, 8°, 4°, 2°, 1°, 0.8°, 0.4°, 0.2°, 0.1°, 0.08°, 0.04°, 0.02°, 0.01° Drive capability is 5 Std TTL loads, buffered outputs
Converter Busy Output	2 μsec positive pulse (logic 1 = busy) Drive capability is 5 Std TTL loads, buffered output
Inhibit Input	Logic 0 inhibits update of angle display and BCD output Loading is 1 Std TTL load
FRONT PANEL CONTROLS	
Synchro/Resolver	Selects synchro or resolver mode
Line-to-Line Voltage	Selects 11.8V or 26V or 90V
Measurement Mode	Selects dual speed 1:36, or dual speed 2:36, or single speed of 1X or 2X input, or single speed of 36X input
Hold/Convert	Applies Inhibit
Lamp Test	Tests LED display by lighting all segments (888.88 display)
Power ON/OFF	Main power control
TEMPERATURE RANGES	
Operating	0°C to +55°C
Storage	−55°C to +125°C
POWER INPUT	
Voltage	115/230V rms ±10%
Power Frequency	47 to 440 Hz
Fuse (on Rear Panel)	Buss, GMW -1, 1 Amp
Isolation	Transformer
PHYSICAL CHARACTERISTICS	
MSR-236	MIL-T-21200 type drip-proof combination case. Removable front cover stores signal and power cables. Color either "Flight-Line" yellow or "Standard" grey.
Size	12 x 9.6 x 4.8 inch (30.5 x 24.4 x 12.2 cm)
Weight	11.7 lbs typ, including cables (5.3 kg)
Connectors	Standard MS connectors on front panel; 15 ft signal cable for reference and signal inputs terminates with clearly identified alligator clips; 8 ft power cord.

PIN ASSIGNMENTS

J1 POWER CONNECTOR

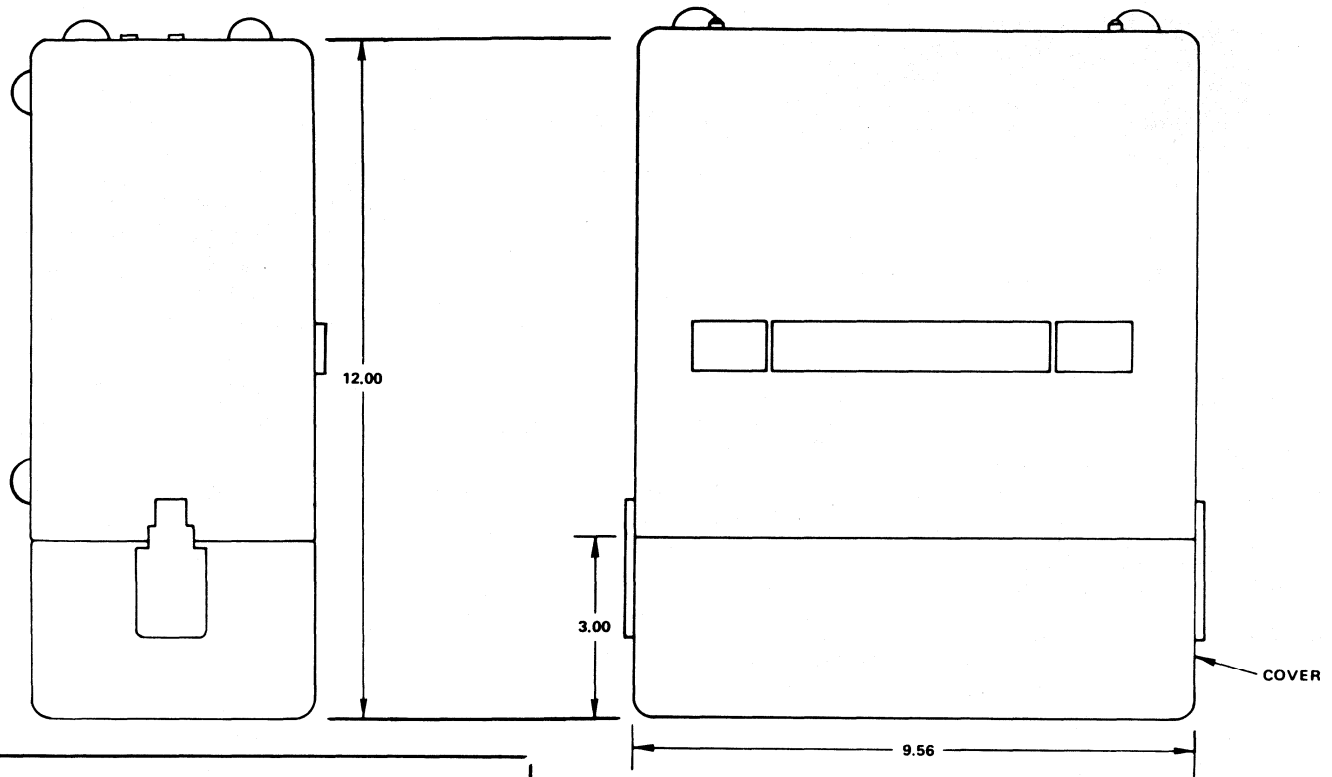
MSR-236 Pin No.	Function
A	115V/230V High
E	115V/230V Low (Neutral)
C	Chassis GND

NOTE: 115V or 230V operation is selected by a switch inside the case. Units are set for 115V unless specified otherwise.

J2 INPUT/OUTPUT CONNECTOR

MSR-236 Pin No.	Function
A	S1 } X36 INPUT
B	S3 } S4 for
C	S4 } resolver
D	S2 } inputs only
E	200°
F	100°
G	80°
H	40°
J	20°
K	10°
L	8°
M	4°
N	2°
P	S1 } X1 INPUT
R	S3 } S4 for
S	S4 } resolver
T	S2 } inputs only
U	RH Reference high
V	RL Reference low
W	.8°
X	.4°
Y	.2°
Z	.1°
a	.08°
b	.04°
c	.02°
d	.01°
e	CB Converter Busy
f	GND Digital ground
g	INH Inhibit
h	Spare pin
j	1°
—	Spare pins

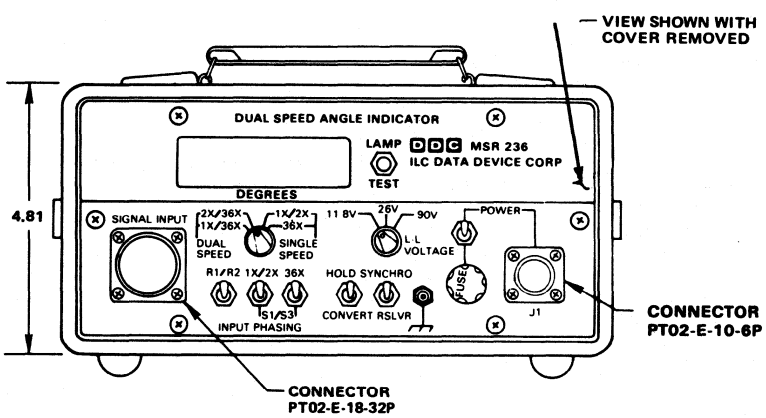
MSR-236 MECHANICAL OUTLINE



ORDERING INFORMATION

MSR-236* Instrument packaged in a MIL-T-21200 combination case. MS connectors, signal cord, line cord and instruction manual are included.

*MSR-236 case will be "standard" grey unless another color is requested.



ILC DATA DEVICE CORPORATION

SYNCHRO AND RESOLVER ANGLE SIMULATORS

FOR NEW DESIGNS
USE SIM-31200

DESCRIPTION

The SR-400 and SR-460 are precision solid state angle simulators intended to meet the demand for compact, high quality synchro and resolver source standards. They are suitable for production testing systems, quality control inspections, laboratory instrumentation, and portable use in the field. Easily interfaced with external digital control systems, they may be incorporated for control and display into a variety of systems, including navigation equipment, antenna positioning devices, and machine tool control systems. To provide a complete synchro/resolver stimuli and measurement capability for automatic and semi-automatic test equipment (ATE), the SR-400 (or SR-460) angle simulator can be connected to its sister instrument, the SR-203 (or HSR-203) angle indicator.

The SR-400 and SR-460 differ only in the allowed ranges for the reference frequency. The SR-400 (designed for 400 Hz) has a frequency range of 360 – 1000 Hz for all specified reference input voltages. The SR-460 (designed for 60 or 400 Hz) has a frequency range of 47 – 440 Hz at 115V reference input. For a 26V reference input, the SR-460 frequency range is 360 – 440 Hz.

Operational status and output selection may be controlled either manually by front panel switches, or remotely via signals to the rear connector. In either control mode, the angles simulated are displayed on the front panel. When the REMOTE pushbutton is depressed, the front panel ANGLE SELECTOR, SYNCHRO/RESOLVER MODE, and LINE VOLTAGE controls and REF INPUT jacks are disabled, transferring control to the external system. The signal outputs are available both at the front panel and at the rear connector in both local and remote modes.

The input register stores angle data either from the manual front panel 5-decade switch or from the input digital data lines. In the remote mode, a Data Strobe signal at the rear connector gates the angular data, format, and level commands into the converter system. The Strobe Flag indicates to the external system that a strobe was received at the unit.

The display has five 7-segment LED digits equipped with a polarizing filter for good readability. During remote operation the LED display may be tested by grounding (logic 0) the Lamp Test input, producing a readout of 888.88°.

FEATURES

- *ANGLE INPUT: 18-bit BCD angle with ±0.01° resolution selected manually by front panel switches or remotely by digital input. Input buffer storage register with bright 5-decade LED display.*
- *REFERENCE INPUT: 26V or 115V, and frequency from 47 to 1000 Hz.*
- *PROGRAMMABLE OUTPUT: standard synchro or resolver levels at 11.8V, 26V or 90V L-L.*
- *ACCURACY: ±0.01° no load; ±0.03° full load. Short 100μs settling time.*
- *Transformer isolation for reference input and signal output.*
- *DTL/TTL compatible logic for data strobe and input angle.*
- *Short circuit, overload and overvoltage protection. No adjustments or calibrations. No warm-up, drift or jitter.*
- *Operates with transformer isolation from line voltage: 115/230V, 47 to 440 Hz.*

SPECIFICATIONS
For ±10% variation in carrier frequency and reference voltage; up to 10% harmonic distortion in the reference; and ±3% line voltage variation

PARAMETER	VALUE
RESOLUTION	0.01°
ACCURACY	±0.01° no load; ±0.03° full rated load
ANGLE RANGE	000.00° to 359.99°, continuous rotation
DISPLAY	5-digit, 7-segment LED with polarizing filter
DIGITAL INPUT/OUTPUT	
Type	TTL/DTL compatible
Inputs	BCD Angle Input Strobe Lamp Test
REFERENCE INPUT	
Type of Input	115V (nominal) isolation transformer with a 26V tap
Input Locations	Front panel for local mode Rear connector for remote mode
Frequency Ranges:	
SR-400	360 to 1000Hz with 115 or 26V ref input
SR-460	47 to 440Hz with 115V ref input 360-440Hz with 26V ref input

PARAMETER	VALUE
SYNCHRO/RESOLVER OUTPUT	
Type of Output	Synchro (S1, S2, S3 outputs) or resolver (S1, S2, S3, S4 outputs) with transformer isolation
Output Locations	Front panel and rear connector, active in both local and remote modes
L-L Voltage	90V, 26, or 11.8V selectable Voltage accuracy ±3% Output level tracks reference input level
Min Balanced L-L Load Impedance Z_{L-L}	$\frac{90V_{L-L}}{4000\Omega}$ | $\frac{26V_{L-L}}{500\Omega}$ | $\frac{11.8V_{L-L}}{100\Omega}$
Synchro	5500Ω | 650Ω | 135Ω
Resolver	
Breakdown Voltage	±500VDC to logic GND
POWER INPUT (Rear Connector – Separate line cord supplied)	
Voltage	115/230V RMS ± 10%
Power Frequency	47 to 440Hz
Fuse (on Rear Panel)	Buss, GMW -2, 2 Amp
Isolation	Transformer
PHYSICAL CHARACTERISTICS	
Size	8-1/8 x 3-1/2 x 14-1/2 in. (20.6 x 8.9 x 36.8 cm)

SECTION I

MIL-STD-1553

DATA BUS PRODUCTS

SUMMARY TABLE

Name	Form Factor	Features	Page
BUS-1553	Encap. Module 3.1 x 2.6 x 0.4"	Interface module for MIL-STD-1553 A/B applications. Has 16 transmit and 16 receive data lines. Contains hybrid tranceiver BUS-8553 and Pulse Transformer BUS-25679 internal. Stub couple compatible with an external BUS-25679 Transformer.**	317
BUS-1555	Encapsulated Module 3.1 x 2.6 x 0.8"	MIL-STD-1553 A/B decoder module for test equipment. Has 16-bit parallel and NRZ serial data outputs, and 16 MHz internal clock with clock output. Error flags include Sync, Manchester II and High/Low Bit Count.	319
BUS-1556	Encapsulated Module 3.1 x 2.6 x 0.8"	MIL-STD-1553 A/B error generating encoder module for test equipment. Generates Manchester Coding, Parity, High/Low Bit Count and Sync Field error signals. Converts parallel data into Manchester II serial data.	323
BUS-8554	1.25 x 1.25 x 0.2" Plug-in hybrid	Form-fit-function replacement for CT-3231. Operates from ±12V to ±15V. Less power on receiver than CT-3231. Compatible with BUS-25679 Transformer in stub coupled applications.**	327
BUS-8555	0.9 x 1 x 0.2" Flatpack hybrid	For McDonnell Douglas or MIL-STD-1553 A/B receiver applications. Form-fit function replacement for CT-3078. Operates at ±12V to ±15V and dissipates less power than CT-3078. Compatible with BUS-25679 for stub coupled applications.**	330
BUS-8556	1.25 x 1.25 x 0.2" Flatpack hybrid	For McDonnell Douglas or MIL-STD-1553A transmitter applications. Form-fit-function replacement for CT-2077 and CT-3077. Operates on ±12V to ±15V and is compatible with BUS-25679 Transformer for stub coupled applications.**	332
BUS-8559	24 pin DDIP hybrid	MIL-STD-1553 transceiver with variable output for use in test systems	334
BUS-8937	1.7 x 1.1 x 0.2" Plug-in hybrid	Manchester encoder/decoder, compatible with all MIL-STD-1553 applications. Features address recognition, 16 three state transmit and receive lines and double buffered registers. Interfaces directly with BUS-8553 transceiver. Compatible with BUS-8554, BUS-8555 and BUS-8556 with external logic inverter circuitry.	337
BUS Transformers	0.6 x 0.6 x 0.275" 0.6 x 0.6 x 0.3"	MIL-STD-1553 Isolation Transformers.	342
BUS-63102	1.25 x 1.25 x 0.2" Flatpack hybrid	Universal transceiver for MIL-STD-1553 A/B and McDonnell-Douglas applications.	345
BUS-63104	1.25 x 1.25 x 0.2" Square pack hybrid	Form fit-function replacement for CT-3231 Transceiver. Meets all specifications of MIL-STD-1553 A/B. Operates from ±12 to ±15V.	349
BUS-63105 BUS-63125 SERIES	24 pin DDIP hybrid	LSI based low cost transceiver for MIL-STD-1553 A/B to replace BUS-8553. Single and dual redundant.	352
BUS-64100	2.2 x 1.2 x 0.2" Hybrid	Low power MIL-STD-1553 Terminal Bit Processor with LSI design which performs Broadcast, Mode Code, Own Address and Time Out functions. Has 16-bit or 8-bit byte parallel or serial I/O, Dual rank registers and on/off line self-test.	356

**For other transformer requirements contact the factory.

SUMMARY TABLE CONTINUED

Name	Form Factor	Features	Page
BUS-65101	1.6 x 1.9 x 0.2" Hybrid	MIL-STD-1553 dumb RTU hybrid with 16-bit or 8-bit 3-state parallel or serial I/O. Functions as single or dual redundant RTU, Bus Controller or Bus Monitor. Provides error flags for Own Address, Mode Code, Broadcast and Time Out. Contains transceiver, encoder/decoder, dual rank I/O registers and clock oscillator.	362
BUS-65122	2.1 x 1.9 x 0.25" Hybrid	Dual redunant MIL-STD-1553 RTU hybrid, including dual transceivers, dual encoder/decoders, protocol sequencer and 32 word FIFO. Features include small size, low power, mode code implementation, wrap around test and time out.	370
BUS-65201	1.8 x 1.6 x 0.2" Hybrid	MIL-STD-1553 and MACAIR compatible dumb RTU with functions to interface between the MUX data bus and a subsystem 3-state parallel data highway. Sufficient handshaking, control and data lines for operation as RTU, BC or Bus Monitor. Output flags for Own Address, Mode Code, Broadcast, Timeout, Valid Word and Sync Type.	380
BUS-65400	6.6 x 4.9" P.C. card	Dual redundant MIL-STD-1553 interface card with Smiths LSI Chip Set, DDC standard transceivers (BUS-63115) and isolation transformers (BUS-25679). May be directly incorporated into a subsystem or used for circuit evaluation during design stages.	388
BUS-65401	7 x 4 x 0.35" P.C. Card	Complete dual redundant MIL-STD-1553 RTU with protocol and dual port memory subsystem interface. Serves as an intelligent interface between the 1553 Data Bus and a subsystem data highway.	402
BUS-65500	9.2 x 6.3 x 0.4" P.C. Card	Dual redundant Bus Controller and Remote Terminal Unit with VME interface. Supports all MIL-STD-1553 message formats, 11 Mode Codes and provides built-in-test capability. Its 4K x 16 bit dual port RAM and four types of interrupts minimize CPU overhead.	410
BUS-65600	2.1 x 1.9 x 0.25" Hybrid	Dual redundant MIL-STD-1553 Bus Controller and RTU hybrid with error detection and complete mode code capability. Includes dual encoder/decoder, dual bit processor, RTU protocol, BC protocol and DMA subsystem interface.	420
BUS-66106 and BUS-66111	1.9 x 1.6 x 0.2" Hybrid and 36 pin DDIP Hybrid	Provides protocol timing for a MIL-STD-1553 Bus Controller, validates the RTU Status Word and supports all 1553 message formats. Interfaces to a 16 bit data highway and a 6 bit address bus for DMA type handshake during message transfer.	422
BUS-66108	2.4 x 1.6 x .2" Hybrid	Provides complete protocol, timing and control functions for dual redundant MIL-STD-1553 RTU. Supports 13 Mode Codes, transfers data with DMA handshaking. Interfaces with 8 and 16 bit data highways. Separate latched outputs for Command word and Word Count.	434
BUS-68003	14.5 x 17 x 3.5" Instrument	Low cost MIL-STD-1553 Data Bus Exerciser with bus controller or dumb RTU operating modes. Generates and detects errors in accordance with MIL-STD-1553 for troubleshooting subsystems. Programmable via front panel keyboard, standard rear panel parallel I/O or optional IEEE-488 or RS-232 I/O.	444
BUS-68010	3.5 x 8.5 x 9.3" Instrument	Low-cost portable instrument for troubleshooting MIL-STD-1553 systems. Simulates functions of Bus Controller, Bus Monitor and Remote Terminal. Detects parity, sync type, and long/short word errors. Programmable to generate word format and word count errors, Broadcast/Mode Code and intermessage gap.	450

SUMMARY TABLE CONTINUED

Name	Form Factor	Features	Page
MT32008	48 pin DIP 48 pin Flat Pack 48 pin Chip Carrier	MIL-STD-1553 LSI Manchester encoder/decoder with flags for valid sync, proper Manchester II Coding, Bit Count, Own Address and Odd Parity. Encodes serial Manchester II data with sync and odd parity.	454
DBA-488	7-1/8 x 6-1/2 x 1-11/16" chassis	Data Bus Adapter controls the transmission of data, timing, and control signals between instruments and the IEEE-488 bus. Interfacing information stored in plug-in ROM. Available as a standard option for most DDC synchro instruments.	462
ADDENDUM			
BUS-65112	2.1 x 1.9 x 0.25" hybrid	MIL-STD-1553 dual redundant RTU hybrid including dual transceivers, dual encoder/decoder and RTU protocol. Supports 13 mode codes and transfers data with DMA type handshake.	A-6
BUS-66300	2.1 x 1.9 x 0.25" hybrid	Small intelligent MIL-STD-1553 to MIL-STD-1750 interface hybrid with buffer controls for 1750 address and 1553 data buses. Provides Command, Interrupt and Mode Control Word registers. Compatible with DDC standard product BUS-65600 BC/RT.	A-14

BACKGROUND INFORMATION

During the 1950s, military aircraft mission requirements reached such a level of complexity that they could no longer be satisfied with independent and self-sufficient electronics (avionics) subsystems. There was a recognized need for these subsystems to be integrated so they could share information and resources. By the mid 60s, avionics integration had caused a dramatic increase in the complexity of subsystem interfaces and in the size and weight of interconnecting cable bundles. Wiring is now so complex that modification and system testing are difficult and costly. Digital technology offers an obvious solution—time division multiplexing on a serial data bus (see Fig. 1).

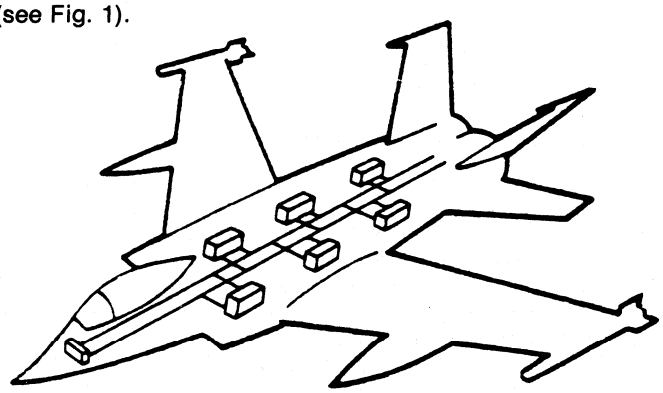


Fig. 1. Point-to-point wiring once used to integrate aircraft avionics, resulted in heavy cables and system complexity (above). The multiplexed data bus now being used to integrate avionics results in simplicity and flexibility.

In 1968, the SAE A2K Committee, with Tri-Service and other industry representation, was formed to generate a military standard for multiplexing. MIL-STD-1553—Military Standard Aircraft Internal Time Division Command/Response Multiplex Data Bus—was issued in 1973. The current revision, MIL-STD-1553B, came out in 1978. A tribute to its success is its widespread application in military programs—and the ready availability of interfacing components. Avionics integration in these applications is flexible, lightweight, and easily tested and modified.

MIL-STD-1553B characterizes all aspects of the data bus network—media, transmission technique, protocol, and terminal interface. The standard provides specifications detailed enough to ensure the interchangeability of equipment from numerous suppliers but flexible enough to allow multiple supplier designs.

TOPOLOGY AND MEDIA

A 1553B data network requires a bus topology that allows all subsystems coupled to the data bus to have access to all transmissions (see Fig. 2). Dual redundant data bus media provide fault tolerance with no single point failure mechanism. Short stub and long stub terminal coupling to the 1553B data bus is transformer-coupled for signal common mode rejection and uses isolation resistors for fault protection (see Fig. 3). Up to 31 terminals can be placed on a 1553B data bus, and each terminal can service up to 30 subsystems.

The data bus travels a shielded twisted pair cable. Its characteristic impedance (70 Ω), attenuation (1.5 dB/100 ft), and capacitance (30 pF/ft) are specified in 1553B along with numerous other parameters. Coupling characteristics are also specified—transformer turns ratio (1:1.4), input impedance (3k Ω), common mode rejection (45 dB), and data bus voltage (1 to 20 V pk-to-pk).

MIL-STD-1553B data bus transmissions are serial time division multiplex messages in pulse code modulation form. Bus traffic is half duplex, hence it travels in one direction at a time over one of the dual redundant cables. Either cable may be used for any message. Coded information samples are transmitted one bit at a time over the data bus.

The 1553B data bus network functions in a command/response sequence. Access to the data bus is provided only when a command is received by a terminal, at which time the terminal may respond—but only with the action the command requests. Central control of media access is the primary operating mode of the 1553B data bus, although a form of distributed control, called dynamic bus control, is possible. Essentially, dynamic bus control allows central control to pass from one terminal to another. Transmissions continue in a command/response fashion, after bus control has passed.

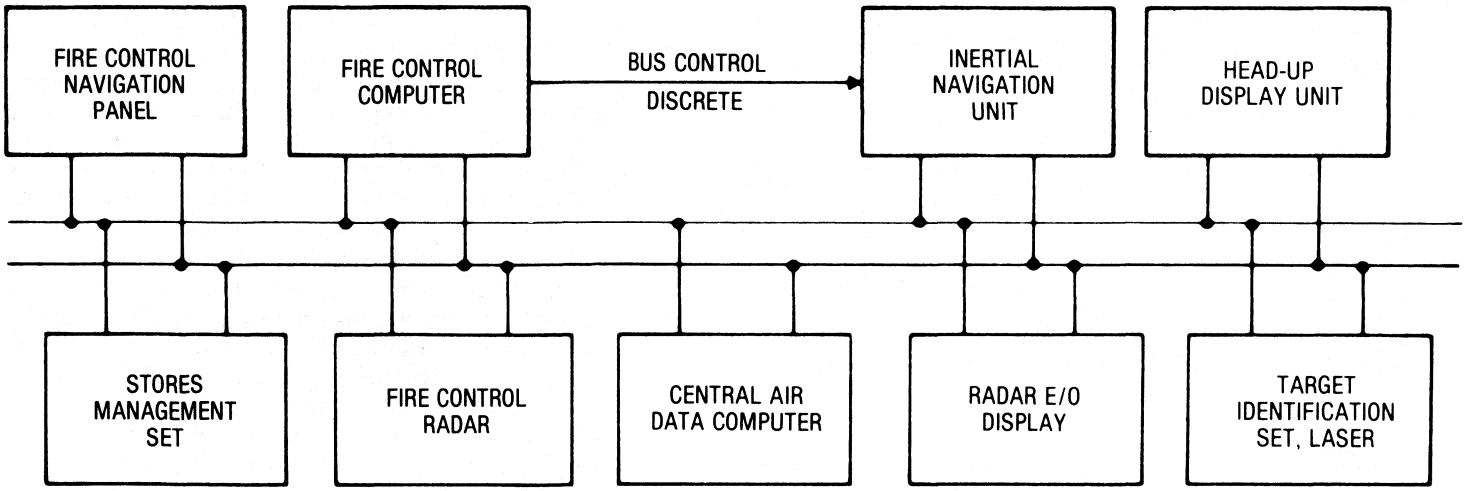


Fig. 2. The MIL-STD-1553B data network requires all data bus subsystems to have access to all transmissions.

TERMINALS

Three types of interfaces between subsystems and the data bus are provided—a bus controller, bus monitor, and remote terminal unit (RTU). A bus controller initiates message transfers on the data bus. A bus monitor receives bus traffic and extracts selected information to be used at a later time. Any terminal not operating as a bus controller or bus monitor is a remote terminal unit.

Terminal interface characteristics detailed in MIL-STD-1553 include limits for input and output voltage levels, input impedance, waveform fidelity, noise parameters, as well as short and long stub coupling conditions.

CODING METHOD

Transmissions on the 1553B data bus are coded in Manchester II biphase level form (see Fig. 4). Manchester coding is self-clocking with a zero crossing during each bit time. Having no DC voltage component, Manchester coding is ideal for the transformer coupling requirement of 1553B. Its noise rejection properties are superior to voltage level coding, since each bit requires a voltage transition. Manchester II biphase level coding also offers good error detection properties.

MIL-STD-1553B specifies a transmission bit rate on the data bus of 1 Mbit per second with a combined accuracy and long-term stability of ±0.1%. The short-term (1-s) stability is specified as ±0.01%.

Each word of a 1553B message requires an initial sync pattern, which is an invalid Manchester waveform 3 bits long. The sync pattern has a voltage transition at 1½-bit times. The phase of this sync pattern determines whether the waveform is a command and status waveform or a data waveform (see Fig. 5). If the first 1½-bit times are positive, it is a command and status type; if the first 1½-bit times are negative, it is a data type. This 3-bit sync pattern provides good noise immunity with a small message overhead.

The last bit of a 1553B word is an odd parity bit. Use of a single parity bit per word is compatible with undetected terminal bit error rate of 10^{-12} bps. Odd parity therefore provides good error detection with a minimum message overhead and is easy to implement.

MIL-STD-1553B requires a 4-μs gap between sequential messages. This intermessage gap time is measured between the mid-bit crossing of the RTU parity bit and the mid-sync crossing of the bus controller command sync (see Fig. 5).

Each bus controller command requires an RTU response of 4 to 12 μs. The RTU response time is measured between the mid-bit crossing of the bus controller parity bit and the mid-sync crossing of the RTU status sync. A terminal must wait 14 μs before considering that a no-response condition exists.

MIL-STD-1553B allows three word formats—command words, data words, and status words. Each consists of a 3-bit sync, 16 bits of data, and a parity bit (see Fig. 6).

Since 1553B uses a central control (command/response) protocol, only the bus controller can transmit a command word. The command word defines the format of the subsequent data bus message and contains the 5-bit address of the receiving or transmitting terminal, a transmit or receive command bit, a 5-bit subaddress/mode field, and a 5-bit word count/mode code field. the subaddress/mode field identifies 30 unique subsystem or memory locations. If the field contains 00000 to 11111, then a terminal management mode command has been received, and the subsequent word count/mode code field is interpreted not as a word count but as a mode code.

The data word's 3-bit sync pattern distinguishes it from command and status words. Following the sync field are a

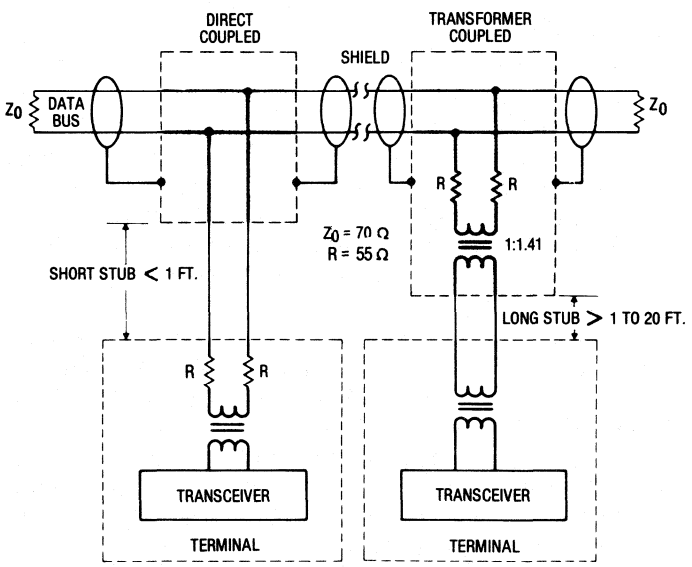


Fig. 3. The 1553B specs for data bus coupling require the data bus to be terminated at both ends, and the terminals to be transformer-coupled to the bus through isolation resistors.

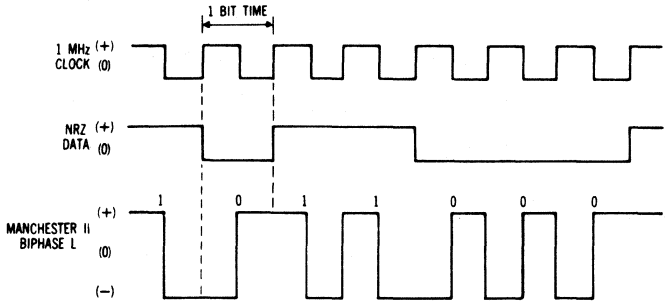


Fig. 4. Manchester II encoding provides the noise immunity benefits of a self-clocking code, with zero transitions during each bit time, and is ideal for transformer coupling.

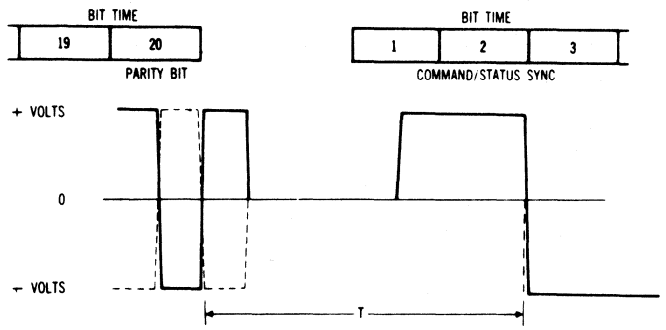


Fig. 5. The bus controller must provide a 4-us min gap between messages, and the remote terminal status response must be 4 to 12 μs.

16-bit data field and 1 parity bit. There are no restrictions on the data field, except that the most significant bit must be transmitted first.

A terminal transmits the status word acknowledgement during each message, except a broadcast message. The word acknowledgement contains a 3-bit sync field, the 5-bit address of the transmitting terminal, and numerous status bits. Remote terminal status is conveyed with message error, instrumentation, broadcast received, and terminal flag bits. Subsystem status is conveyed with service request, busy subsystem flag, and dynamic bus control acceptance flag bits.

MESSAGE FORMATS

MIL-STD-1553B provides for three categories of message formats—message transfers between two terminals, mode commands for terminal management, and broadcasts to all remote terminals. Figure 7 illustrates 5 of the 10 possible message formats. Each message may contain as many as 32 data words.

In bus-controller-to-remote-terminal transfers, the bus controller transmits the receive command and data words contiguously (no gap). After the elapsed response time, the remote terminal acknowledges the status word. Before the next command can be executed, there must be an intermessage gap.

In remote-terminal-to-bus-controller transfers, the bus controller sends the transmit command. After the elapsed response time, the remote terminal transmits the status word and data words contiguously.

Receive and transmit mode commands may contain up to one data word. Broadcast commands require all remote terminals to receive the message. The data may originate from the bus controller or any remote terminal.

MIL-STD-1553B specifies that the transfer of data bus messages be transparent to the user subsystem. Management of data bus traffic is the responsibility of the bus controller and remote terminals. Mode commands are used by the bus controller as a tool for data bus management and may contain any of the 15 assigned mode codes (see Table on page 316). Mode codes are divided into data-word and no-data-word categories.

A number of mode codes are assigned for terminal testing and error recovery routines. If the bus controller receives a status word response with the message error bit set, it can branch to an error handling sequence. Error handling sequences may contain mode codes such as transmit status word, transmit last command, initiate self-test, transmit bit word, or shut down transmitter. If the fault condition has been eliminated, normal message transfers resume.

TERMINAL OPERATION

Each type of terminal provides an interface between the serial data bus and the subsystem. Terminal operation can be partitioned into functional blocks of transceiver, encoder/decoder, protocol, and subsystem interface (see Fig. 8).

The transceiver contains the analog transmitter and receiver functions required to interface directly to the data bus, and the receiver portion contains the signal limiting, filtering, and threshold detection circuits that meet the data bus error rate requirements. The transceiver receives an analog signal from the transformer and outputs a serial digital Manchester coded signal to the decoder. The transmitter portion contains the circuits required to drive the data bus load with a trapezoidal waveform, as well as a timer to prevent "chattering" on the data bus.

The digital encoder and decoder functions required to translate messages to and from Manchester II format reside in the encoder/decoder. The decoder also provides word error checking on each 20-bit word received. It must flag invalid conditions of sync, Manchester coding, bit count, and parity. After the decoder validates the word, it flags the command/status or data word received and outputs the 16-bit digital word. The encoder controls the transmitter and generates the parity bit and command/status or data sync required for the 20-bit word.

The protocol circuits provide the terminal intelligence that manages the data bus transfers. In the receive mode, the circuits decode and validate the received address, then decode and act upon the received command or status word. If the command word is a mode command, the protocol circuit initiates appropriate action. Invalid word count and message errors are flagged in the protocol circuits. In the transmit mode, the protocol circuit formats the message, including status and data words. The circuit also controls the built-in test function and subsystem interface.

The subsystem interface contains the circuits required to transfer messages between the 1553B terminal and the subsystem. Typical functions are buffer storage, interrupt generation, and timing and control of subsystem handshaking.

The MIL-STD-1553B is a mature standard that has been imposed on various military programs. Therefore, numer-

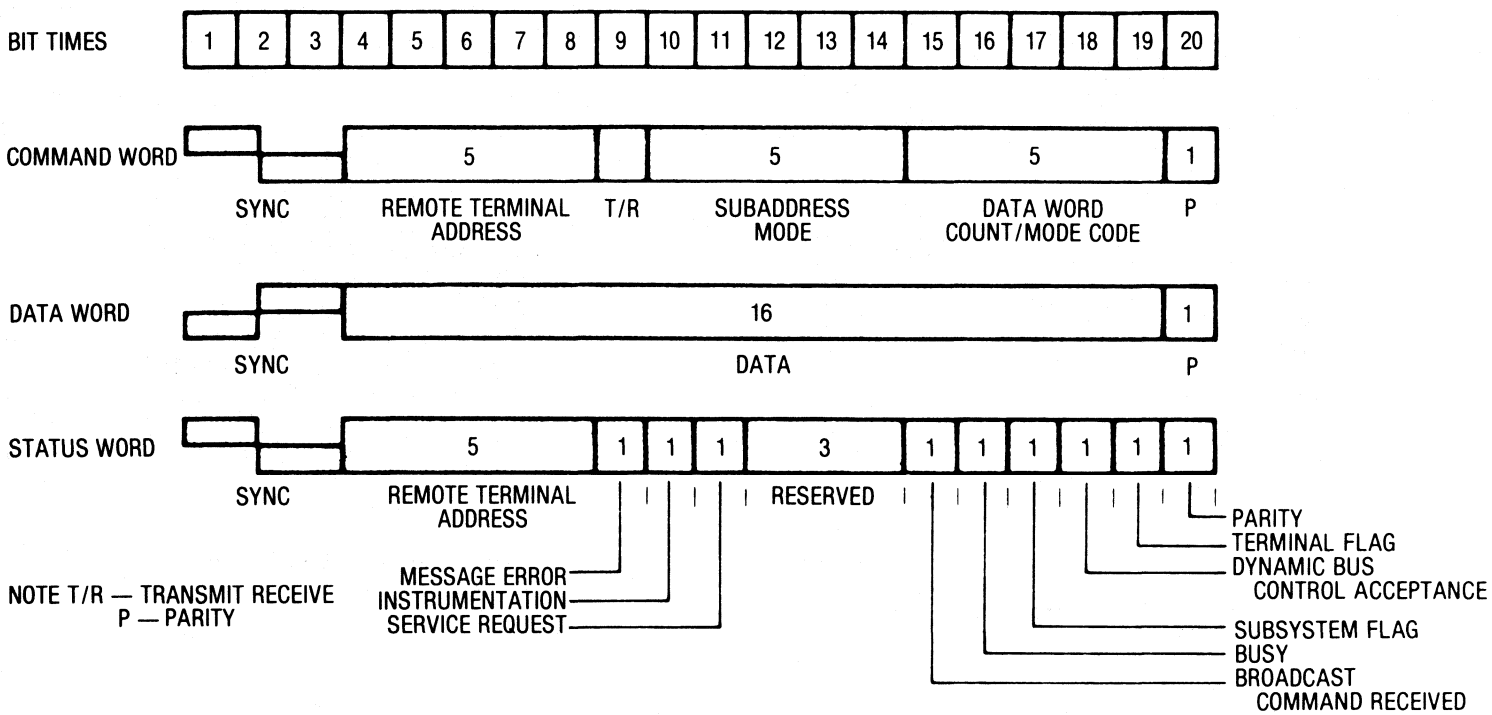


Fig. 6. Word formats allowed by 1553B include command words from bus controllers, status words from remote terminals, and data words from both.

ous suppliers have introduced components that can be used to implement bus controller, RTU, and bus monitor functions. The transceiver, encoder/decoder, protocol, and subsystem interface functional blocks have been implemented with sets of monolithic ICs and hybrid circuits.

Power requirements and circuit complexity have created a need for multiple chip 1553B terminals. The requirement to drive a 100-mA load at 30 V pk-to-pk has made it necessary for bipolar technology to be incorporated into 1553B transceivers. (By comparison, encoder/decoder and protocol circuits have been implemented in low power CMOS ICs. The protocol circuit, due to its complexity, has thus far warranted a separate IC.)

These multiple IC designs are often packaged in a single hybrid circuit—the ILC Data Device remote terminal components, for instance—to meet the small-size requirements of airborne military equipment. Figure 9 shows a 1553B remote terminal achieved by packaging monolithic ICs in a single package BUS65122 hybrid circuit.

Summarizing, the success of MIL-STD-1553B as a widely used local network standard for the military can be attributed to a number of important factors. First off, Tri-service as well as industry participation in creating 1553B resulted in a consensus of requirements. Secondly, detailed specifications for the data bus media and terminal interface resulted in the interchangeability of suppliers' hardware. And last but certainly not least, imposition of the 1553B standard on a number of military programs resulted in multiple suppliers.

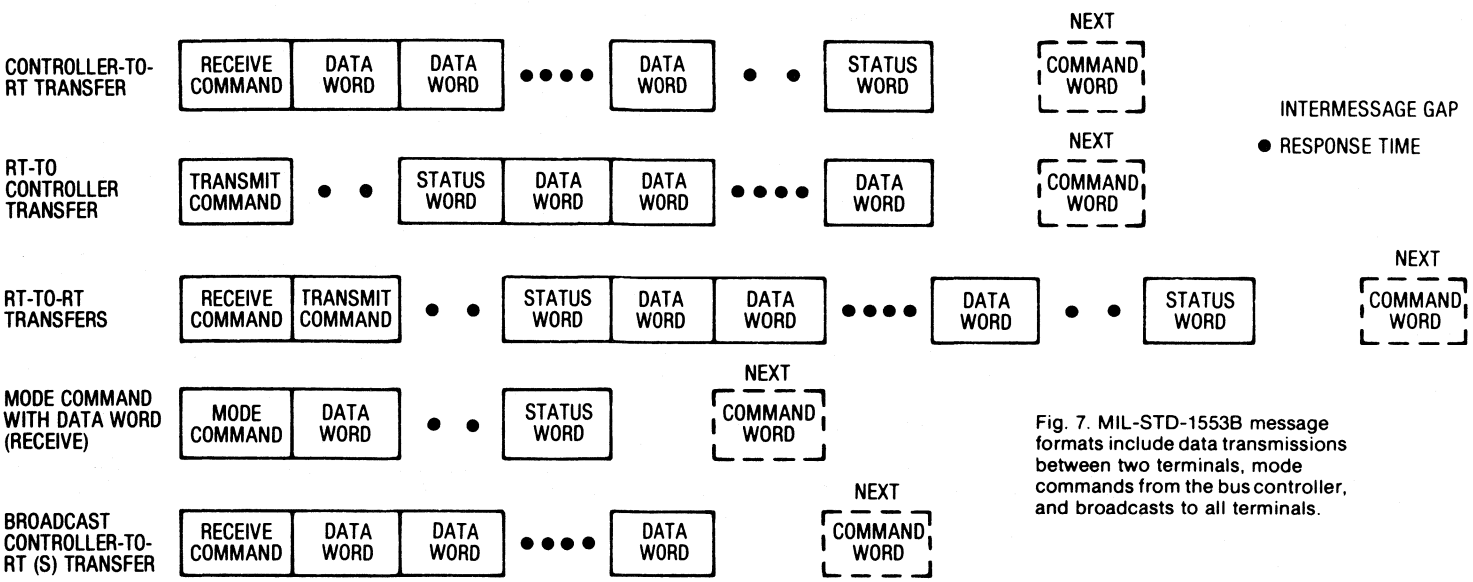


Fig. 7. MIL-STD-1553B message formats include data transmissions between two terminals, mode commands from the bus controller, and broadcasts to all terminals.

Mode Codes for MIL-STD-1553B

Transmit-receive bit	Mode code	Function	Associated data word	Broadcast command allowed
1	00000	Dynamic bus control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit data word	No	No
1	00011	Initiate self-test	No	Yes
1	00100	Transmitter shutdown	No	Yes
1	00101	Override transmitter shutdown	No	Yes
1	00110	Inhibit terminal flag bit	No	Yes
1	00111	Override inhibit terminal flag bit	No	Yes
1	01000	Reset remote terminal	No	Yes
1	01001	Reserved	No	TBD
1	01111	Reserved	No	TBD
1	10000	Transmit vector word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit last command	Yes	No
1	10011	Transmit bit word	Yes	No
0	10100	Selected transmitter shutdown	Yes	Yes
0	10101	Override selected transmitter shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
1 or 0	11111	Reserved	Yes	TBD

Note: TBD – to be determined

Assigned mode codes help the terminals manage data bus message traffic.

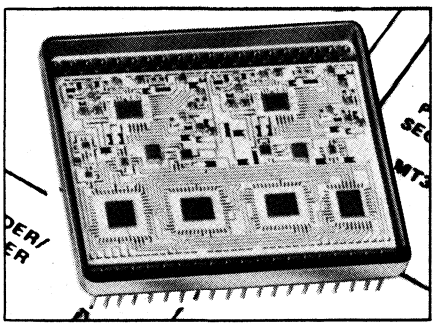


Fig. 9. Remote terminal hardware can be implemented in a single hybrid circuit to meet military requirements.

IEEE-488 DATA BUS STANDARD

INTRODUCTION

In an attempt to standardize instrumentation interfaces, used in Automatic Test Equipment, the Institute of Electrical and Electronic Engineers has advocated the adoption of the IEEE-488-1975 Digital Interface for Programmable Instrumentation.

THEORY OF OPERATION

Generally, the IEEE-488 Standard is described as a method to interface many instruments of various designs and data formats to a single predetermined data bus configuration; thus facilitating instrument hardware compatibility. This is accomplished through 16 hard wire lines and a standard connector. Eight lines are used for handling bi-directional data transmissions. Three handshake control lines handle the required timing of transmissions on the bus. The data transfer rate is mandated by the slowest listener in the system. Five interface management lines handle the remaining functions, such as type and condition of information (command or data) being transferred on the bus.

DBA-488 DATA BUS ADAPTOR

The DBA-488 Data Bus Adapter (page 462) is a standard option available for use with DDC's Synchro Instruments SR-103/HSR-103, SR/HSR-102A and SR/HSR-202, and SR-400/460.

APPLICATION NOTES

The following application notes are available upon request:

- o THE MILITARY STANDARD FOR AVIONICS INTEGRATION
- o MIL-STD-1553 BUS MONITOR
- o MANCHESTER CODING DATA BUS
- o 1553 DATA BUS DESCRIPTION

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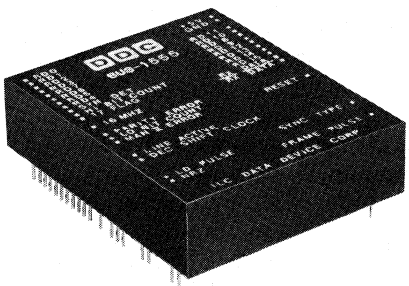


MIL-STD-1553 MANCHESTER II DECODER FOR TEST EQUIPMENT

DESCRIPTION AND APPLICATIONS

Providing enhanced bit error capability and precise message error detection, the BUS-1555 Manchester II Decoder Module avails itself to a wide range of applications. The decoder is encapsulated in a 3.1 x 2.6 x 0.8 inch module and is compatible with receivers designed to meet MIL-STD-1553 A/B, DDC Models BUS-63105 and BUS-8559 are directly compatible with this decoder.

The BUS-1555 will sample Manchester II input data at 16 MHz, which improves bit recognition and overall system capability. Error flags are provided for low and high bit count, odd parity and Manchester II phasing errors. Control logic outputs include Line Active, Frame, Sync Detector, Sync Type and Load Data Pulses. Internal logic may be initialized by means of the Reset Input function (see figure 1). The power supply input range is +4.5V to +5.5V and nominal power dissipation is 2.5 watts. The input is biphase TTL complementary serial data, which is decoded and output as both 16 bit TTL parallel and NRZ serial data.

The BUS-1555 is well suited for use in MIL-STD-1553 test equipment and as a data bus monitor terminal where subsystem listening devices are used. Applications include both ground and on board avionics system.

FEATURES

- *16 MHz CLOCK RATE*
- *ERROR FLAGS FOR SYNC MANCHESTER II ERROR HIGH AND LOW BIT COUNT*
- *CONFORMS TO MIL-STD-1553 A & B*
- *16 BIT PARALLEL AND NRZ SERIAL OUTPUTS*

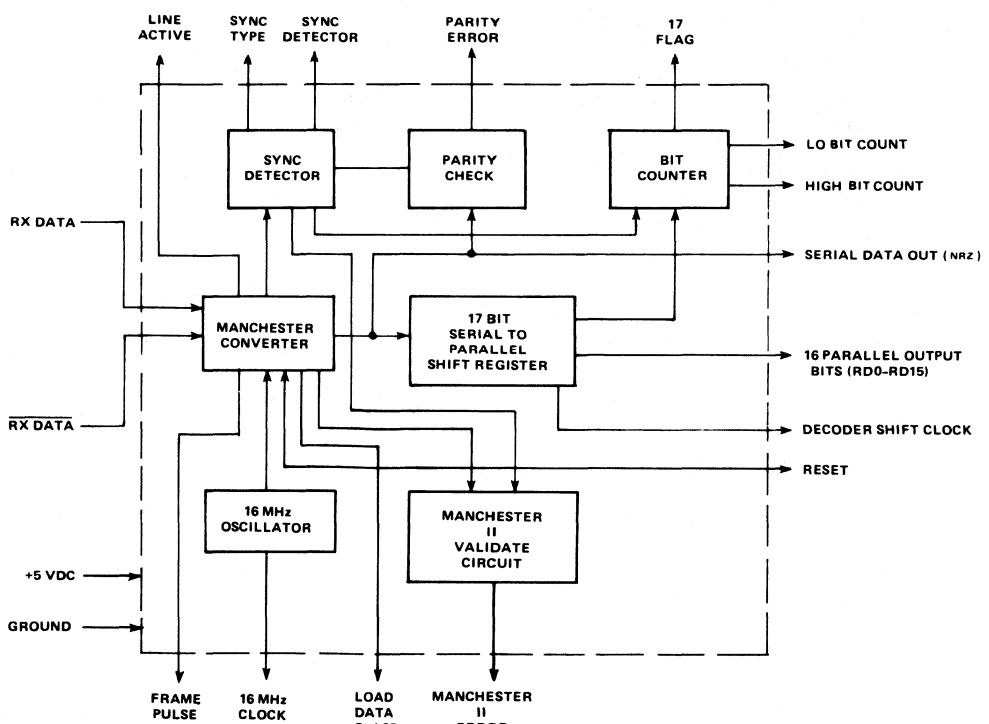


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS		
PARAMETER	**UNITS**	**VALUE**
INTERNAL CLOCK OUTPUT		
Oscillator Type	TTL	As per MIL-STD-1553B Long and short term stability
Frequency	MHz	16 ±1000 Hz
Cross over variation	ns	±150
Drive capability	TTL	1 LS load
DIGITAL IN/OUTPUTS		
Serial Data Input	Bits	Complementary TTL bi-phase nonreturn zero, Manchester II format
	TTL	3 LS loads
PARALLEL DATA		
RDO-RD15	TTL	16 bit parallel positive logic (RD15 = MSB)
Drive Capability		8 LS loads (RDO-RD15 each)
Decoder Shift Clock Output	TTL	Synchronous output with respect to serial NRZ data output
Drive Capability	TTL	1 LS load
Control Logic	TTL	See pin connection for fan in/out and loading specifications
POWER SUPPLY CHARACTERISTICS		
Voltage Input Range	V	+4.5 to 5.5
Current	A	0 5 max @ +5V nominal
TEMPERATURE RANGE		
Operating	°C	0 to +70
Storage	°C	−55°C to +125°C
PHYSICAL CHARACTERISTICS		
Size	in.	3.1 x 2.6 x 0 8 (78 x 66 x 20mm)
Weight	oz	6 (170g)

GENERAL DESCRIPTION

Figure 1 is a block diagram of the BUS-1555, illustrating its functions of Manchester decoding, sync detection, serial to parallel conversion, and validation of MIL-STD-1553 Manchester coding, sync, parity and bit count. Use of a 16 MHz clock to sample the complementary (RX and $\overline{RX}$) biphase Manchester data results in improved bit recognition and enhanced overall error detection. In accordance with MIL-STD-1553A and B, error free reception consists of a 20 μsec word, with a 3 μsec sync field, followed by a 16 μsec data field, followed by a 1 μsec parity bit. In addition, the sync field must be 2 equal 1.5 μsec halves, and the data field and parity bit must be valid Manchester coding.

The error detection sequence starts with recognition of a valid (command or data) sync (figure 2), and ends with a BUS-1555 Load Data output pulse. Activity on error flag outputs is to be ignored except during the Load Data pulse interval. Upon receipt of a valid sync, the Sync Detect line goes high and the Frame Pulse Line is pulsed. After a valid sync, the next data bit time (1 μsec) is checked for a valid Manchester transition. If a Manchester error has occurred in the first data bit, the Manchester error flag is activated, the low bit count error flag is inhibited, and a Load Data pulse is generated at the end of the frame. If the first data bit passes the Manchester test, the remaining 16 bits are checked for Manchester, bit count and parity.

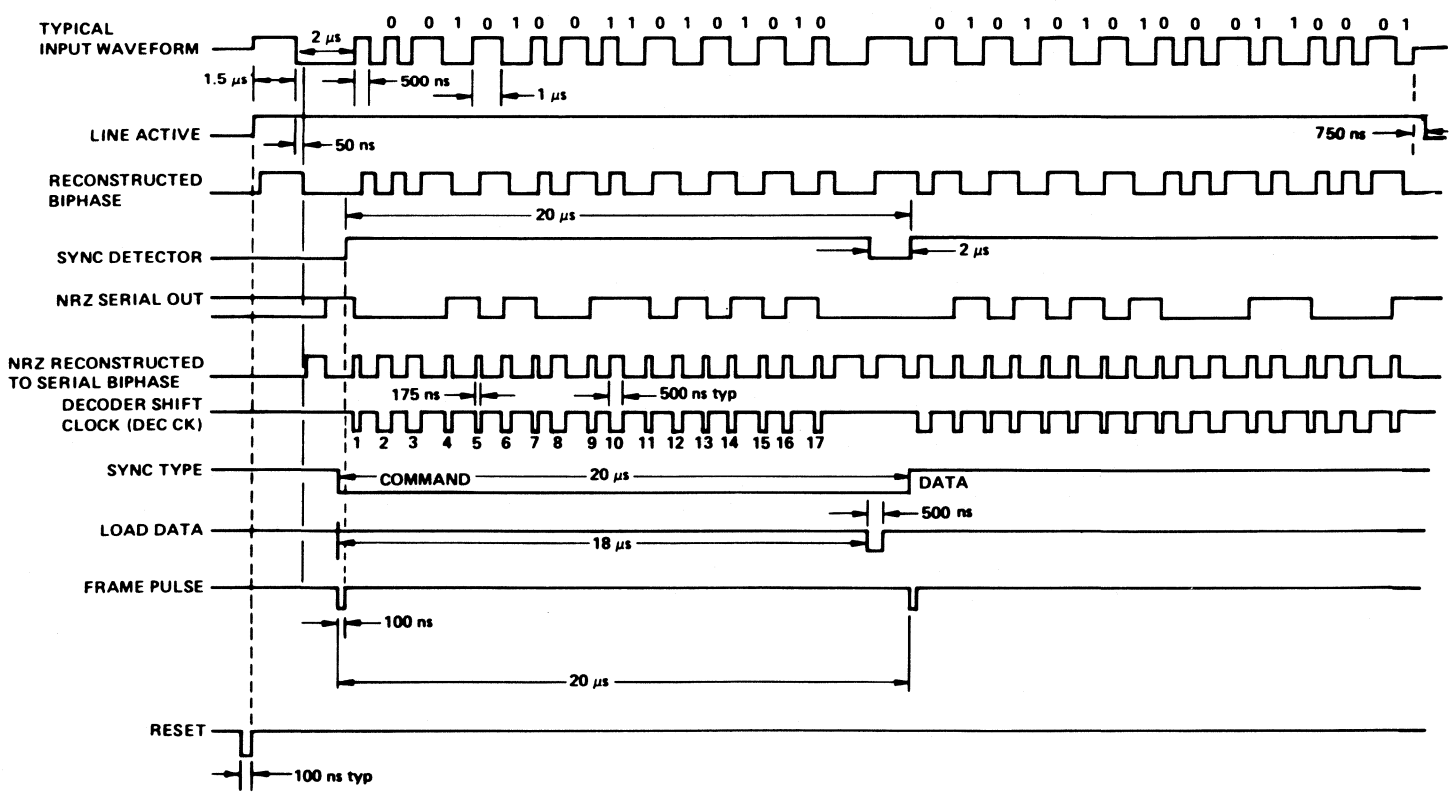


FIGURE 2. DECODER TIMING DIAGRAM

Pin Function Table

PIN	DESCRIPTION	LOADING	FAN IN/OUT
RX DATA	Receiver Data (TTL)	3	In
$\overline{\text{RX DATA}}$	Receiver Data (TTL)	3	In
LINE ACTIVE	Monitors the data bus data and interprets valid activity. The output goes high when a valid sync on both RX and $\overline{\text{RX}}$ inputs is identified. It remains high if successive words are received and will go low 750 nanoseconds after the last bit of a valid word.	6	Out
FRAME PULSE	Identifies when a valid sync field has been detected and its trailing edge is coincident with the positive going edge of the SYN DET output.	6	Out
SYNC TYPE	Indicates received sync field polarity, outputs a low for command or status sync, and a high for data sync.	10	Out
16 MHZ	16 MHz clock	1	Out
SYN DET	Sync Detector outputs a high when a valid sync field has been recognized, a low when the first half of the following sync field is recognized or a last bit of the last word has occurred. When the signal goes low between consecutive 20 bit words it will again go high when the complete valid field has been recognized.	7	Out
LD PULSE	Load Data is a positive pulse signaling the end of a decoded word. It samples all error flags and should be used to transfer error flags into holding registers.	10	Out
PARITY ERROR	Is valid for 17 bits only. It outputs a logic "1" during Load Data pulse sample time, if there is a parity error.		
MAN II ERROR	Manchester II Error flags invalid Manchester coding on data and parity bits only and does not include the sync field. It checks for at least one transition per data and parity bit. A logic "1" level on this line at Load Data pulse sample time indicates Manchester II Error.	10	Out
17 FLAG	Indicates a bit count of 17 and will be a logic "1" when this condition is true. This line shall also be sampled at Load Data pulse time.	10	Out
LO BIT COUNT	Indicates less than 17 bits are contained within the decoded waveform. A logic "1" will indicate this condition. The Load Data pulse is the sample pulse to be used for ascertaining this condition.	10	Out
HI BIT COUNT	Indicates greater than 17 bits are contained within the decoded waveform. A logic "1" will indicate this condition. The Load Data pulse is the sample pulse to be used for ascertaining this condition.	10	Out
NRZ	Is serial data output in non-return to zero format and represents the decoded data that is being shifted into the serial to parallel internal shift register.	7	Out
RD0-RD15	Parallel Data Out consists of 16 bits referred to as RD0-RD15, with RD15 being MSB. This is not latched data and is valid only if 17 bits are sent and all validation checks pass. Data shall be sampled at the Load Data pulse time.	8	Out
DEC SHIFT CLK	Decoder Shift Clock is the "sync'ed clock line output for the serial data out (NRZ). There will be a maximum number of 17 clock pulses out on this line regardless if greater than 17 bits are sent and detected. For less than 17 bits the number of clock pulses resulting on this line will be equal to the number of bits sent.	1	Out
RESET	Reset pulse is an active low signal that resets the module.	1	In

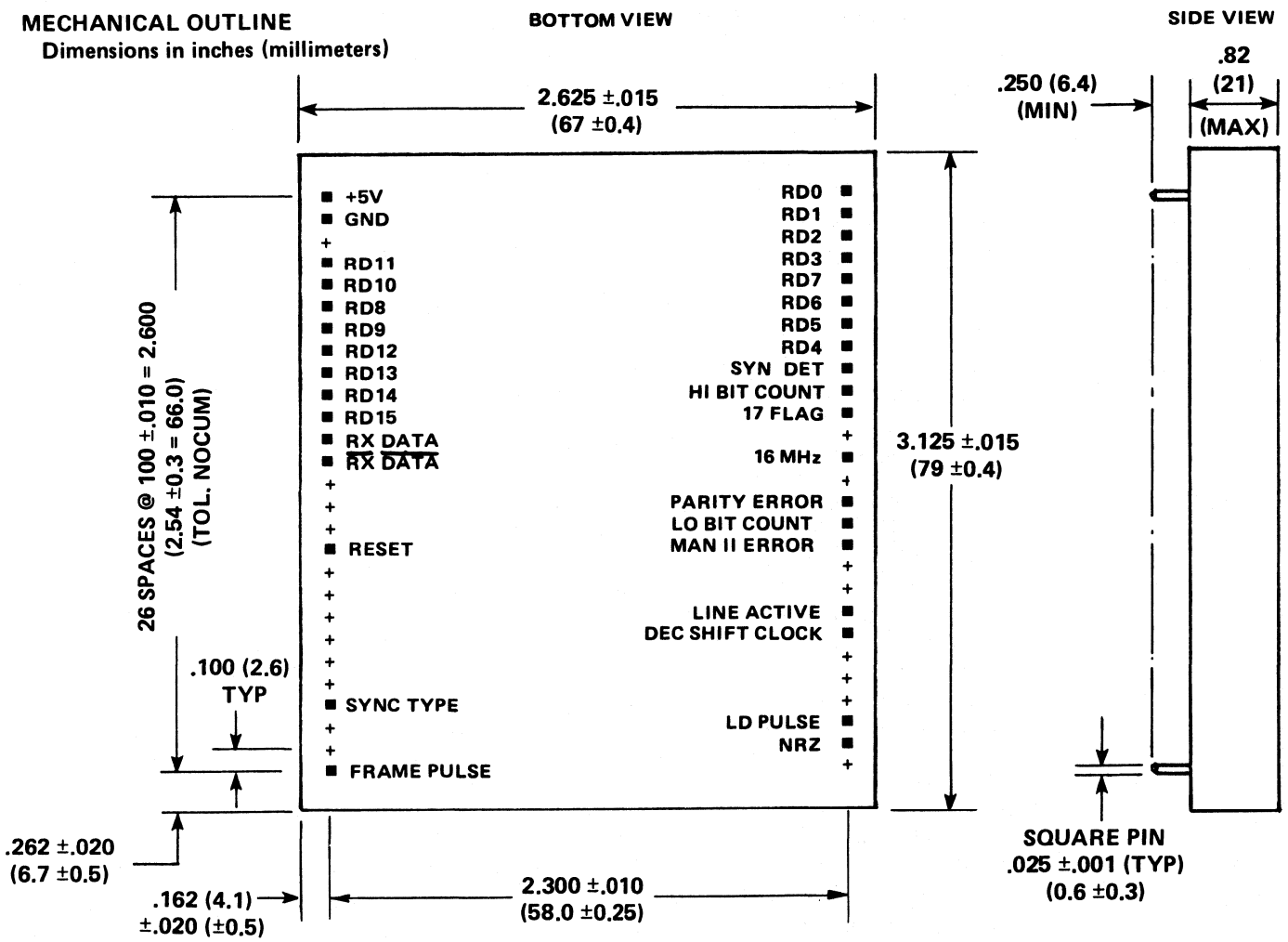
A Manchester error at any bit time takes highest priority. It causes the low bit count error flag to be inhibited, the Manchester error flag to be activated, and a Load Data pulse to appear at the end of the frame.

It is to be noted that the BUS-1555 continues to monitor the input for valid sync after the error checking sequence has begun. As a result of this this, a bit time ending with no Manchester transition present, and 1.5 μsec elapsed since the last Manchester transition, will be interpreted as half of a sync field. Under these conditions the bit counter will not be incremented, and if the second half of the sync field doesn't occur, a low bit count error flag will result. If a bit time ends with no Manchester transition present, and 1.0 μsec elapsed since the last Manchester transition, a Manchester error flag will result.

The valid word indicator is referred to as the 17 flag. This flag is activated when there are 16 data bits plus 1 parity bit valid Manchester transitions. The Parity Error flag is only valid when the 17 flag has been activated.

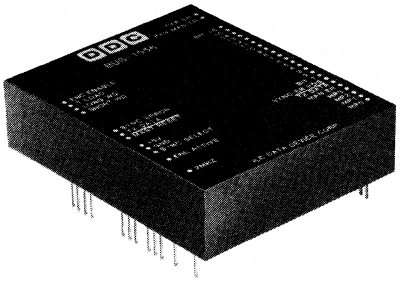
MECHANICAL OUTLINE

Dimensions in inches (millimeters)



ORDERING INFORMATION

Order: BUS-1555



MIL-STD-1553 ENCODER
Generates Errors For Test Equipment

DESCRIPTION

The BUS-1556 MIL-STD-1553 Encoder is a versatile building block, featuring capability for generating a number of different error types. The Manchester encoder is encapsulated in a 3.1 x 2.6 x 0.8 inch module and is compatible with transmitters designed to meet MIL-STD-1553 A/B. (DDC models BUS-63105 and BUS-8559).

The BUS-1556 converts 16-bit parallel input data to a Manchester II encoded serial output. All timing is derived from an externally supplied 2 MHz clock. The encoder outputs error-free data words or it may be pin programmed to output words containing one or more encoding errors. The errors generated by the BUS-1556 include Manchester II error in any of the 16 data bits, and parity bit positions; parity error, long word (one extra bit) error, short word (one missing bit) error, and two different forms of sync field errors.

A Master Reset pin for initialization, an Encoder Enable input, an Encoder Active and T Load outputs are provided for handshaking with a parallel subsystem. Complementary bi-phase serial data output is provided via the TX DATA and $\overline{\text{TX DATA}}$ pins. The power supply input range is +4.5 V to +5.5 V and nominal power dissipation is 2.5 watts.

APPLICATIONS

The BUS-1556 is intended for use in test fixtures as well as in Automatic Test Equipment (ATE) for testing MIL-STD-1553 A/B monitors, bus controllers and remote terminals. Applications include both ground support and on-board avionics systems.

FEATURES

- *ENCODES PARALLEL DATA INTO SERIAL MANCHESTER*
- *ERROR GENERATION CAPABILITY:*
  - *MANCHESTER CODING ERROR*
  - *PARITY ERROR*
  - *HIGH BIT COUNT ERROR*
  - *LOW BIT COUNT ERROR*
  - *SYNC FIELD ERROR*
- *CONFORMS TO MIL-STD-1553 A AND B*
- *USED IN TEST SYSTEMS WITH BUS-1555 DECODER*

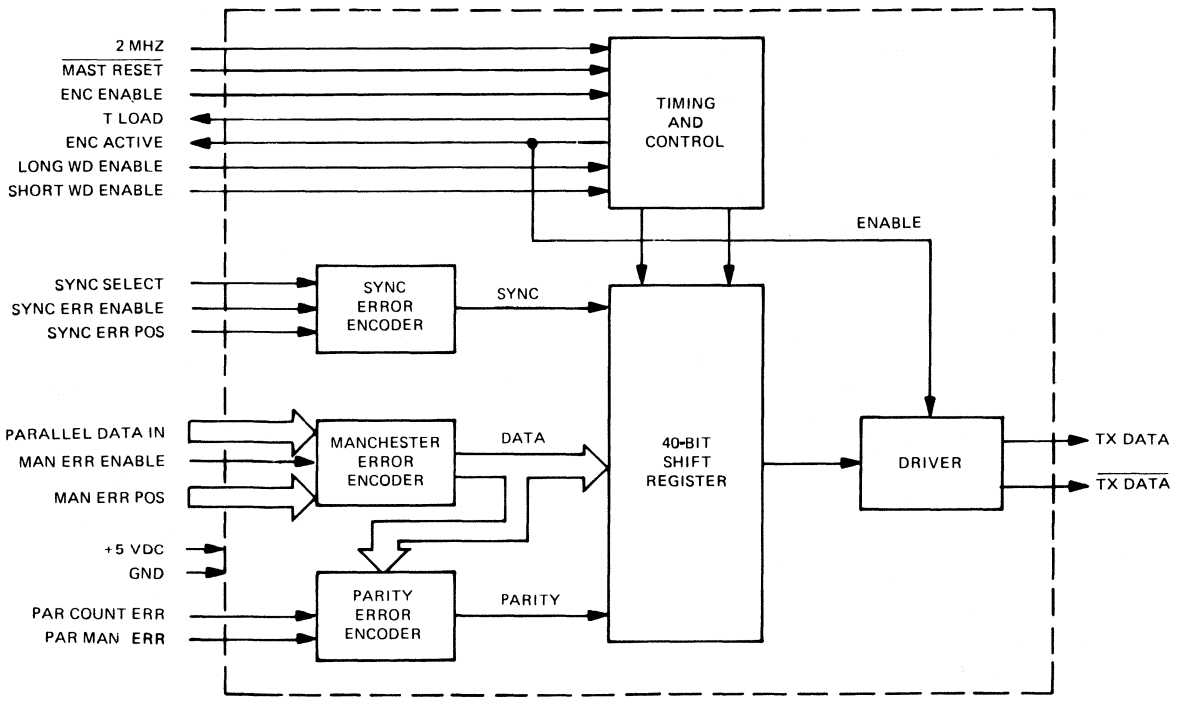


FIGURE 1. BUS-1556 BLOCK DIAGRAM

SPECIFICATIONS		
PARAMETER	**UNITS**	**VALUE**
EXTERNAL CLOCK INPUT		
Oscillator Type (2 MHz)	TTL	As per MIL-STD-1553 A/B long and short term stability requirements
Frequency	MHz	2.000 ± .001
Crossover Varation	ns	±150
Loading		1 LS TTL load
PARALLEL DATA INPUT		
Bit 1 (MSB)-Bit 15 (LSB)	TTL	16-bit parallel positive logic
Loading		2 LS TTL loads
SERIAL DATA OUTPUT		
TX DATA and $\overline{\text{TX DATA}}$	TTL	Complementary TTL Manchester bi-phase II format
Fan-Out		5 Standard TTL loads
POWER SUPPLY CHARACTERISTICS		
Voltage Input Range	V	+4.5 to +5.5
Current	A	0.65 max., 0.4 typ
TEMPERATURE RANGE		
Operating	°C	0 to + 70
Storage	°C	—55 to + 125
PHYSICAL CHARACTERISTICS		
Size	in	3.1 x 2.6 x 0.8 (78x66x20mm)
Weight	oz	6 (170g)

TECHNICAL INFORMATION

The BUS-1556 error-generating encoder operates in accordance with MIL-STD-1553 A/B to convert 16 bit parallel TTL input data to TTL Manchester II encoded complementary bi-phase serial output (TXData and $\overline{\text{TXData}}$). The encoder may be programmed for either normal operation, or to generate words containing one or more of the following error types: Manchester II encoding error, parity error, sync error, high bit count and low bit count. Each normal outputted serial word consists of a 3μs. sync field, sixteen 1μs. data pulses and one 1μs. parity pulse. Some words programmed to contain errors will deviate from this pattern.

All module timing is derived from an externally supplied 2MHz clock. Thirty-two TTL lines interface to a parallel subsystem. These include the 16 bit parallel input data (Bit 1-Bit 16), Sync Select, six error control lines (Manchester Error, Parity Error, Parity Manchester Error, Sync Error, Long Word and Short Word), five error modifying lines (Manchester Error Position 0-3, Sync Error Position), and four handshaking lines (Encoder Enable and Master Reset inputs; T-Load and Encoder Active outputs). TXData and $\overline{\text{TXData}}$ provide the complementary bi-phase TTL input to a MIL-STD-1553 A/B compatible transmitter. Normal transmitted words are sent when all error control lines are low. Erroneous words are sent whenever one or more of the error control lines are asserted high.

PIN FUNCTION TABLE

PIN	DESCRIPTION	LS LOADS
BIT 1–BIT 16	Parallel data inputs.	2
SYNC SELECT	A logic "1" input causes a Command/Status sync output. A logic "0" input causes a Data sync output.	4
2 MHZ	2MHz clock input.	1
ENC ENABLE	A 3 μsec minimum duration logic "1" input enables the start of a MIL-STD-1553 encoded output word.	1
$\overline{\text{MAST RESET}}$	A 100 nsec active low pulse input resets all encoder circuits.	1
MAN ER	A logic "1" input enables the generation of Manchester errors. The bit position of the error is determined by MP0-MP3.	2
MP0-MP3	Binary coded input representing the desired bit position of the Manchester error. A logic "1" input must be present on MAN ER to enable the function.	1
PAR ER	A logic "1" input causes a parity count error.	1
PAR MAN ER	A logic "1" input causes the Manchester error in the parity bit.	1
SYNC ERROR	A logic "1" input enables the generation of a sync error. The position of the error is determined by SYNC ER POS.	2
SYNC ER POS	A logic "0" input causes the sync transition to occur early. A logic "1" input causes the sync transition to occur late. A logic "1" input must be present on SYNC ERROR to enable the function.	2
LONG WD	A logic "1" input causes the encoded output word to contain one bit too many.	2
SHORT WD	A logic "1" input causes the encoded output word to contain one bit too few.	1
TX DATA	Serial Manchester coded MIL-STD-1553 output.	10
$\overline{\text{TX DATA}}$	Inverted Manchester coded MIL-STD-1553 output.	10
ENC ACTIVE	A logic "1" output signifies that the encoder is transmitting.	7
T LOAD	A 750 ns positive output pulse signifies that data and control inputs are being loaded into the encoder.	10

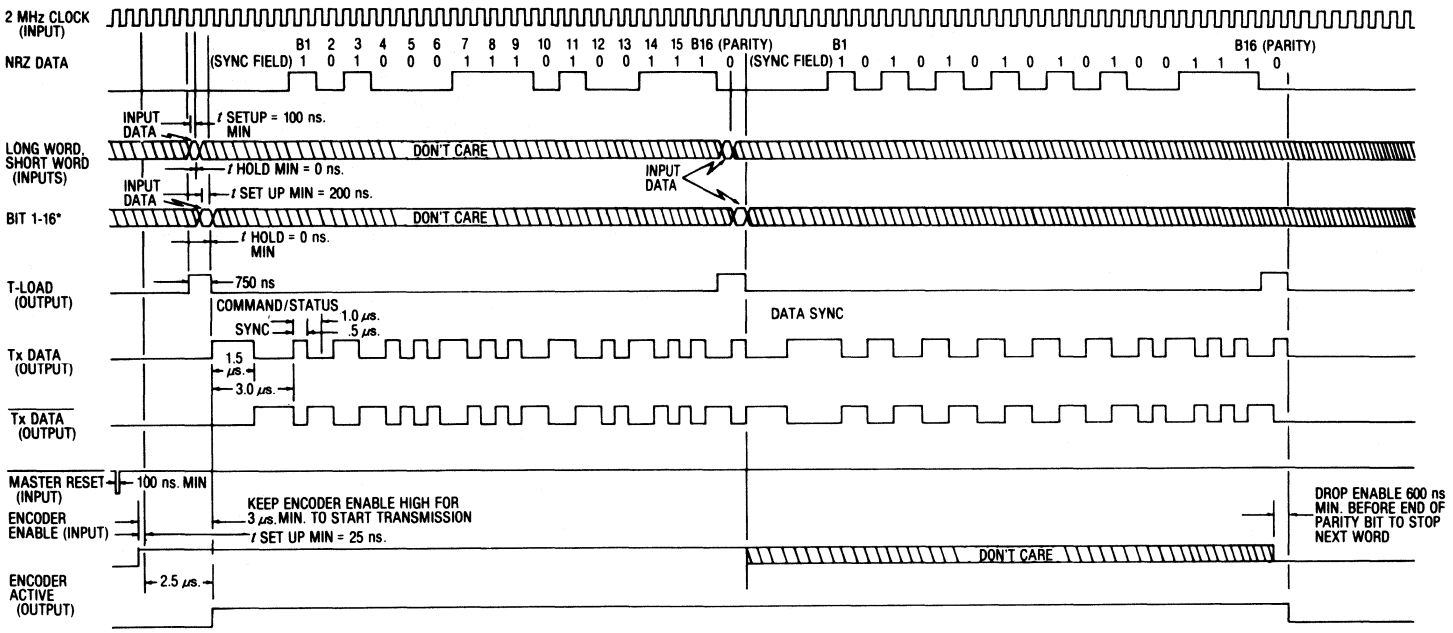


FIGURE 2. ENCODER TIMING DIAGRAM

*SYNC SELECT, SYNC ERROR, SYNC ERROR POSITION, MANCHESTER ERROR, MEP0-3, PARITY ERROR, PARITY MANCHESTER ERROR INPUTS ARE EXECUTED BETWEEN BIT TIMES 1-16

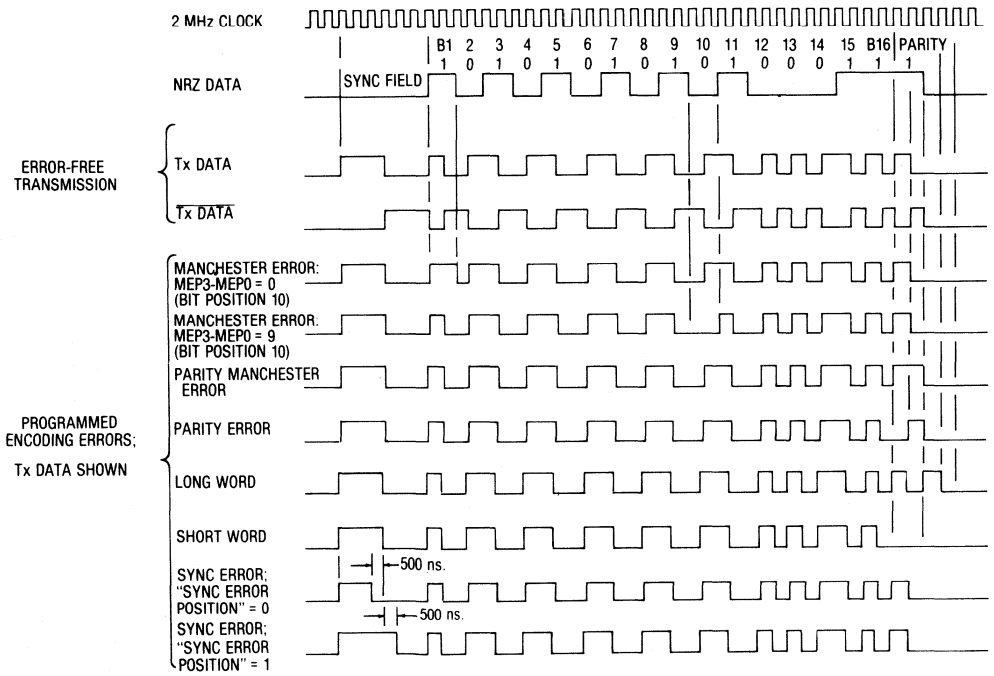
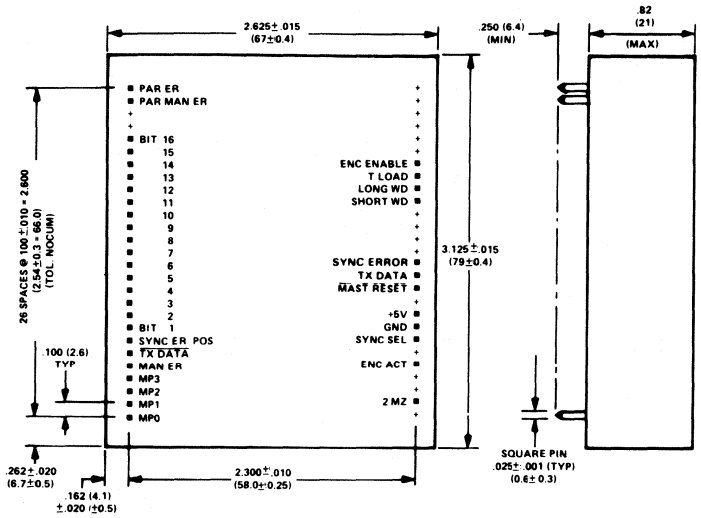


FIGURE 3. ENCODING ERRORS

MECHANICAL OUTLINE
Dimensions in inches (millimeters)



BOTTOM VIEW

TEST METHODS

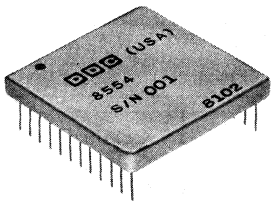
BUS-1556 converter modules are high quality products whose semiconductor components are hermetically sealed. These modules will meet the specific test methods and conditions of MIL-STD-202E shown unless alternative methods are specified by the customer in his procurement documentation.

ORDERING INFORMATION

Order: BUS-1556

Specifications are subject to change without notice.

MIL-STD-1553 TRANSCEIVER



FOR NEW DESIGNS USE
BUS-63104

DESCRIPTION AND APPLICATIONS

The DDC Model BUS-8554 Transceiver is a complete transmitter and receiver conforming to MIL standards 1553A and 1553B. The receiver section accepts phase-modulated bipolar data at the input and produces a biphase TTL signal at the output (Figure 1). The outputs, DATA and $\overline{\text{DATA}}$, represent positive and negative excursions of the input beyond an internally fixed threshold. These positive and negative thresholds are set at the factory for nominal 750mV p-p signal, measured at point A, Figure 2. External threshold levels of 0 to ±2V, p-p may be selected for specific applications by connecting 0 to 10k ohm resistors between pins 5, 12 and ground. An external strobe input is provided to allow the removal of the receiver from the line. A logic "0" applied to "STROBE" will disable the receiver output.

The BUS-8554 transmitter section accepts bi-phase TTL data at the input and produces a 30 volt nominal p-p differential signal across a 145Ω load. When coupled to the data bus with a 1:1 transformer, isolated (on the data side) with two 55.0 ohm fault isolation resistors, and loaded by two 70 ohm terminations (plus additional receivers), the data bus signal produced is 6.5 volts nominal p-p measured at point "A" (Figure 2).

When both DATA and $\overline{\text{DATA}}$ inputs are held low or high, the transmitter presents a high impedance to the line. An external inhibit input is provided to allow the removal of the transmitter output from the line (Figure 3). A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the transmitter.

The transceiver is available in a 24 pin hybrid package, measuring 1.25 x 1.25 x 0.2 inches, and can be used in any MIL-STD-1553 transceiver application.

FEATURES

- *1.25 x 1.25 x .17 SIZE*
- *MEETS ALL SPECIFICATIONS OF MIL-STD-1553A AND 1553B*
- *IMPROVED FILTERING ON RECEIVER TO ENHANCE BIT ERROR RATE OF SYSTEM*
- *TTL COMPATIBLE*
- *MEETS MIL-STD-883*

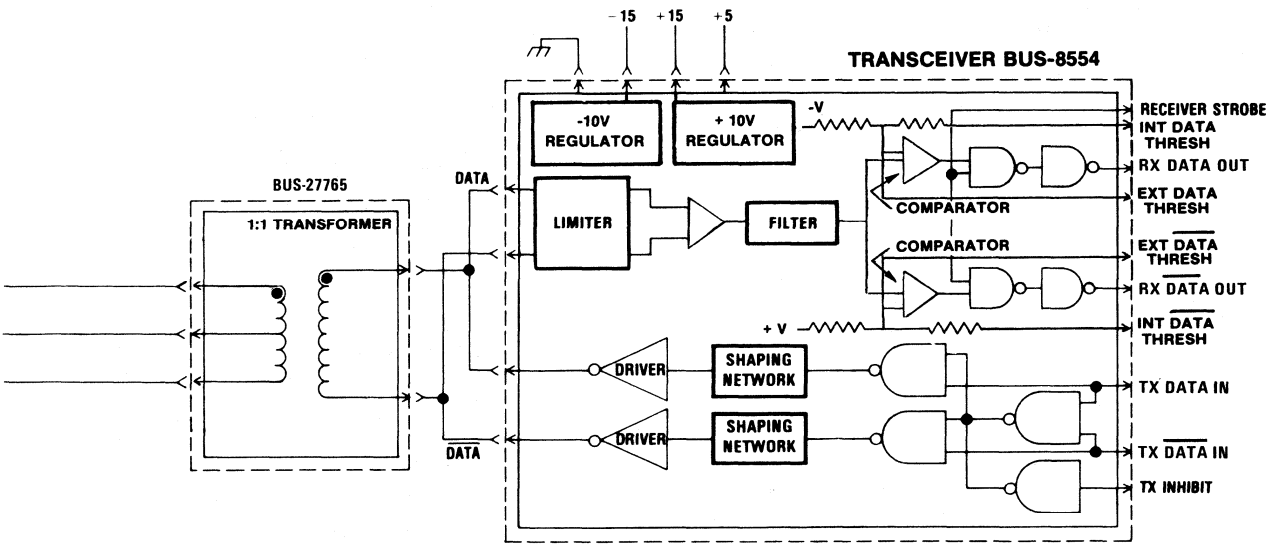


FIGURE 1. BLOCK DIAGRAM

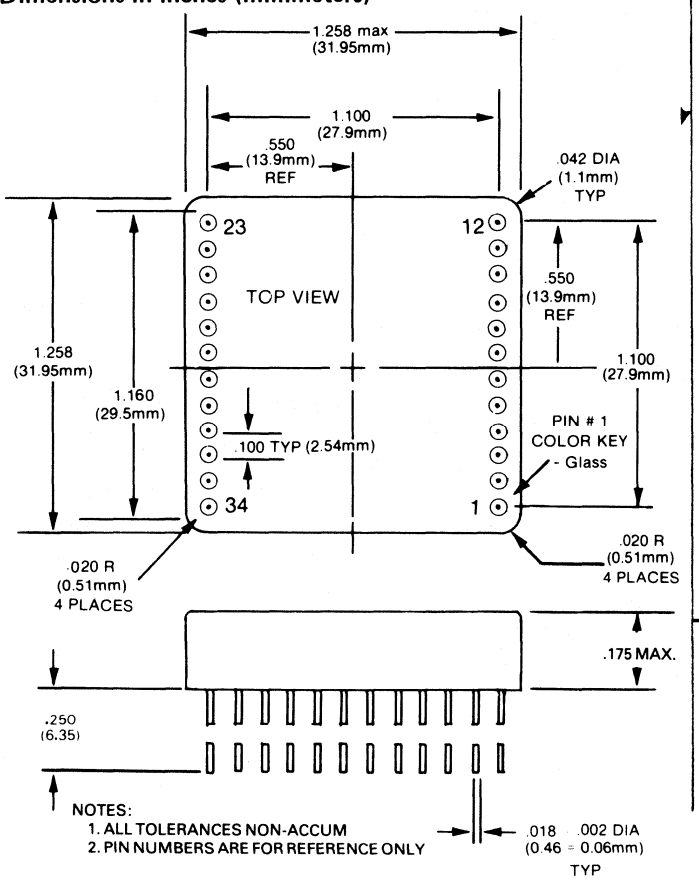
SPECIFICATIONS

PARAMETER	UNIT	VALUE
RECEIVER		
Input level	V	40 p-p differential max
Input Impedance	Ω	4K differential min
Threshold Level	mV	750 p-p nominal, internally set (direct coupled mode) Pins 6 and 11 grounded
Optional Threshold Adjust	V	0 to 2 p-p (0 to 10k ohm external between Pins 5, 12 and GND.
Output Level		TTL
Power Supply Requirements	V	±12 to ±15 (± 5% @ 30 mA max)
	V	+5 (± 10%) @ 15 mA max
TRANSMITTER		
Input Level		TTL
Output Level	V	30 p-p nom across 145Ω load
	V	21 p-p nom (measured at point C, Fig. 2)
Rise/Fall Time	ns	130 typ
Output Noise	mV	10 p-p differential max
Output Impedance (Receiver Mode)	Ω	>4K differential min (at 1 MHz with Transformer)
Power Supply Requirements	V	±15 @ 82 mA max @ 50% Duty Cycle
	V	+5 (± 10%) @ 15 mA max
GENERAL		
Operating Temperature Range	°C	-55 to +125 (case temp.)
Storage Temperature Range	°C	-55 to +135
Size (24 Pin hybrid)	in	1.25 x 1.25 x 0.2 (32 x 32 x 5mm)
Weight	oz	0.4 typ (11.39g)

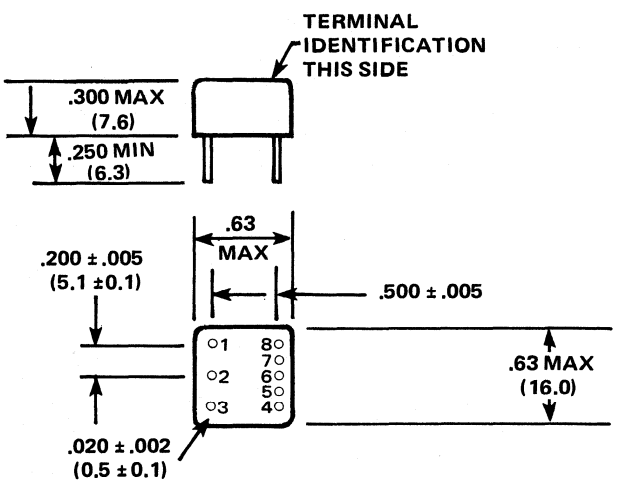
BUS-8554 PIN CONNECTION TABLE

PIN	FUNCTION
1	TX Data Out
2	TX $\overline{\text{Data}}$ Out
3	GND
4	+12V to +15VDC
5	EXT Data Thresh
6	INT Data Thresh
7	RX Data Out
8	Strobe
9	GND
10	RX $\overline{\text{Data}}$ Out
11	INT $\overline{\text{Data}}$ Thresh
12	EXT $\overline{\text{Data}}$ Thresh
23	+12 To +15V DC
24	N.C.
25	RX Data In
26	RX $\overline{\text{Data}}$ In
27	GND
28	GND (case)
29	-12 To -15VDC
30	+5 VDC
31	TX Inhibit
32	TX $\underline{\text{Data}}$ In
33	TX Data In
34	-12 To -15VDC

MECHANICAL OUTLINE BUS-8554
24 PIN SQUARE PACKAGE
Dimensions in inches (millimeters)



MECHANICAL OUTLINE
TRANSFORMER (P/N BUS-27765)



NOTES:
1. All dimensions are in inches (millimeters)
2. Pin callouts on bottom view are for reference only

ORDERING INFORMATION

ORDER:

BUS-8554-883

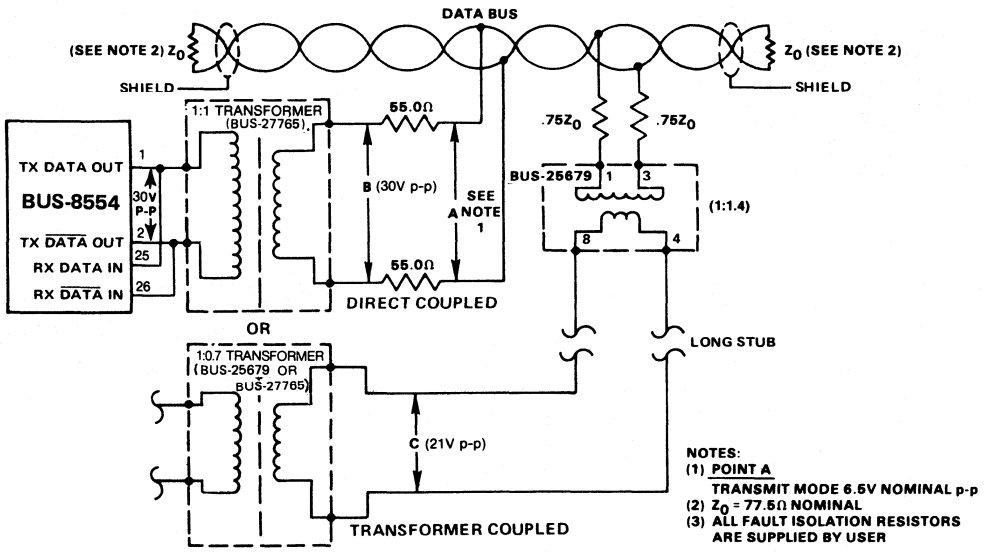


FIGURE 2. TYPICAL TRANSFORMER CONNECTIONS

CAUTION: Complementary inputs on TX and $\overline{TX}$ for more than 10 seconds may cause permanent damage at high temperatures due to high power dissipation by output drivers.

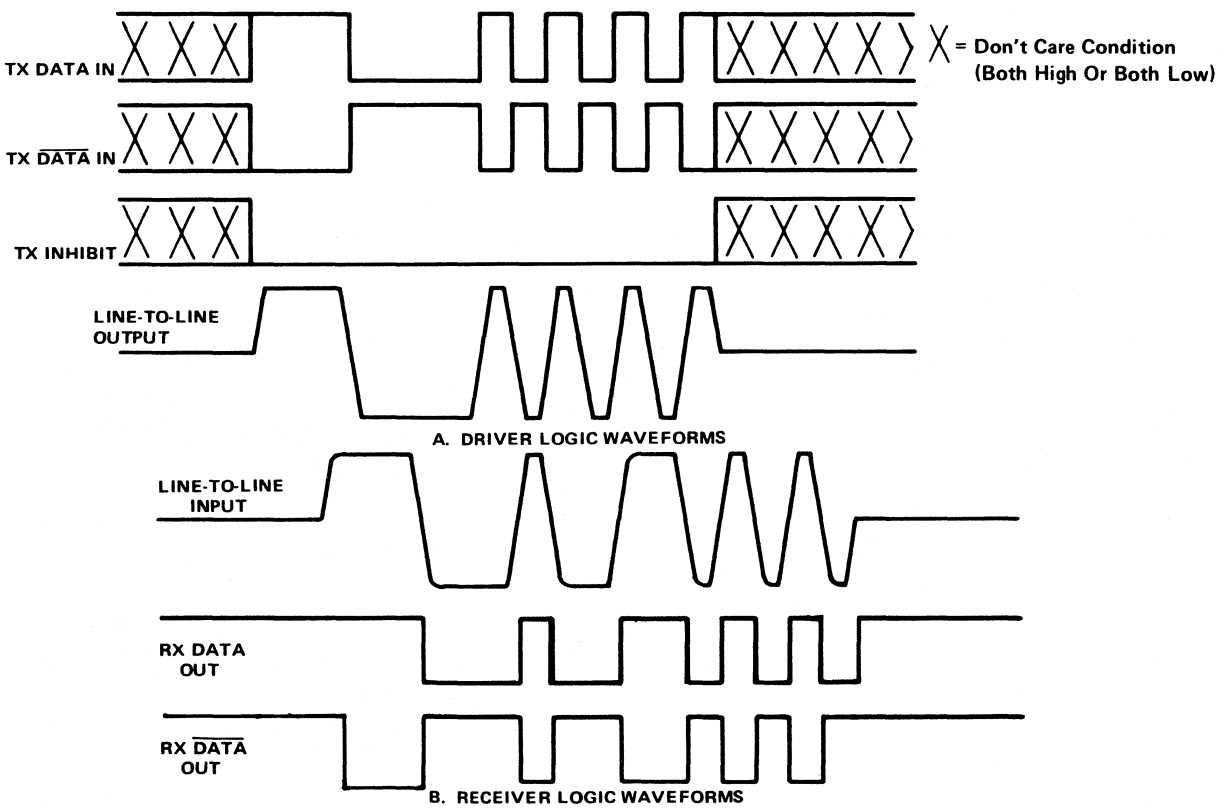
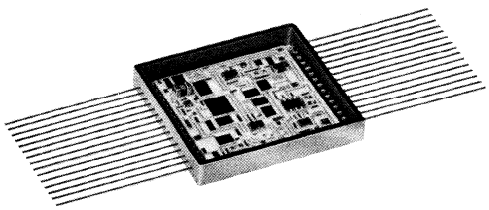


FIGURE 3. LOGIC WAVEFORMS

NOTE: 1) RX DATA and $\overline{RX\ DATA}$ lines are high when BUS-8554 is not receiving.
2) When BUS-8554 is used with Harris HD-15530, CMOS Manchester Encoder-Decoder, external inverters must be used on receiver DATA and $\overline{DATA}$ lines.

DDC
ILC DATA DEVICE CORPORATION

DATA BUS RECEIVER



DESCRIPTION AND APPLICATIONS

A hybrid data bus receiver, the BUS-8555 has been designed to convert bipolar, biphase Manchester II data to TTL levels, in accordance with McDonnell Douglas Corporation's A-3818, A-5232, A-4905, A-5690 and MIL-STD 1553 A/B specifications. This unit features the flexibility of internal and external threshold configurations†, which provide signal detection between 750 mV, peak to peak (nominal), preset internally; and 0.0 V to 2.0 V, peak to peak, adjusted externally (Figure 1). The BUS-8555's advanced design permits operation between 10 kHz and 1 MHz, while maintaining full accuracy with ±12 V to ±15 V power supply inputs. The BUS-8555 dissipates less power (550 mW) than competitive receivers.

Figure 2 illustrates the positive and negative excursions of a typical input waveform from the data bus.

† Internal threshold level is preset to 750 mV, peak to peak, when pins 18 and 28 are grounded.

FEATURES

- *MEET REQUIREMENTS OF McDONNELL DOUGLAS CORPORATION A-3818, A-5232, A-4905, A-5690 AND MIL-STD-1553 A/B*
- *550 mW POWER CONSUMPTION*
- *TTL COMPATIBLE OUTPUT*
- *MEETS MIL-STD-883*

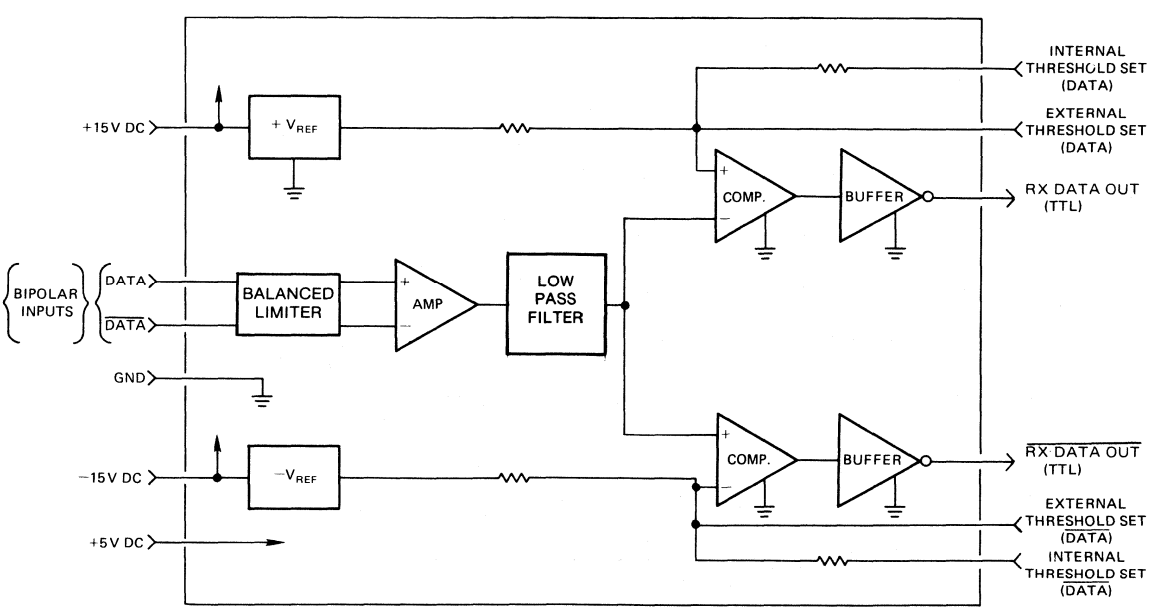


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

PARAMETER	VALUE
ANALOG INPUTS	
Bipolar (Differential) DATA and $\overline{\text{DATA}}$	40, p-p (max)
Input Impedance (Differential)	4 K (min)
Common Mode Rejection Ratio	40 (min)
Threshold Levels	
Internal (preset)	750, p-p (nom, with pins 18 & 28 grounded)
External Threshold Adjustment	0.0 to 2.0 (adjustable linearly with 0.0 to 10.0 k resistor respectively to ground.)
OUTPUTS	
DATA and $\overline{\text{DATA}}$ Output	TTL level Manchester II (biphase) serial data
POWER SUPPLY CHARACTERISTICS	
Operating Voltage Range	+4.5 V to 5.5 V, 20 mA @ +5 V −10 V to −18 V, 15 mA @ −15 V +10 V to +18 V, 15 mA @ +15 V
THERMAL CHARACTERISTICS	
Temperature Range Operating	−55 to +125 (Case)
Storage Temperature Range	−55 to +135
PHYSICAL CHARACTERISTICS	
Size	.895 X .950 X 0.15 max (22.7 X 24.1 X 3.8 mm max)
Weight	0.3 (8.5g)

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	+15 VDC	16	EXT THRESH (DATA)
2	NC	17	NC
3	NC	18	INT THRESH SET (DATA)
4	NC	19	NC
5	DATA INPUT	20	DATA OUTPUT
6	NC	21	NC
7	$\overline{\text{DATA}}$ INPUT	22	SEE NOTE
8	NC	23	NC
9	GND	24	GND
10	NC	25	NC
11	CASE GND	26	$\overline{\text{DATA}}$ OUTPUT
12	NC	27	NC
13	−15 VDC	28	INT THRESH SET ($\overline{\text{DATA}}$)
14	NC	29	NC
15	+5 VDC	30	EXT THRESH ($\overline{\text{DATA}}$)

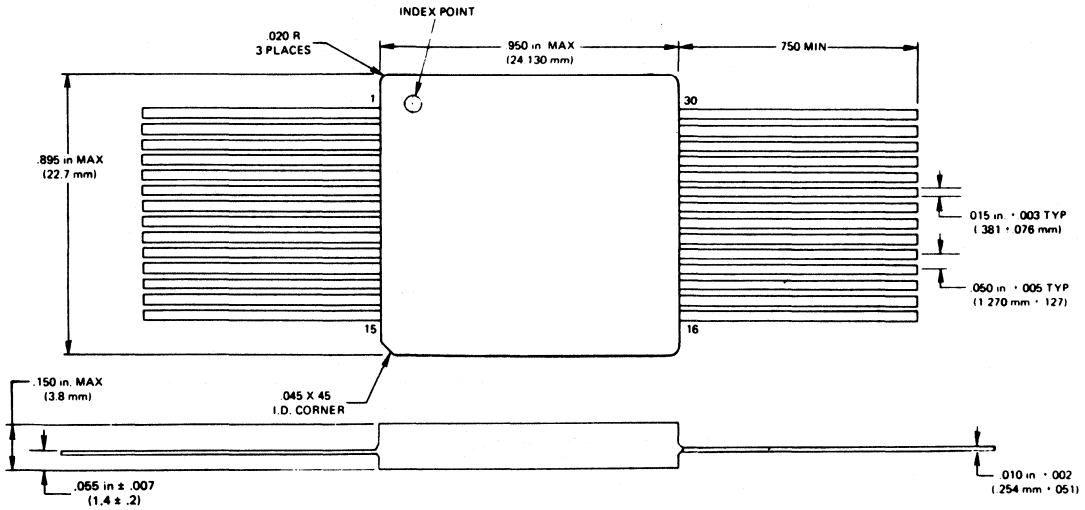
NOTE: Zero crossing output is available on special order; contact factory for details.

ORDERING INFORMATION

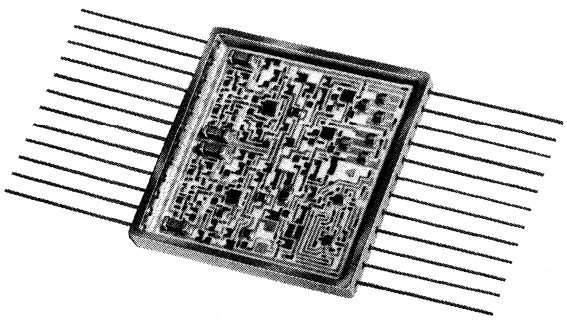
ORDER:

BUS-8555-883B

MECHANICAL OUTLINE



DATA BUS TRANSMITTER



FEATURES

- *LINEAR PHASE EQUIRIPPLE FILTER DESIGN*
- *MEETS REQUIREMENTS OF McDONNELL DOUGLAS A-3818, A-5232, A-4905 AND A-5690*
- *MEETS MIL-STD-883*

DESCRIPTION AND APPLICATIONS

The BUS-8556 transmitter meets the transmission requirements of the Command/Response Multiplex Data Bus set forth in McDonnell Douglas Specifications A-3818, A-4905, A-5232 and A-5690. It is completely compatible with receiver BUS-8555. The BUS-8556 incorporates a linear phase equiripple filter design (see figure 1).

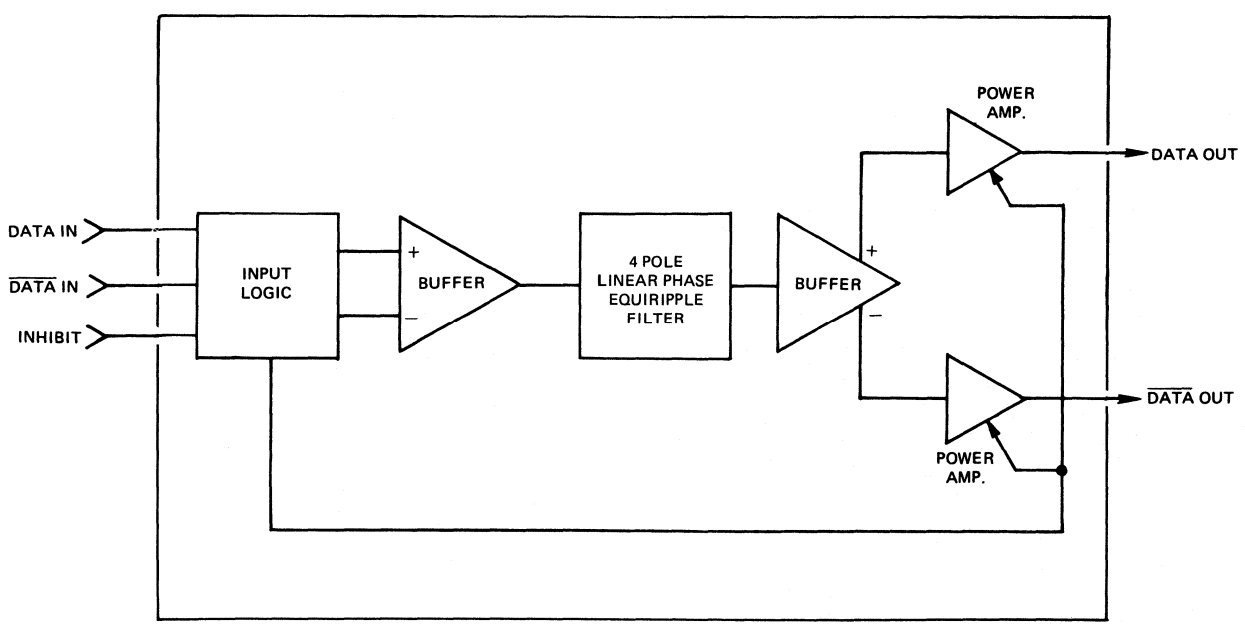


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

PARAMETER	UNITS	VALUES
INPUT LEVEL		
DATA and $\overline{\text{DATA}}$		TTL (Driving logic must sink 0.7mA max)
Inhibit		TTL to inhibit transmitter (Driving logic must sink 0.36 mA max)
OUTPUT CHARACTERISTICS		
DATA and DATA (p-p differential	V	32, ±4
Output Impedance	Ω	<10 max when transmitting
Harmonic Content		Filtered to eliminate harmonics above 1MHz (see figure 3)
Differential Group Delay	ns	± 35
Output Noise	mV	10 p-p
POWER REQUIREMENTS		
Range/Regulation	V	+5±5% | ±12 to ±15
. Current (see Figure 4)	mA	24 | 150 max† 40 max††
Power Dissipation	watts	2.9 (100% duty cycle) @±12V DC
		† Transmitting
		†† Standby
THERMAL CHARACTERISTICS		
Operating	°C	-55 to+125
Storage	°C	-55 to+150
PHYSICAL CHARACTERISTICS		
Size	in	1.25 x 1.25 x 0.20 (32 x 32 x 5.1mm)
Weight	oz	0.5 (14g)

TRANSMITTER WAVEFORM

The output waveform is derived from the referenced linear phase "low pass" filter which attenuates frequency components above 1MHz. Unlike the trapezoidal waveform required in the MIL-STD-1553A/B specification, a sinusoidal waveform is required by all four McDonnell Douglas specifications. Figure 2 is an illustration of an actual output waveform from the BUS-8556. The crisp symmetrical biphase shape is directly attributed to our filter design.

TECHNICAL INFORMATION

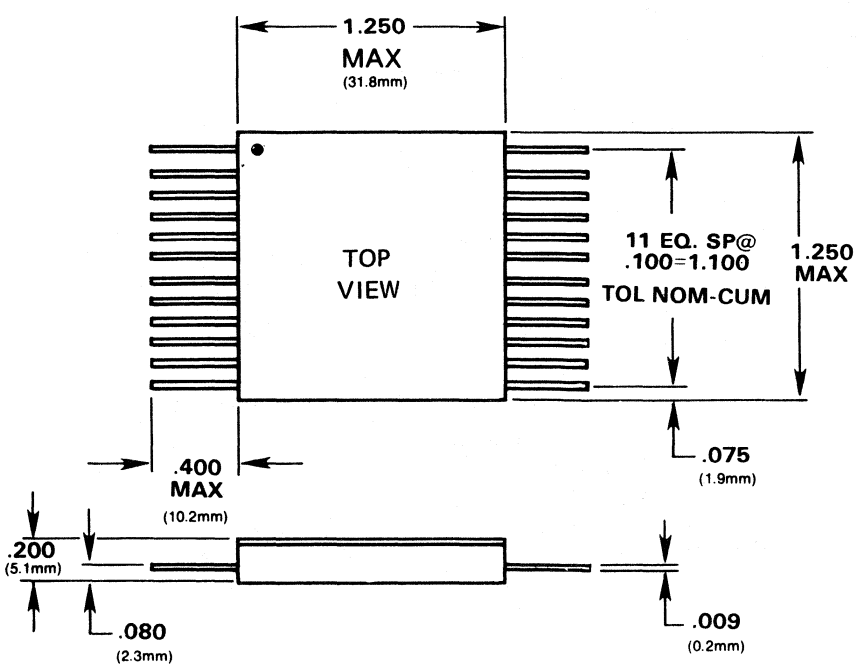
The BUS-8556 processes TTL biphase data from a Manchester II encoder, e.g. BUS-8937 hybrid*. When both DATA and $\overline{\text{DATA}}$ inputs are in the same logic state the Transmitter is inhibited (logic "1" disable the power amplifier outputs) and precludes any transmission. Waveform shaping functions are illustrated in Figure 3 as a result of differential time delay and gain response. The final stage buffer shown in Figure 1, provides a signal splitting function, which is equal to data phase shift from zero to 180 degrees (DATA and $\overline{\text{DATA}}$ respectively). The power amplifier boosts the signal to 30V, p-p nominal and provides a balanced low impedance output, without external gain circuitry.

* Contact DDC for BUS-8937 Data Sheet

ORDERING INFORMATION

ORDER:
BUS-8556-883

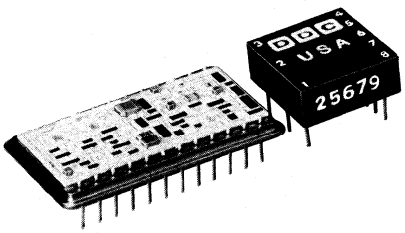
MECHANICAL OUTLINE



PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	+12V to +15V	13	
2		14	
3	$\overline{\text{DATA}}$ IN	15	
4	GND	16	$\overline{\text{DATA}}$ OUT
5	INHIBIT	17	
6	+5V	18	
7	DATA IN	19	
8		20	
9	CASE	21	DATA OUT
10	GND	22	
11		23	
12	-12V to -15V	24	

DDC
ILC DATA DEVICE CORPORATION



VARIABLE OUTPUT MIL-STD-1553 TRANSCEIVER

DESCRIPTION AND APPLICATIONS

Designed specifically for use in automatic test equipment when a variable transmitter output level is required, the DDC Model BUS-8559 Transceiver is a complete transmitter and receiver conforming to MIL standards 1553A and 1553B. The receiver section accepts phase-modulated bipolar data at the input and produces a bi-phase TTL signal at the output (Figure 1). The outputs, DATA and $\overline{\text{DATA}}$, represent positive and negative excursions of the input beyond an internally fixed threshold. These positive and negative thresholds are internally set at the factory for a nominal 1V p-p signal, measured at point "A", Figure 2. An external strobe input is provided to allow the removal of the receiver from the line. A logic "0" applied to "STROBE" will disable the receiver output.

The BUS-8559 transmitter section accepts bi-phase TTL data at the input and produces a 0 to 27 volt nominal p-p differential signal across the 145Ω load, when measured at point "B", Figure 2. When coupled to the data bus with the specified transformer*, isolated (on the data side) with two 55.0Ω fault isolation resistors, and loaded by two 70Ω terminations (plus additional receivers), the data bus signal produced is 0 to 7.5 volts nominal p-p measured at point "A" (Figure 2).

When both DATA and $\overline{\text{DATA}}$ inputs are held low or high, the transmitter presents a high impedance to the line. An external inhibit input is provided to allow the removal of the transmitter output from the line (Figure 3). A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the transmitter.

The transceiver is available in a 24 pin hybrid package measuring 1.4 x 0.8 x 0.2 inch, and can be used in any MIL-STD-1553 application which requires the use of a transceiver.

*Transformer P/N BUS-25679. See Mechanicals.

FEATURES

- *VARIABLE TRANSMITTER OUTPUT*
- *TRANSMITTER/RECEIVER IN A SINGLE 24 PIN DDIP HYBRID*
- *VERY LOW POWER DISSIPATION*
- *MEETS MIL-STD-1553A AND 1553B*
- *IMPROVED FILTERING ON RECEIVER TO ENHANCE BIT ERROR RATE OF SYSTEM*
- *±15V OR +15 AND −12V OPERATION*

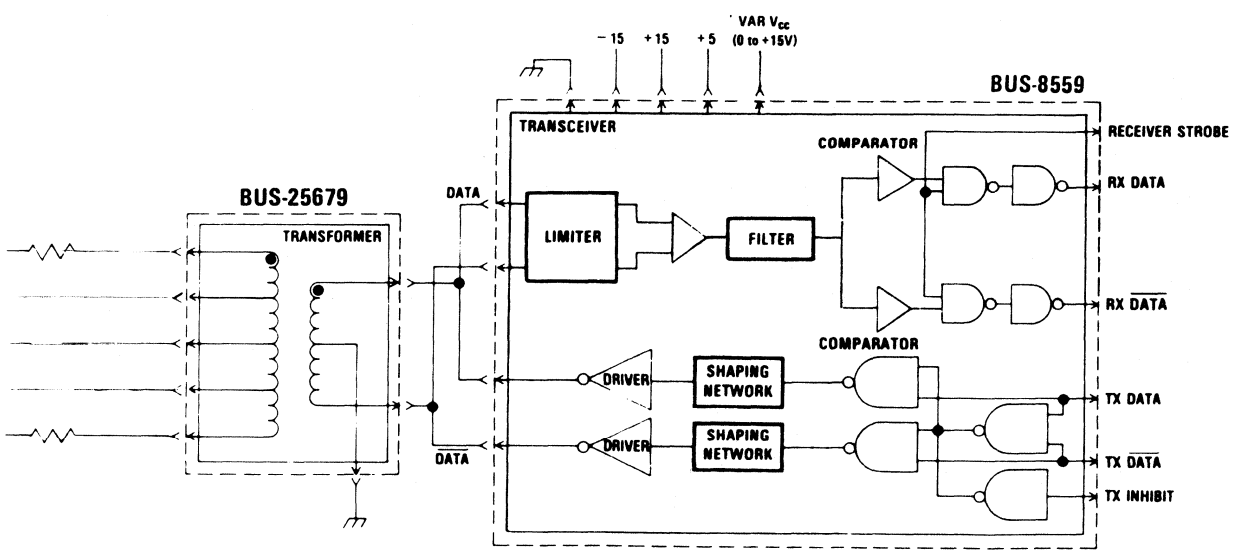


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS-TRANSFORMER AND BUS-8559 HYBRID

PARAMETER	VALUE
RECEIVER	
Input Level	40V p-p differential max
Input Impedance	4 KΩ differential min
Threshold Level	1V p-p nominal, internally set (direct coupled mode)
Output Level	TTL, 10 LS Loads
Outputs:	
V_{OL}	0.6V max
V_{OH}	2.5V min
I_{OL}	4mA max
I_{OH}	−400 μA max
TRANSMITTER	
Input Level	TTL, 2 LS Loads
Inputs:	
V_{ih}	2V min
V_{il}	0.8V max
I_{ih}	80 μA max
I_{il}	−3.2mA max
Output Level	0 to 27V p-p nominal across 145Ω load 0 to 20V p-p nominal (measured at point C, Figure 2)
Rise/Fall Time	130 nsec typical
Output Noise	10mV p-p differential max
Variable Vcc	0 to +15V DC

GENERAL

Power Supply Requirements

P.S.	STDBY	25%	100%
V	mA	mA	mA
+5	25 max	22 max	21 max
+15	30 max	30 max	30 max
-15	30 max	30 max	30 max
V_{cc}	0	70	180

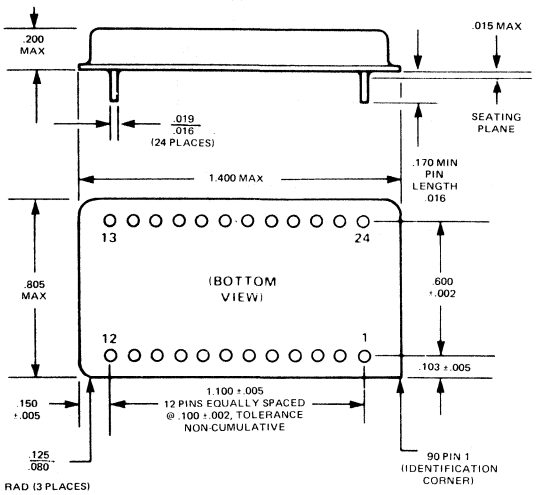
Operating Temperature Range	−55°C to +125°C (case temp.)
Storage Temperature Range	−55°C to +135°C
Size (24pin DDIP hybrid)	1.4 x 0.8 x 0.2 inch (36 x 20 x 5mm)
Weight	0.4 oz typ (11g)

NOTES: (1) Will operate with ±12V P.S.

BUS-8559 PIN CONNECTION TABLE

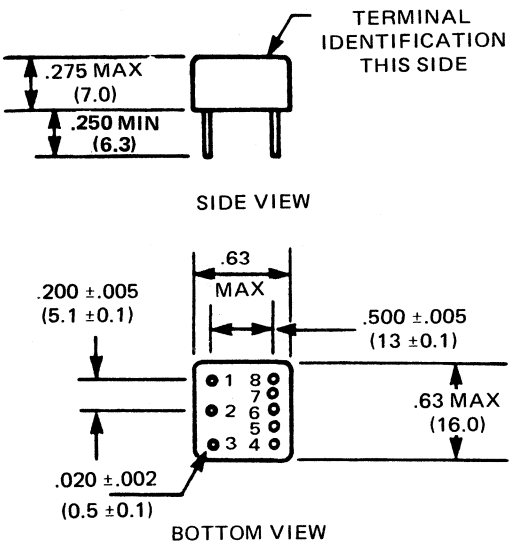
PIN	FUNCTION
1	TX Data Out
2	TX $\overline{\text{Data}}$ Out
3	GND
4	N.C.
5	N.C.
6	Variable Vcc
7	RX Data Out
8	Strobe
9	GND
10	RX $\overline{\text{Data}}$ Out
11	N.C.
12	N.C.
13	+15V DC
14	N.C.
15	RX Data In
16	RX $\overline{\text{Data}}$ In
17	N.C.
18	GND
19	−15VDC
20	+5VDC
21	TX Inhibit
22	TX Data In
23	TX $\overline{\text{Data}}$ In
24	N.C.

MECHANICAL OUTLINE
24 Pin Double DIP



NOTES:
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

MECHANICAL OUTLINE
TRANSFORMER (P/N BUS-25679)



NOTES:
1. All dimensions are in inches(millimeters)
2. Pin callouts on bottom view are for reference only

ORDERING INFORMATION

BUS – 8559 – 883B

MIL-STD-883 Processing:
883B = Conforms to MIL-STD-883 DDC procedures
Blank = Same, except pre burn in test and burn in are omitted

TRANSFORMER: BUS-25679

NOTE: The transceiver and transformer must be ordered as separate parts.

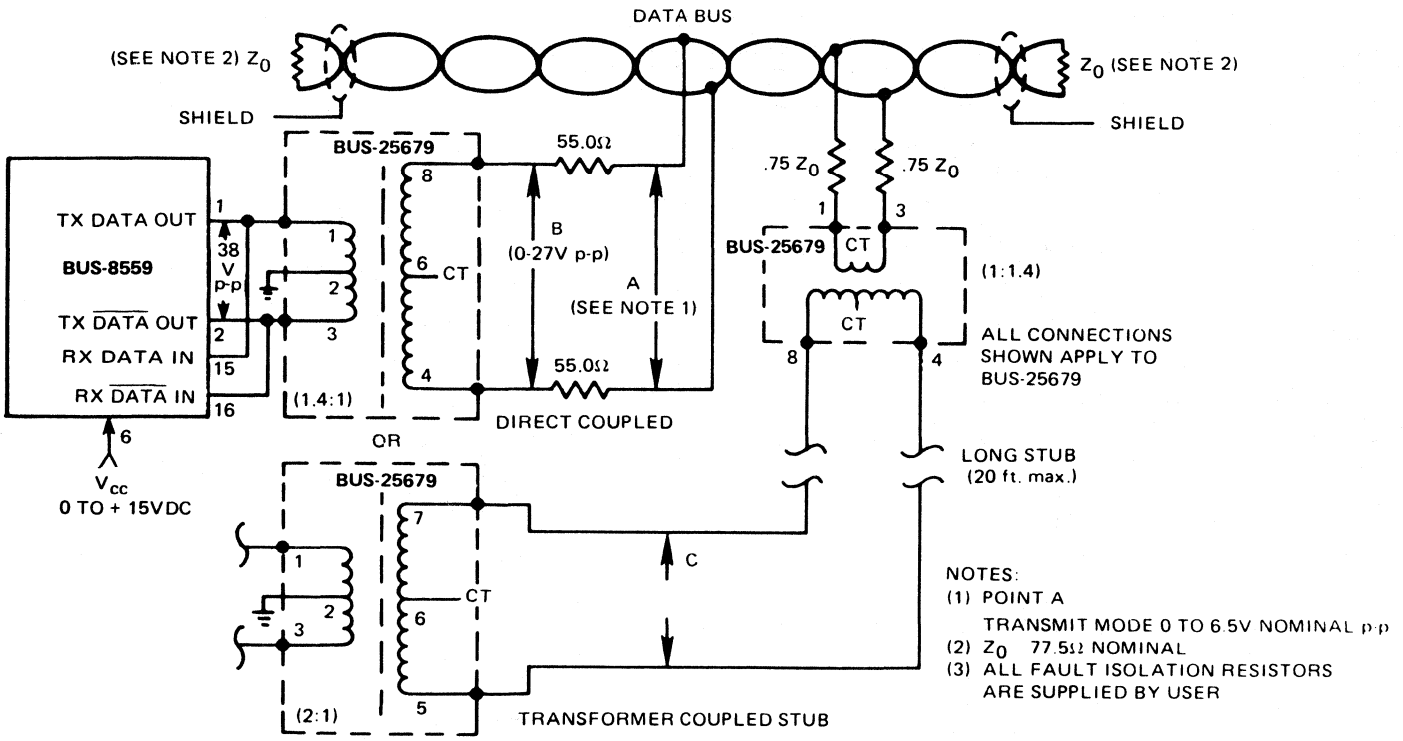
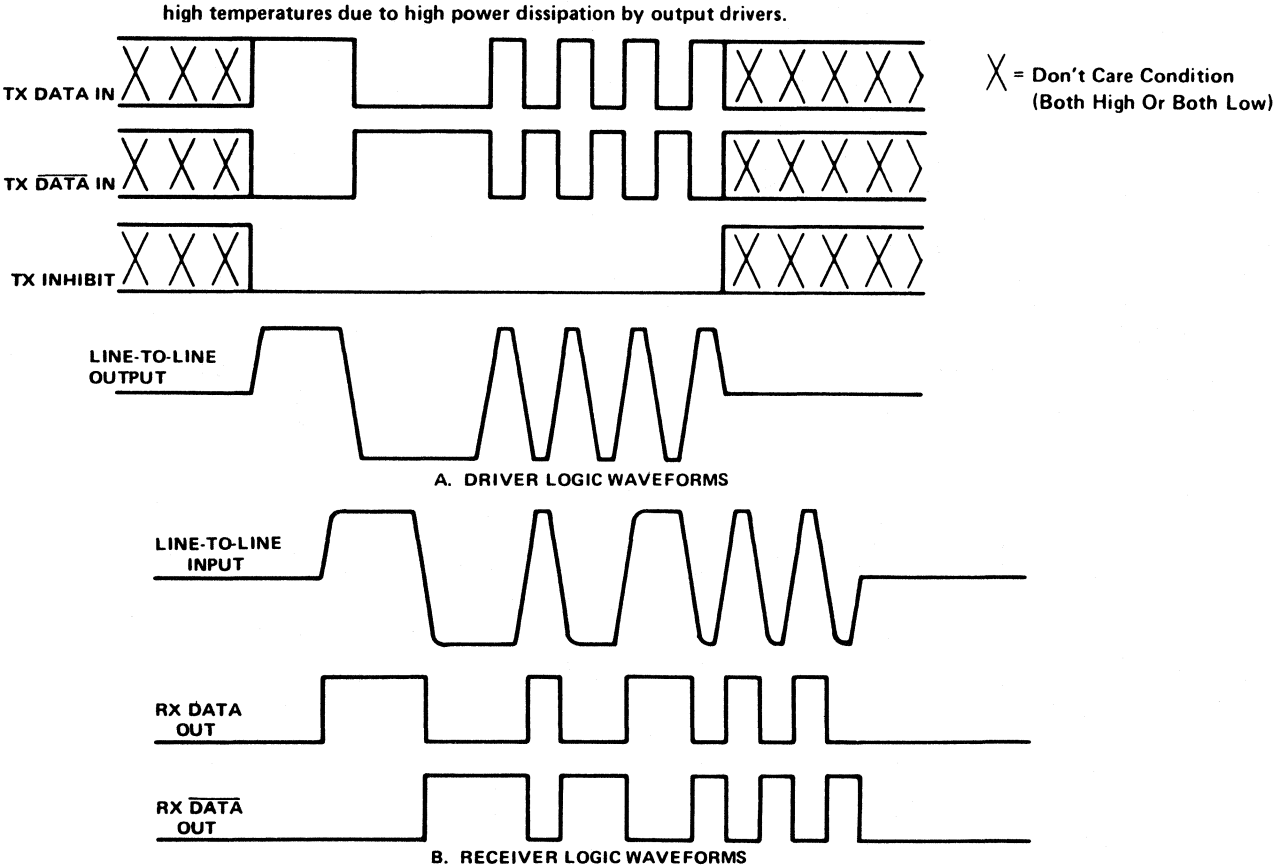


FIGURE 2. TYPICAL TRANSFORMER CONNECTIONS

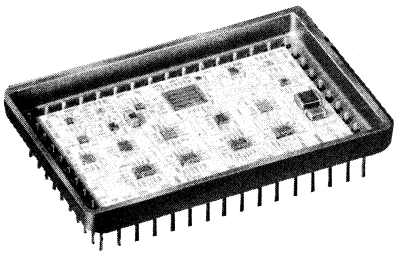
CAUTION: Complementary inputs on TX and $\overline{TX}$ for more than 10 seconds may cause permanent damage at high temperatures due to high power dissipation by output drivers.



NOTE 1) RX DATA and $\overline{RX\ DATA}$ lines are low when BUS-8553 is not receiving.
2) When BUS-8559 is used with Harris HD-15530, CMOS Manchester Encoder-Decoder no external logic is required.

FIGURE 3. LOGIC WAVEFORMS

MIL-STD-1553A/B COMMAND/RESPONSE MANCHESTER II CONVERTER



FEATURES

- *3-STATE, 16 BIT PARALLEL INTERFACE*
- *TTL COMPATIBLE*
- *ADDRESS RECOGNITION*
- *WRAP-AROUND SELF TEST CAPABILITY*
- *MEETS MIL-STD-883*

DESCRIPTION AND APPLICATION

The BUS-8937 is a hybrid device, designed to provide the interface between a parallel 16 bit data bus and a MIL-STD-1553B transceiver. The BUS-8937 is a double buffered serial to parallel and parallel to serial converter providing all data interfacing between a parallel bus and a MIL-STD-1553 transceiver, including Manchester decoder/encoder (Figure 1.). Another feature of the hybrid is address recognition circuitry, which is applicable to all MIL-STD-1553 applications.

SPECIFICATIONS

PARAMETER	UNIT	VALUE
EXTERNAL CLOCK INPUT Oscillator type (12 MHz)	TTL	As per MIL-STD-1553 A/B long and short term stability requirements.
POWER SUPPLY CHARACTERISTICS Voltage input Current	 V mA	 +5, ±10% 200 max, 180 typ
THERMAL CHARACTERISTICS Operating Temperature Storage Temperature	 °C °C	 –55 to +125 (case temperature) –55 to +150
PHYSICAL CHARACTERISTICS Weight Size	 oz in.	 0.7 (20g) 1.7 X 1.1 X 0.2 (43 X 28 X 5.1 mm)

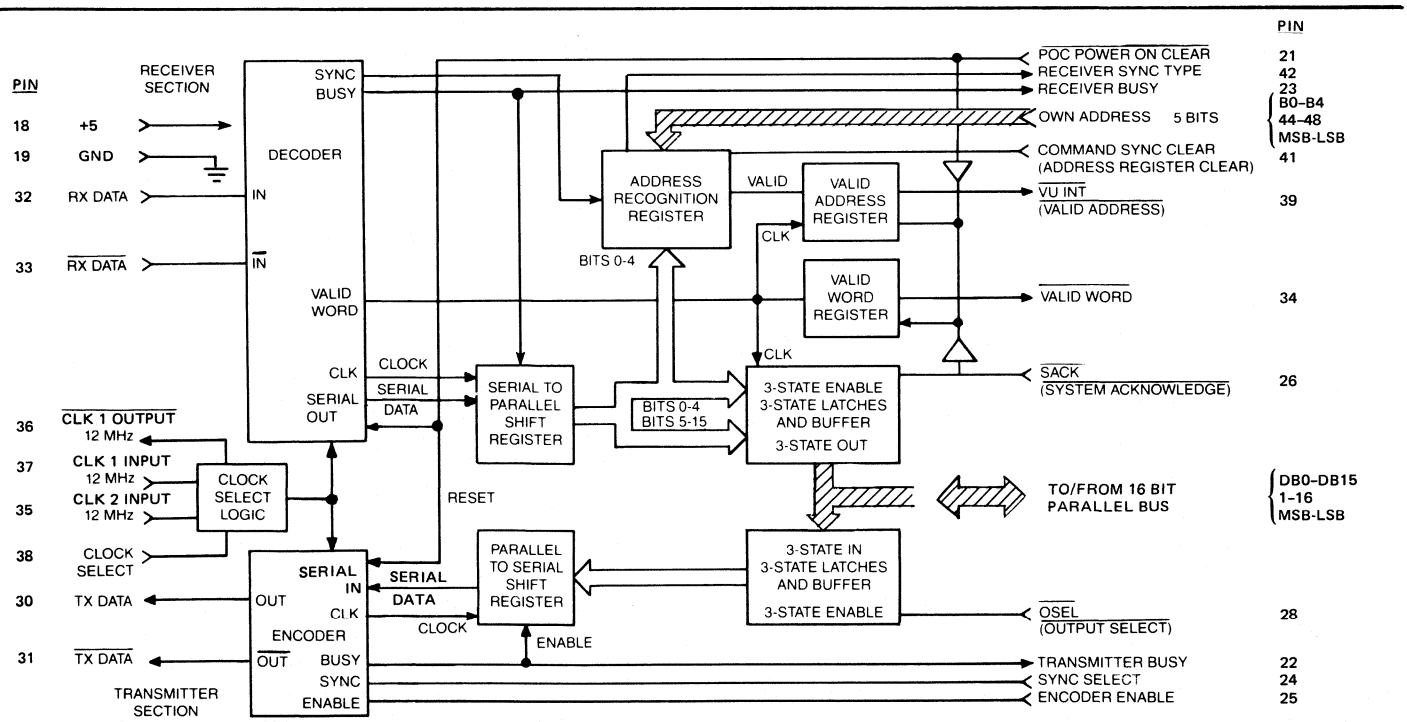


FIGURE 1. BUS-8937 BLOCK DIAGRAM

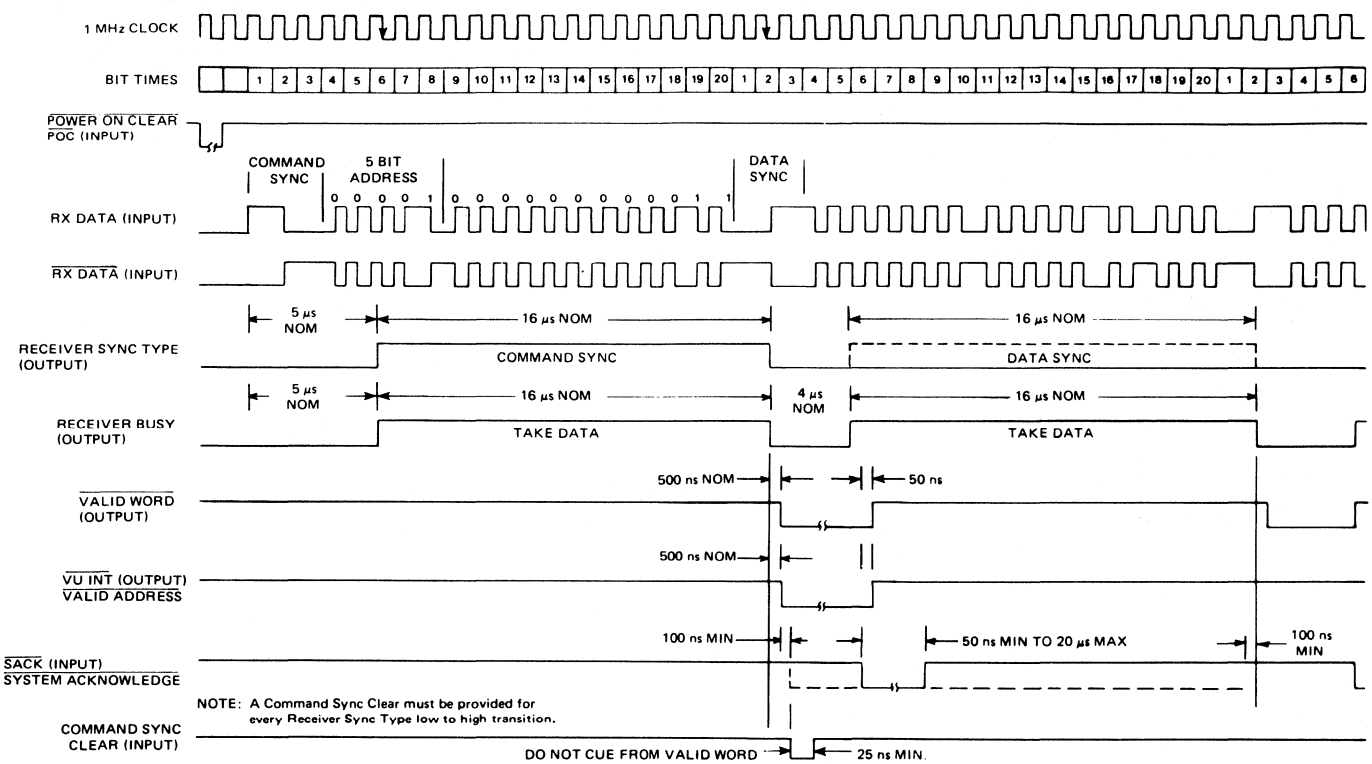


FIGURE 2. RECEIVER SECTION TIMING FOR DECODER OPERATION

BUS-8937 OPERATION

Power On Clear (POC): A logic "0" input applied at turn-on initializes all of the internal logic. This signal clears the Harris 15530 internal counters and initializes the encoder and decoder functions. This can also be used to abort a transmission.

DECODER OPERATION

As seen in Figure 1, BUS-8937 block diagram, the BUS-8937 interfaces directly with the BUS-8553 transceiver by means of four lines, namely Tx Data, Tx Data, Rx Data and Rx Data. In the decode mode of operation the BUS-8937 normally needs logic lows (off mode) on Rx Data and Rx Data. Whenever the MIL-STD-1553 data bus is active the BUS-8553 transceiver will output signals, that are similar to those illustrated in Figure 2 (Rx Data and Rx Data), to the BUS-8937. Approximately 5 microseconds after the BUS-8937 has detected the first transition change in the Rx Data input line, the Receiver Busy output line will activate from a low to high state and remain high for 16 microseconds. During this period, the Harris Encoder/Decoder is shifting serial data out, and the information is being clocked into an internal 16 bit serial to parallel shift register. The Receiver Busy line will go low after 16 microseconds, and will remain low for 4 microseconds if another 20 bit word immediately follows the first word. The second word will cause Receiver Busy to go high for another 16 microsecond time interval. This sequence continues until no additional information is to be processed.

At approximately the same time as the first Receiver Busy low to high transition, the Receiver Sync Type line will go high if a command or status sync field is detected by the Harris decoder. It too will remain high for 16 microseconds If a data sync field is detected by the decoder, the Receiver Sync Type line will remain in the low state. During the receiver busy time the decoder shifts serial data out to the serial to parallel shift register, regardless of whether the data is valid or not. However, the stored data is not shifted into the 3-State output buffer unless a valid word indication occurs. This signal is designated Valid Word. Valid Word performs three functions within the BUS-8937: Strobes the 16 bit parallel word into the 3-state output buffer, strobes the address recognition function, and indicates to the subsystem user that a valid 16 bit word is now ready to be processed. A high to low transition on the Valid Word line will indicate the recipt of a valid word.

The first five bits of a 16 bit command word represent the terminal address. The bits are decoded, shifted through the serial to parallel shift register and compared to the five lines in the Address Recoginition Register (Own Address, B0 (MSB) thru B4.) If a command word is received, and the Own Address lines and decoder remote terminal address bits correspond; and Valid Word occurs, then a Valid Address signal (VU INT) will occur, going from a logic one to logic zero. This signal transitions at the same time as

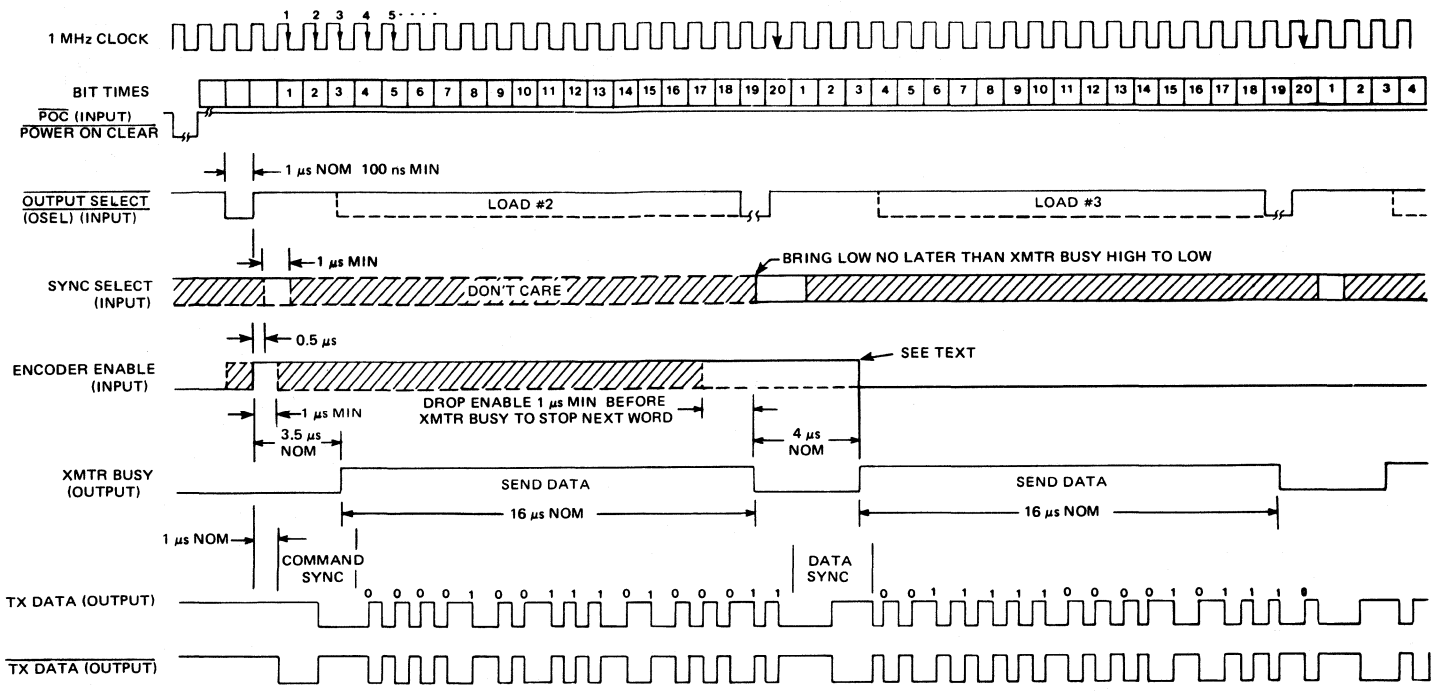


FIGURE 3. TRANSMITTER SECTION TIMING FOR ENCODER OPERATION

Valid Word. Upon detecting a Valid Word output, the user subsystem must respond with a signal called System Acknowledge (SACK). A high low input to the BUS-8937 will set both Valid Word and VU INT (if occurred) to their original high states. These two circuits are then ready to analyze the next received 20 bit word. At the same time SACK will enable the output 3-State Buffer for data readout on the 16 parallel data lines. The user subsystem has up to 20 microseconds to process the data before the next 20 bit word is ready to be latched in the output buffer. A return to the high state on SACK will cause the 3-State Output Buffer to return to the high impedance state, completing the conversion of one 20 bit word. The command Sync Clear input signal is required to initialize BUS-8937 internal logic, set by detection of command or status sync. It also resets Valid Word logic. This input signal must be applied each time a Receiver Sync type transitions, low to high, occurs but must not occur until the Valid Word transitions high to low. Under certain circumstances Valid Address transition may not occur after a valid sync field is recognized.

ENCODER OPERATION

In the encode mode of operation (Figure 3.) the BUS-8937 normally provides logic highs (off mode) on Tx Data and Tx Data. These two signal lines provide output data in complementary serial phase modulated format to the BUS-8553 transceiver during a transmission. To effect a transmission from the BUS-8937, the sequence of events is to first load 16 bit parallel data into the 3-State input buffer. This is achieved by the presentation of an input pulse of logic zero on the Output Select (OSEL) line. Data to the BUS-8937 must be stable when the OSEL occurs. When the XMTR Busy signal goes from low to high the OSEL may be activated to load the next 16 bit word in preparation for transmission.

Next, the user subsystem must bring the Encoder Enable line high to initiate a transmission. Encoder Enable can be conveniently triggered from the leading or trailing edge of OSEL but must remain high for 1 µs.

If the Encoder Enable line is allowed to remain high, successive transmissions will result. The Transmitter Busy line will go high for 16 microseconds every time a 20 bit word is processed through the Harris Encoder. Transmitter Busy indicates to the user subsystem that control logic is shifting data from the parallel to serial data buffer to the bi-phase encoder during a transmit cycle. To terminate a transmission, the Encoder Enable line must be brought low on or before the high to low transition of the current Transmitter Busy signal.

The remaining signal that is required to make the BUS-8937 encoder operate properly is the Sync Select input signal. Sync Select is an input from the user subsystem for the purpose of setting the appropriate sync field polarity to correspond with the word to be transmitted. A high on this line will create a command or status sync field, and a low will result in a data sync field. Initially it should be set to a logic "1" before the Encoder Enable line is set high, and remain high no later than the high to low transition of the Transmitter Busy signal.

PIN FUNCTION AND FAN/OUT TABLE

PIN	COMMENT	PARAMETER	VALUE(S) MAX.	UNITS	LS TTL LOADING	IN/OUT-PUT	PIN	COMMENT	PARAMETER	VALUE(S) MAX.	UNITS	LS TTL LOADING	IN/OUT-PUT
1 THRU	DBO (MSB) THRU	IOH	−2.58	MA	29 DRIVE		32	RX DATA	IIH	+1	μA	1	INPUT
16	DB15 (LSB) PARALLEL	IOL	11.60	MA		BOTH	33	RX DATA	IIL	−1	μA	1	INPUT
	DATA I/O	IIH	40	μA	1LOAD		34	VALID WORD	IOH	−400	μA	10	OUTPUT
		IIL	−420	μA					IOL	4	MA		
17	N.C.						35	CLOCK 2 IN	IIH	20	μA	1	INPUT
18	+5VDC								IIL	−.4	MA		
19	GROUND						36	$\overline{\text{CLOCK 1 OUT}}$	IOH	−380	μA	9	OUTPUT
20	N.C.								IOL	3.6	MA		
21	$\overline{\text{POC}}$	IIH	20	μA	1	INPUT	37	CLOCK 1 IN	IIH	20	μA	1	INPUT
		IIL	−.4	MA					IIL	−.4	MA		
22	XMTR BUSY	IOH	−260	μA	6	OUTPUT	38	CLOCK SELECT (1)	IIH	40	μA	2	INPUT
		IOL	1.2	MA					IIL	−.8	MA		
23	RCV. BUSH	IOH	−380	μA	9	OUTPUT	39	$\overline{\text{VU INT}}$	IOH	−400	μA	10	OUTPUT
		IOL	3.6	MA					IOL	8	MA		
24	SYNC SEL	IIH	+1	μA	1	INPUT	40	N.C.					
		IIL	−1	μA			41	COMMAND SYNC. CLEAR	IIH	40	μA	1	INPUT
25	ENCODER ENABLE	IIH	+1	μA	1	INPUT			IIL	−.8	MA		
		IIL	−1	μA			42	RCVR. SYNC TYPE	IOH	−360	μA	9	OUTPUT
26	$\overline{\text{SACK}}$	IIH	60	μA	3	INPUT			IOL	3.2	MA		
		IIL	−1.2	MA			43	N.C.					
27	N.C.						44	BO ADDRESS (MSB)	IIH	40	μA	2	INPUT
28	OSEL NOT	IIH	20	μA	1	INPUT			IIL	−.8	MA		
		IIL	−.4	MA			45-48	B1-B4 (LSB)	IIH	60	μA	3	INPUT
29	N.C.								IIL	−1.2	MA		
30	TX DATA	IOH	−3	MA	1	OUTPUT	POWER REQUIREMENT		200 MA MAX @ 5VDC (180 MA TYP)				
31	$\overline{\text{TX DATA}}$	IOL	1.8	MA	1	OUTPUT							

(1) Logic "1" enables clock 1.

$\overline{\text{POC}}$ CIRCUIT

The $\overline{\text{POC}}$ input is required to initialize all internal logic upon power-up. The suggested circuit is intended as a low cost and easily implemented $\overline{\text{POC}}$ pulse generator (Figure 4).

When the power supply plus five volts is applied to pin A of Figure 1, the 2 microfarad capacitor looks momentarily as a short circuit. The RC time constant set up by the 2 microfarad cap and the series 1.5 ohm resistor delays the input five volts to pin 21 of the BUS-8937. This approx. 3 microsecond exponential rise caused by the capacitor charging, is a sufficient logic low $\overline{\text{POC}}$ signal.

Other considerations for generating the $\overline{\text{POC}}$ logic, would be Master System Restate (MSR) logic or perhaps a timed TTL buffered interface.

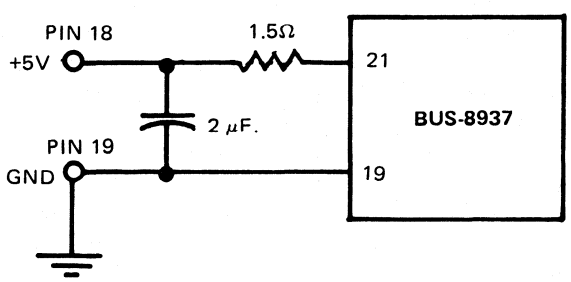


FIGURE 4. $\overline{\text{POC}}$ CIRCUIT

COMMAND SYNC CLEAR

The external command sync. clear circuit will initiate the 1 μsec pulse required to clear the receiver sync. type BUS-8937 internal logic. The receiver sync. type logic will then be ready to flag the next decoded word type.

The circuit incorporates two 74LS121 monostable multivibrators with Schmitt Trigger inputs. Receiver sync, type and receiver busy are connected directly to U1 inputs A1 and A2 to monitor a decoded command (or status) sync. When the BUS-8937 flags a command sync., U1 is triggered by the high to low transition. It will then generate an output high level pulse 2.8 μsec in width, which will trigger U2, on the trailing edge. The output from U2 is the command sync, clear low level 1 μsec pulse to be applied to the BUS-8937. This circuit resets after U1 and U2 have been timed out.

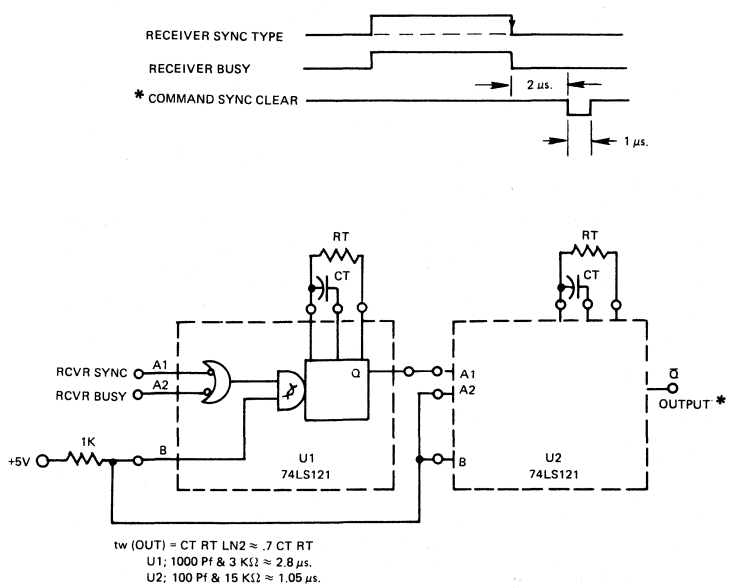


FIGURE 5. COMMAND SYNC CLEAR CIRCUIT

WRAP-AROUND SELF TEST

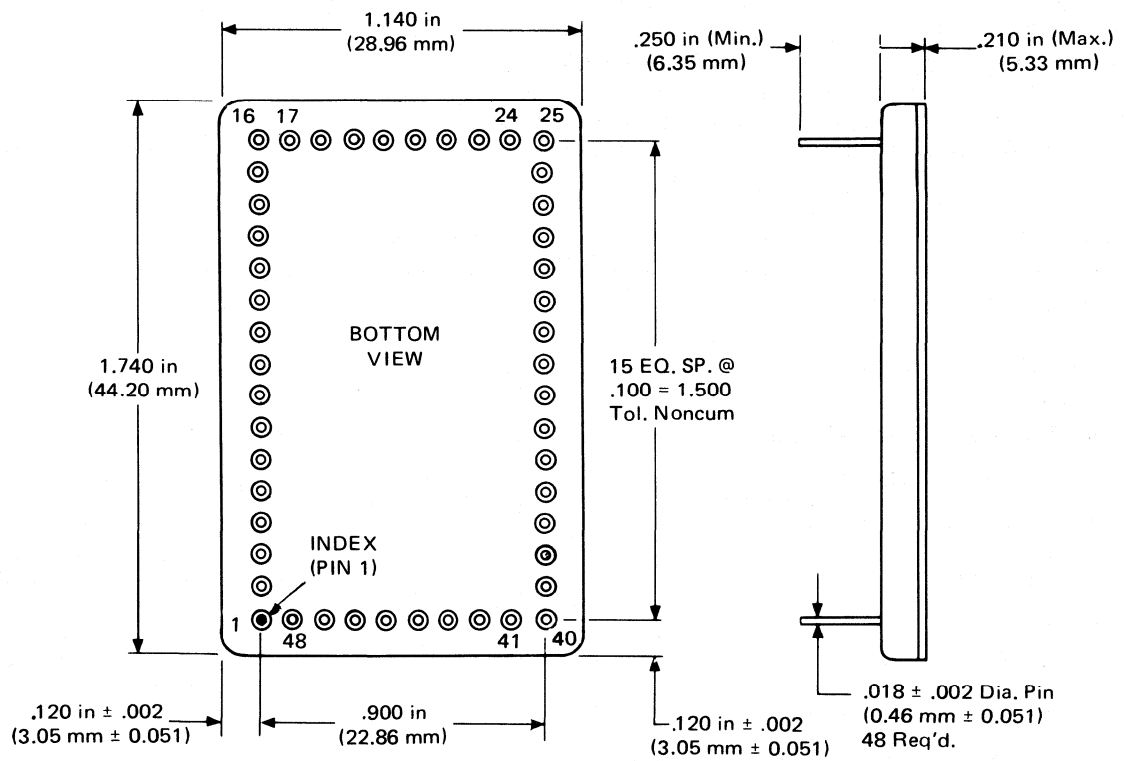
Self test capability can be achieved by multiplexing TX DATA and $\overline{\text{TX DATA}}$ through external multiplexers and routed into RX DATA and $\overline{\text{RX DATA}}$. TX inputs to the transceiver should be inhibited while wrap-around is in progress.

ORDERING INFORMATION

BUS - 8937 - 883B

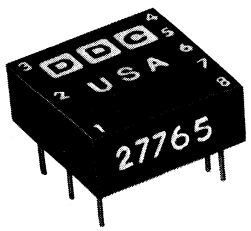
└ MIL-STD-883B Processing:
883B = MIL-STD-883
DDC procedures
Blank = Same except preburn in test and burn in are omitted.

MECHANICAL OUTLINE



ILC DATA DEVICE CORPORATION

MIL-STD-1553 DATA BUS ISOLATION TRANSFORMERS



DESCRIPTION AND APPLICATIONS

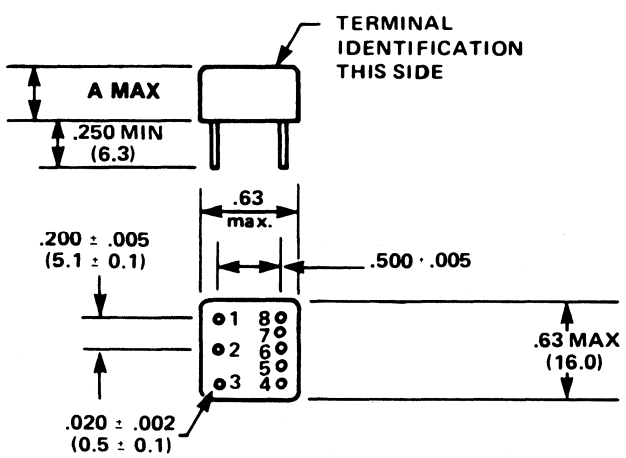
The military Data Bus Specification, MIL-STD-1553, has brought about the need for versatile pulse transformers that meet all the electrical requirements of Manchester II serial bi-phase data transmission. The BUS-25679, BUS-27765 and BUS-29854 provide all of the turns ratio configurations, component isolation and common mode rejection ratio characteristics necessary for MIL-STD-1553 A and B.

The step up and down ratios, available with these transformers, complement our entire product line and are compatible with competitive drivers, receivers and transceivers (contact the factory for details). The transformers are low profile, modular units that are multi-tapped to accommodate existing system configurations. They are encapsulated in accordance with MIL-T-21038. Their tin coated steel leads conveniently accommodate printed circuit board mounting. They accurately process sinusoidal or trapezoidal waveforms, in accordance with MIL-STD-1553 A and B and McDonnell Douglas specifications A-3818, A-5690, A-5232 and A-4905.

FEATURES

- *MANCHESTER II, BI-PHASE, 1MHz OPERATION*
- *FOR USE WITH MIL-STD-1553 A AND B AND MACAIR SPECIFICATIONS A-3818, A-5690, A-5232 AND A-4905*
- *8 PIN, LOW PROFILE PACKAGE*
- *OPERATING TEMPERATURE: -55° C to +125° C*

MECHANICAL OUTLINE (BUS-25679, BUS-27785 & BUS-29854)



DIMENSION TABLE		
BUS-25679	BUS-27765	BUS-29854
A = 0.275 in. (7mm)	A = 0.300 in. (7.6mm)	A = 0.275 in. (7mm)

Notes
1. Dimensions are maximums unless otherwise noted.
2. All dimensions are in inches (millimeters).
3. Pin callouts on bottom view are for reference only.

TURNS RATIO TABLE				
		TURNS RATIO		
PRIMARY	SECONDARY	BUS-25679	BUS-27765	BUS-29854
1, 3	4, 8	1.4 : 1	1 : 1	1 : 0.83
1, 3	5, 7	2 : 1	1 : .707 (1.4 : 1)	1 : 0.60

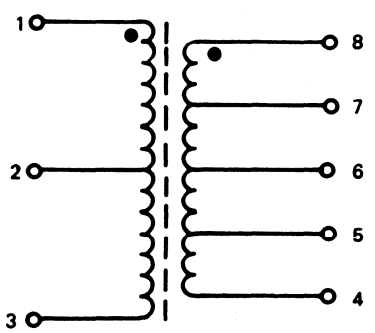


FIGURE 1. TURNS RATIO DIAGRAM

BUS TRANSFORMERS

SPECIFICATIONS				
PARAMETER	**UNITS**	**VALUE**		
		BUS-25679	**BUS-27765**	**BUS-29854**
FREQUENCY RESPONSE				
Operating Range	KHz	250 to 3000	10 to 3000	250 to 3000
Self Resonance	MHz	40 min	40 min	40 min
COMMON MODE REJECTION (CMR)	dB	50 min	40 min	50 min
ELECTRICAL REQUIREMENTS				
Terminals 1, 3 & 4, 8				
Winding Resistance (RDC)	Ω	1 max	3 max	1.9 max
Interwinding Capacitance	pF	70 max	30 max	70 max
Winding Inductance				
(LM)	mH	7.5 min	7.5 min	7.5 min
(LL)	uH	6.0 max	6.0 max	6.0 max
PEAK TO PEAK VOLTAGE				
Terminals 1, 3	Vpp	60 max	39.2 max	60 max
PEAK PULSE CURRENTS (AC)				
Terminals 1, 3 (primary)	mA	180 max	140 max	180 max
DROOP				
3 us Pulse Duration				
140Ω Load Across 1.42				(1.66 Ratio)
Ratio	%	10 max	10 max	10 max
DECAY TIME				
140Ω Load Across				(1.66 Ratio)
1.42 Ratio	ns	25 max	25 max	25 max
BACKSWING				
Across 140Ω Load				(1.66 Ratio)
(1.42 Ratio)		none	none	none
TURNS RATIOS				
Terminals				
1, 3 : 4, 8		1.4 : 1	1 : 1	1 : 0.83
1, 3 : 5, 7		2 : 1	1 : .707	1 : 0.60
2 : 6		CT	CT	CT
Winding Tolerance	± %	5	3	5
TEMPERATURE REQUIREMENTS				
Operating (ambient)	°C	-55 to +125	-55 to +125	-55 to +125
Storage	°C	-55 to +130	-55 to +130	-55 to +130
PHYSICAL CHARACTERISTICS				
Size	in	0.63 x 0.63 x 0.275 (16 x 16 x 7 mm)	0.63 x 0.63 x 0.300 (16 x 16 x7.6 mm)	0.63 x 0.63 x 0.275 (16 x 16 x 7 mm)
Weight	oz	0.1 (3g)	0.1 (3g)	0.1 (3g)

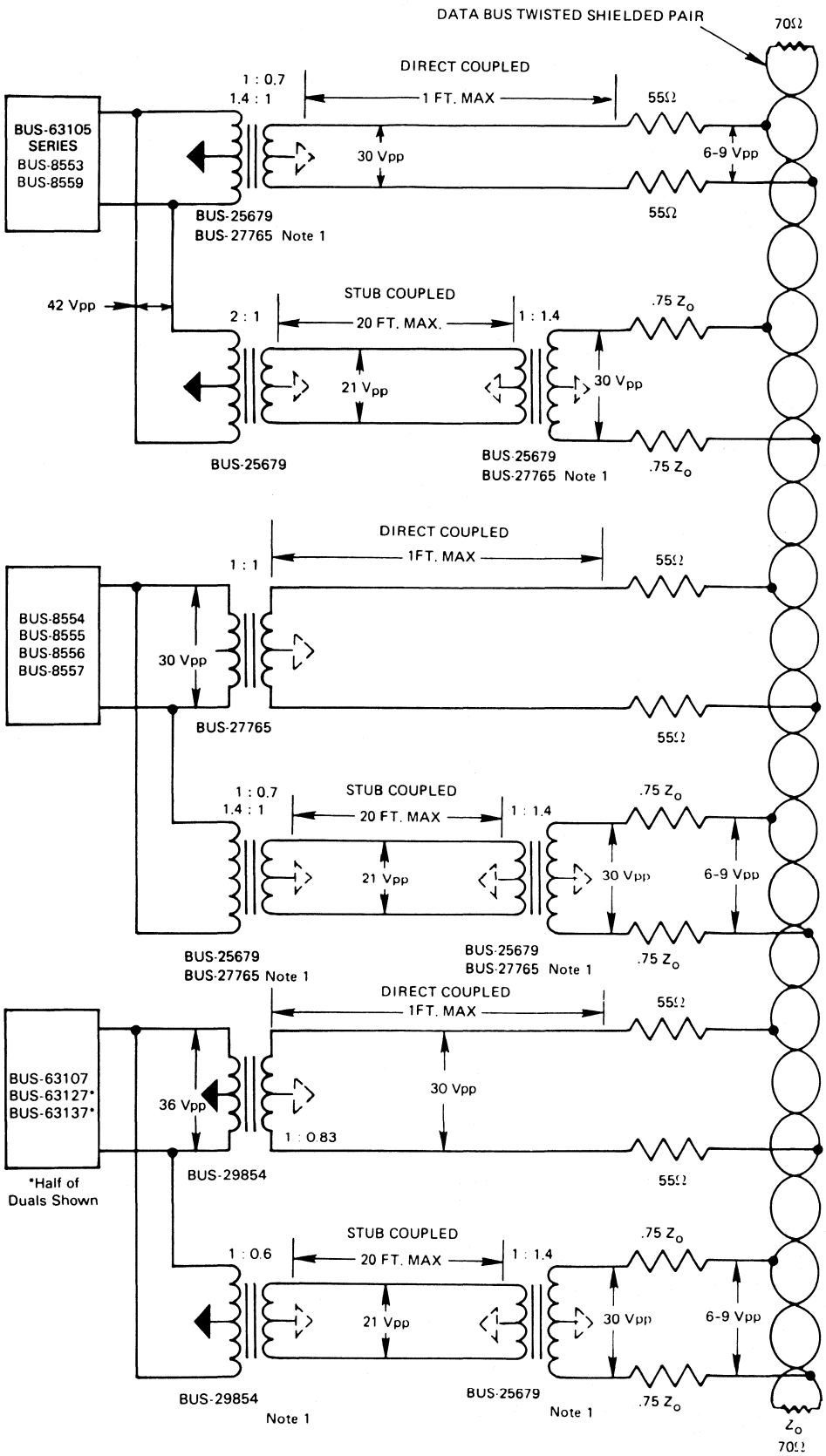
TECHNICAL INFORMATION

For the purpose of illustration, pins 1-3 represent the primary winding for each transformer (See Figure 1). In all applications the BUS-25679 may be used for long stub connections as illustrated in Figure 2. The secondary winding is connected to the Data Bus through two fault isolation resistors for direct, or to another transformer for long stub connections as shown. Please note that the transformers connected to the BUS-8553, BUS-8559 and BUS-63105 series transceivers require that their primary center tap winding be grounded.

ORDERING INFORMATION

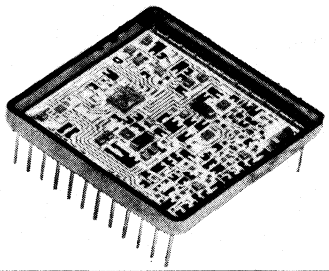
ORDER: BUS-25679, BUS-27765 or BUS-29854

NOTES:
1. Consult Figure 2 for correct unit for application
2. Consult factory for competitor cross reference information



NOTE 1. Refer to turns ratio table for pinouts.

FIGURE 2. CONNECTION DIAGRAM



UNIVERSAL DATA BUS TRANSCEIVER Meets Requirements of MIL-STD-1553 and McDonnell Douglas Specifications

DESCRIPTION

The BUS-63102 is a universal data bus transceiver, which meets the requirements of both MIL-STD-1553 A and B and McDonnell Douglas (MACAIR) specifications A-3818, A-4905, A-5232 and A-5690. The transmitter section (figure 1) incorporates a linear phase equiripple filter which results in a superior transmitted waveform.

The need for a small low power transceiver, compatible with sinusoidal or trapezoidal waveforms, brought about the development of this 1.25 inch square dual-in-line (DIP) hybrid. The unit features the flexibility of internal or external threshold configuration, which provides signal detection preset internally or 0V to 2.0V p-p, adjustable externally. The BUS-63102's advanced design permits operations between 10 kHz and 1 MHz, while maintaining full accuracy with ±12V to ±15V power. The hybrid is fully screened to meet MIL-STD-883B.

APPLICATIONS

The BUS-63102 transceiver is unique to contemporary applications, because its packaging and functional design permit the user to eliminate separate receivers and transmitters. With only one hybrid performing bi-directional communications, the system designer saves valuable circuit board space while taking advantage of the BUS-63102's waveform shaping characteristics. It is ideally suited to external stores which must interface with various aircraft having 1553 or MACAIR type buses.

FEATURES

- *MEETS MIL-STD-1553 A AND B (TRAPEZOIDAL WAVEFORMS)*
- *MEETS MCDONNELL DOUGLAS A-5690, A-3818, A-4905 AND A-5232 (SINUSOIDAL WAVEFORMS)*
- *LOW POWER DISSIPATION*
- *SINGLE PACKAGE TRANSCEIVER*
- *±12V OR ±15V POWER SUPPLIES*
- *LINEAR PHASE EQUIRIPPLE FILTER*

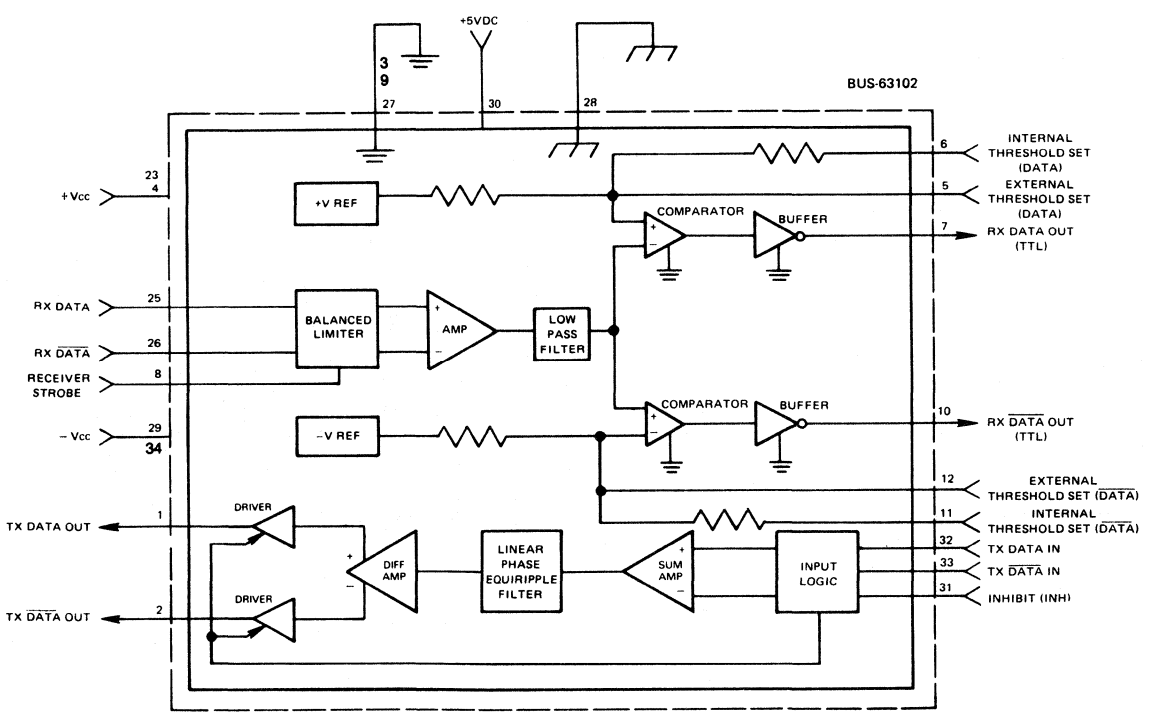


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS		
PARAMETER	**UNITS**	**VALUE**
RECEIVER		
Receiver Strobe	TTL	1 load
Analog Inputs		
Bipolar (Differential) DATA and $\overline{\text{DATA}}$	Vpp	40 (max)
Input Impedance (Differential)		5 kΩ (min)
Threshold Levels		
Internal (Preset)	mVpp	550 (nom)
External Threshold Adjustment	Vpp	0.0 to 2.0 (adjustable linearly with 0 to 10.0 kΩ potentiometer
Outputs		
RX DATA and RX $\overline{\text{DATA}}$	TTL	10 loads, Manchester II (biphase) serial data
TRANSMITTER		
TX DATA and $\overline{\text{TX DATA}}$	TTL	Driving logic must sink 1.6 mA (max)
Inhibit	TTL	To inhibit transmitter driving logic must sink 1.6 mA (max)
Output Characteristics		
DATA and $\overline{\text{DATA}}$ Differential	Vpp	32 ±4 across 140Ω
Harmonic Content		Filtered to eliminate harmonics above 1 MHz (see figure 2)
Differential Group Delay	ns	±35 (10 KHz to 2 MHz)
Output Noise	mVpp	10
GENERAL		
Power Requirements		
+ 5V Power Supply		
Voltage Tolerance	V	5 ± 5%
Current Drain	mA	35
+ Vcc and – Vcc Power Supplies		
Voltage Tolerance	V	12 to 15
Current Drain		
Idle	mA	75
25% Transmit Duty Cycle	mA	105
100% Transmit Duty Cycle	mA	190
TEMPERATURE		
Operating	°C	–55 to +125
Storage	°C	–55 to +150
PHYSICAL CHARACTERISTICS		
Size	in	1.258 x 1.258 x 0.20 (32 x 32 x 5.1 mm) max
Weight		To be determined

TECHNICAL INFORMATION

The BUS-63102 processes TTL biphase data from a Manchester II encoder, e.g. BUS-8937. The transmitter is inhibited when TX DATA and TX $\overline{\text{DATA}}$ are in the same logic state or when high logic is presented to TX Inhibit. The inhibit function precludes further transmissions and is accomplished, in both cases, by disabling the driver (Figure 1). Waveform shaping functions are performed prior to the output amplifier. A differential gain stage provides a signal splitting function and boosts the signal to 32V nominal, which feeds the driver amplifiers. The driver amplifiers provide a balanced output without external gain circuitry.

The output waveform is derived from the linear phase "band pass" filter, which attenuates frequency components above 1 MHz. Figure 3 is an illustration of an actual output waveform from the BUS-63102. The Symmetrical biphase shape is directly attributed to our filter design.

BUS-63102 accepts biphase differential data at its input and produces DATA and $\overline{\text{DATA}}$ TTL outputs. The positive and negative receiver thresholds may be set internally by grounding the appropriate pins, or externally set with resistors. A LOW at STROBE input inhibits the DATA and $\overline{\text{DATA}}$ outputs. STROBE input should have a resistor pullup to +5 volt if unused.

Figure 4 illustrates a configuration of the BUS-63102 Transceiver coupled to a 1:1 isolation transformer (BUS-27765). When connected as shown, these devices provide a complete transmit/receive interface for MIL-STD-1553 and MACAIR specifications A-3818, A-5232, A-5690 and A-4905. When the BUS-63102 is transmitting, a 32V p-p signal is produced. In the direct coupled mode with the BUS-27765 tapped for a 1:1 ratio and the required isolation resistors in the line, the voltage level is typically 7.6V, p-p at the bus connection points.

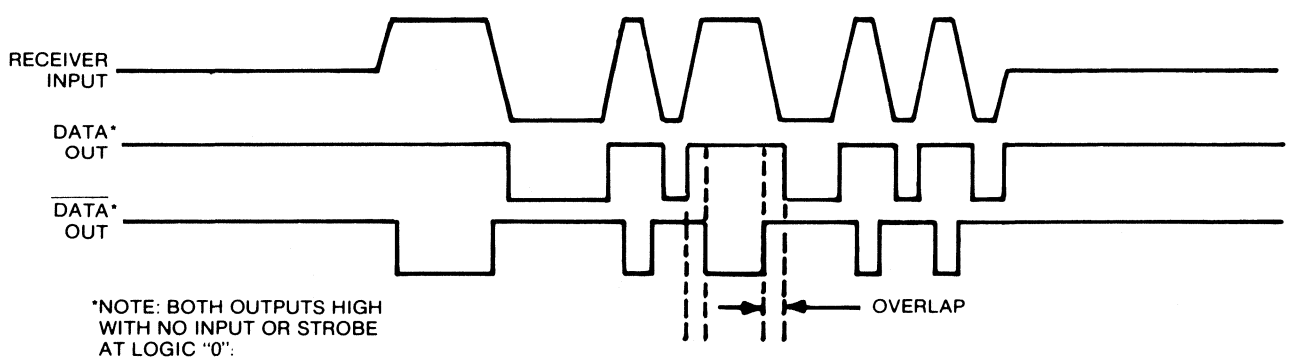


FIGURE 2. RECEIVER WAVEFORMS

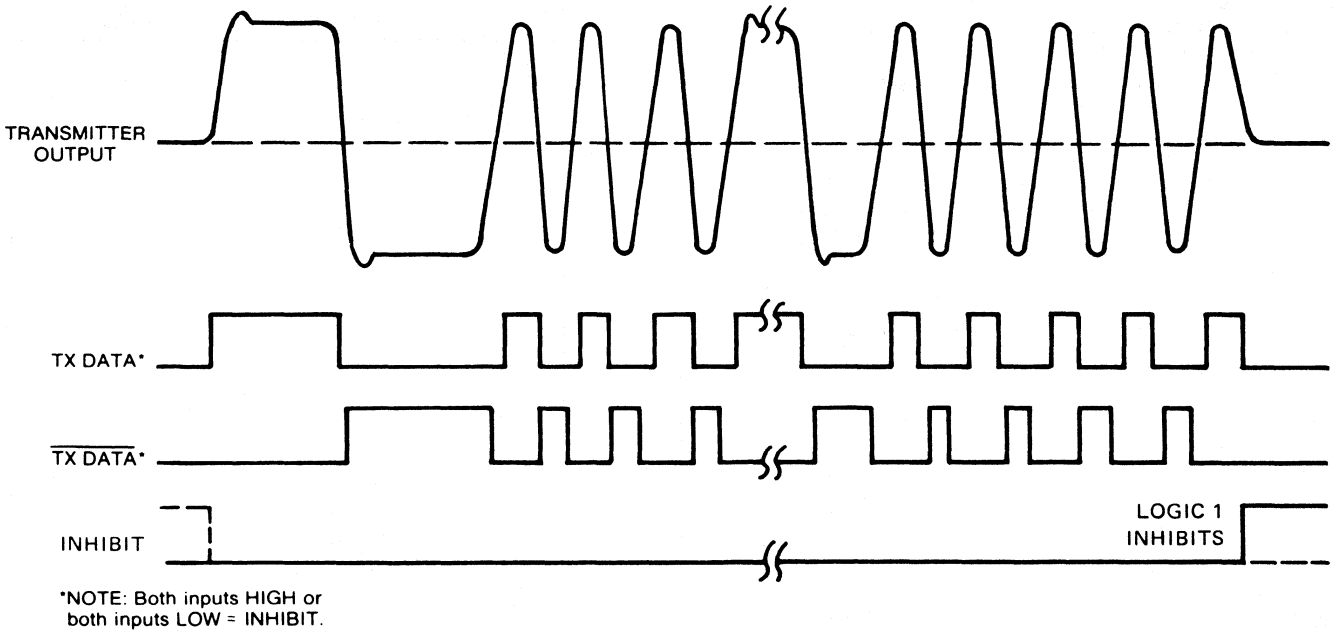


FIGURE 3. TRANSMITTER WAVEFORMS

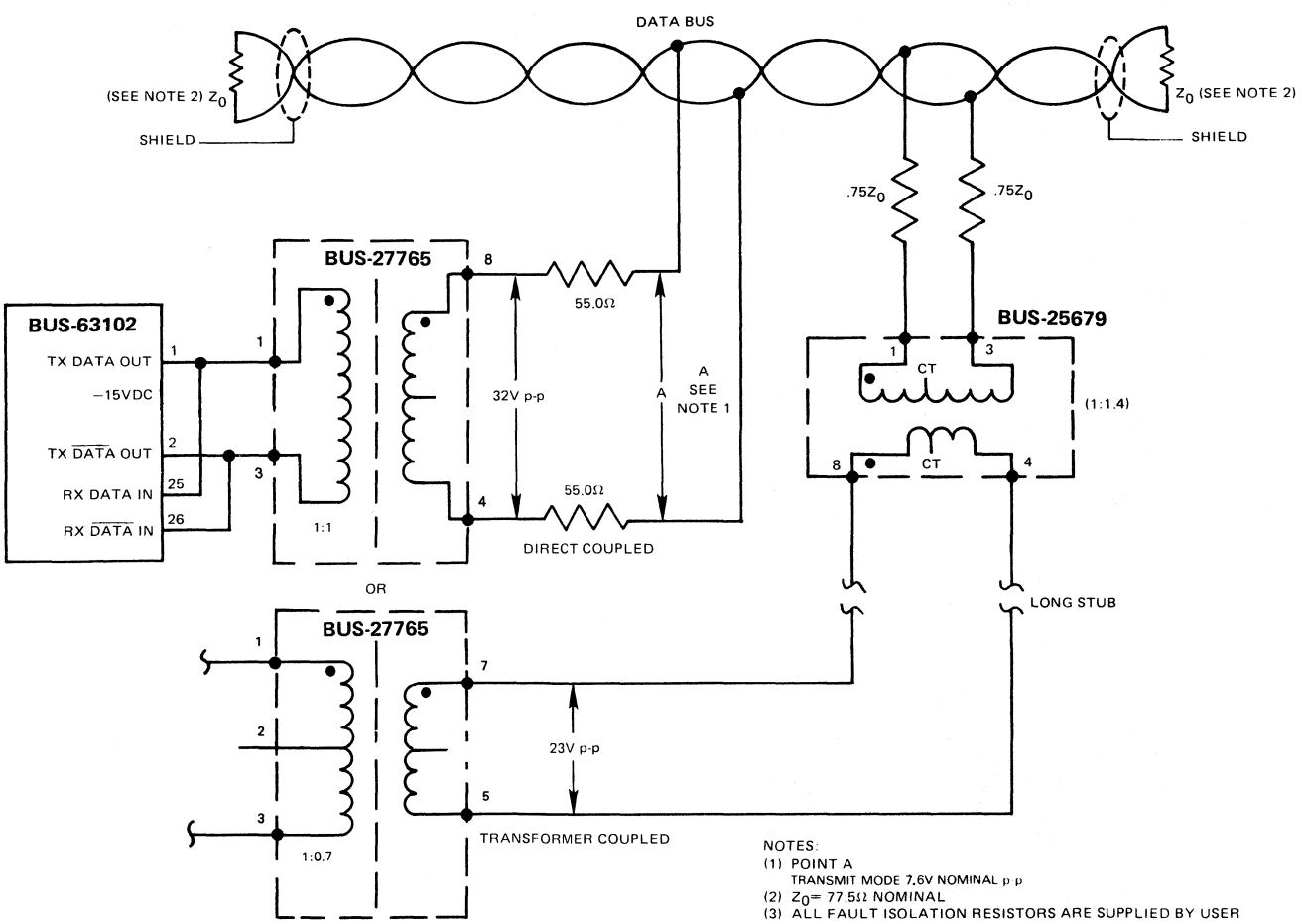
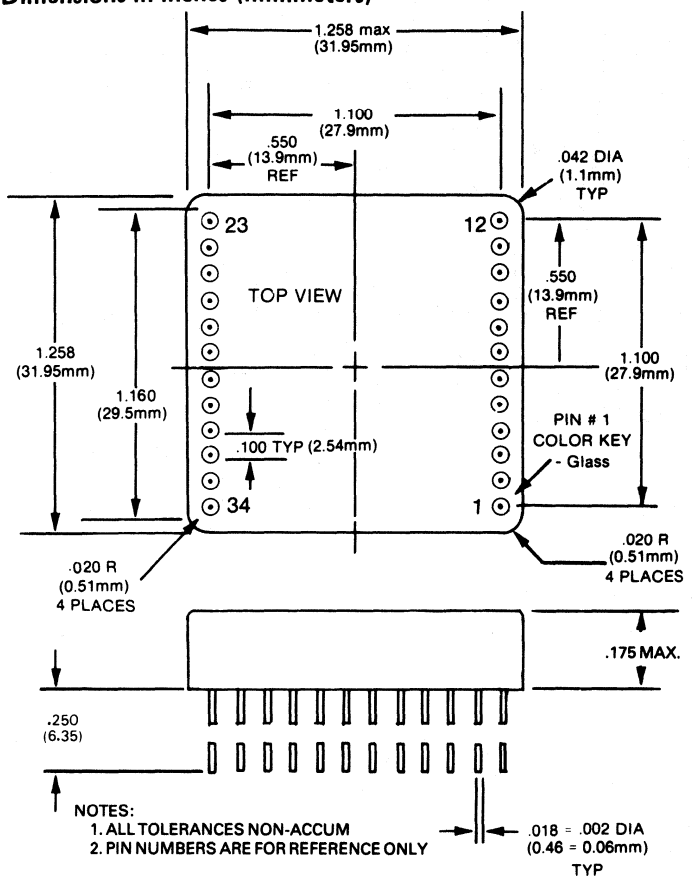


FIGURE 4. BUS COUPLING DIAGRAM

MECHANICAL OUTLINE
24 PIN SQUARE PACKAGE
Dimensions in inches (millimeters)



BUS-63102 PIN CONNECTION TABLE	
PIN	**FUNCTION**
1	TX Data Out
2	TX $\overline{\text{Data}}$ Out
3	GND
4	+ Vcc
5	EXT Data Thresh
6	INT Data Thresh
7	RX Data Out
8	Strobe
9	GND
10	RX $\overline{\text{Data}}$ Out
11	INT $\overline{\text{Data}}$ Thresh
12	EXT $\overline{\text{Data}}$ Thresh
23	+ Vcc
24	N.C.
25	RX Data In
26	RX $\overline{\text{Data}}$ In
27	GND
28	GND (case)
29	− Vcc
30	+5VDC
31	TX Inhibit
32	TX Data In
33	TX $\overline{\text{Data}}$ In
34	− Vcc

ORDERING INFORMATION

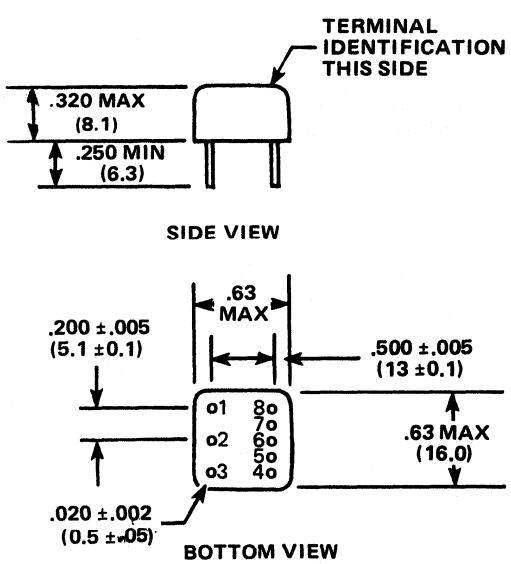
BUS − 63102 − 883B

MIL-STD-883 Processing:
- 883B = Conforms to MIL-STD-883, DDC procedures
- Blank = Same, except pre burn in test and burn in are omitted

TRANSFORMER BUS-27765

NOTE: The transceiver and transformer must be ordered as separate parts.

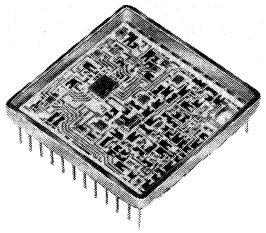
MECHANICAL OUTLINE
TRANSFORMER (P/N BUS-27765)



NOTE:
1. All dimensions are in inches (millimeters)
2. Pin callouts on bottom view are for reference only

BUS-63104

MIL-STD-1553 TRANSCEIVER



DESCRIPTION AND APPLICATIONS

The DDC Model BUS-63104 Transceiver is a complete transmitter and receiver conforming to MIL standards 1553A and 1553B. The receiver section accepts phase-modulated bipolar data at the input and produces a biphase TTL signal at the output (Figure 1). The outputs, DATA and $\overline{\text{DATA}}$, represent positive and negative excursions of the input beyond an internally fixed threshold. These positive and negative thresholds are set at the factory for nominal 750mV p-p signal, measured at point A, Figure 2. External threshold levels of 0 to ±2V, p-p may be selected for specific applications by connecting 0 to 10k ohm resistors between pins 5, 12 and ground. An external strobe input is provided to allow the removal of the receiver from the line. A logic "0" applied to "STROBE" will disable the receiver output.

The BUS-63104 transmitter section accepts biphase TTL data at the input and produces a 30 volt nominal p-p differential signal across a 145Ω load. When coupled to the data bus with a 1:1 transformer, isolated (on the data side) with two 55.0 ohm fault isolation resistors, and loaded by two 70 ohm terminations (plus additional receivers), the data bus signal produced is 6.5 volts nominal p-p measured at point "A" (Figure 2).

When both DATA and $\overline{\text{DATA}}$ inputs are held low or high, the transmitter presents a high impedance to the line. An external inhibit input is provided to allow the removal of the transmitter output from the line (Figure 3). A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the transmitter.

The transceiver is available in a 24 pin hybrid package, measuring 1.25 x 1.25 x 0.2 inches, and can be used in any MIL-STD-1553 transceiver application.

FEATURES

- *FORM-FIT-FUNCTION REPLACEMENT FOR CT3231*
- *MEETS ALL SPECIFICATIONS OF MIL-STD-1553A AND 1553B*
- *IMPROVED FILTERING ON RECEIVER TO ENHANCE BIT ERROR RATE OF SYSTEM*
- *TTL COMPATIBLE*
- *MEETS MIL-STD-883*

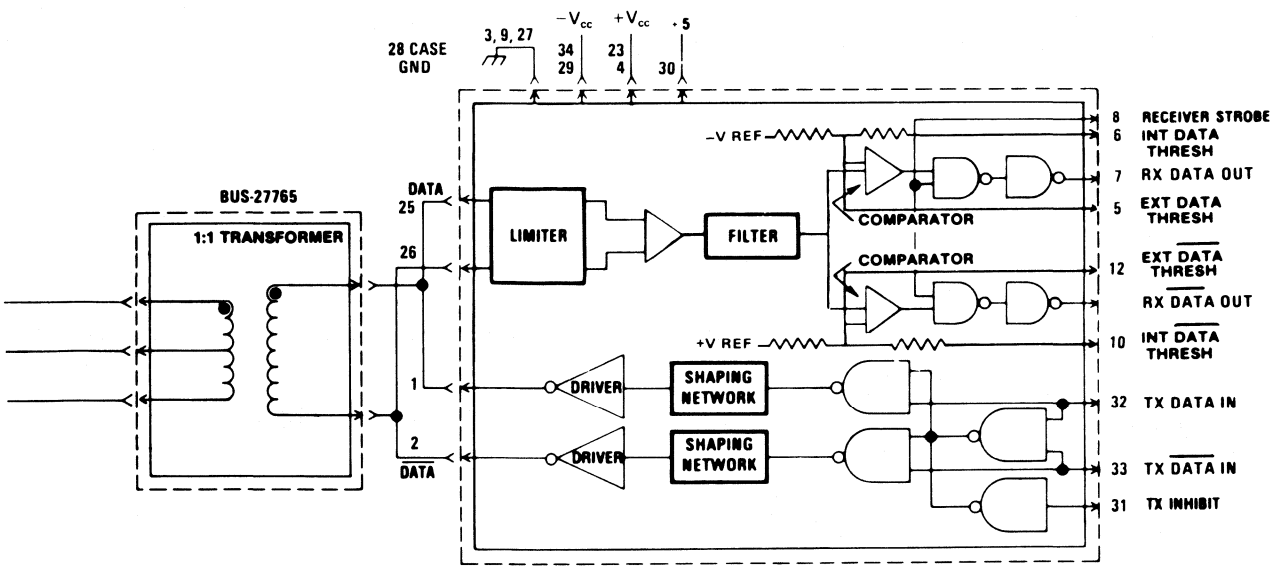


FIGURE 1. BLOCK DIAGRAM

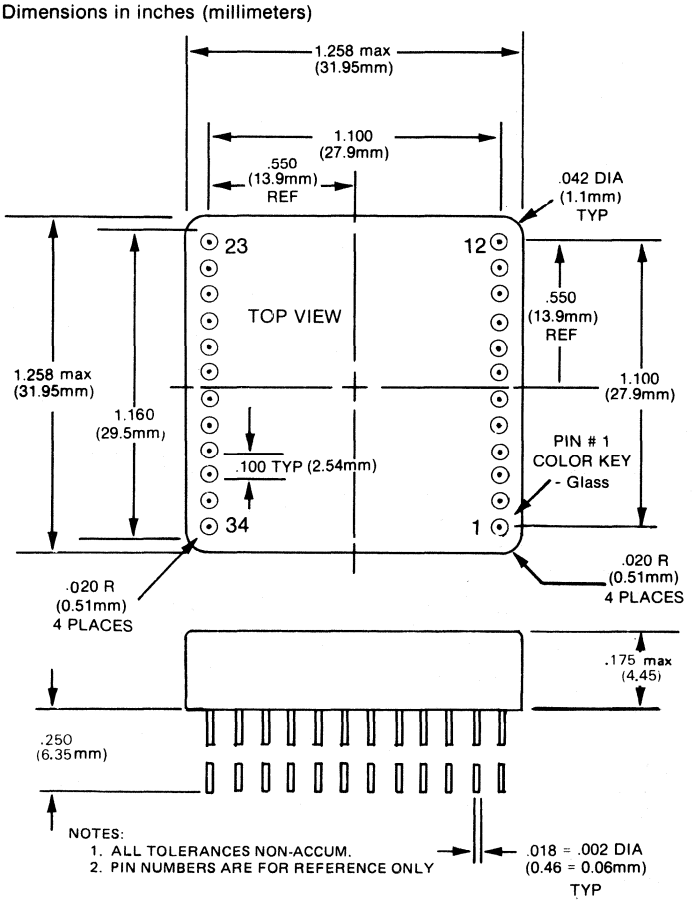
SPECIFICATIONS		
PARAMETER	**UNITS**	**VALUE**
RECEIVER		
Receiver Strobe	TTL	1 load
Analog Inputs		
Bipolar (Differential DATA and $\overline{DATA}$)	Vpp	40 max
Input Impedance (Differential)	Ω	4 k min
Threshold Levels		
Internal (Preset)	mVpp	500 nom, direct coupled, pins 6 and 11 grounded
External Threshold Adjustment	Vpp	0.0 to 2.0 (adjustable with 0 to 10.0 kΩ potentiometers, pin 5 and pin 12 to GND)
Outputs		
RX DATA and RX $\overline{DATA}$	TTL	10 loads, Manchester II (biphase serial data)
TRANSMITTER		
TX DATA and TX $\overline{DATA}$	TTL	1 load
Inhibit	TTL	1 load
Output Characteristics		
DATA and $\overline{DATA}$ Differential	Vpp	30 nom across 140Ω
Rise/Fall Time	ns	130 typ
Output noise	mVpp	10
GENERAL		
Power Requirements		
+5V Power Supply	V	5 ±5%
Current Drain	mA	35
$+V_{CC}$ and $-V_{CC}$ Power Supplies		
Voltage Tolerance	V	12 to 15
Current Drain		
Idle	mA	75
25% Transmit Duty Cycle	mA	105
100% Transmit Duty Cycle	mA	190
TEMPERATURE (CASE)		
Operating	°C	–55 to +125 (case)
Storage	°C	–55 to +150
PHYSICAL CHARACTERISTICS		
Size	in	1.258 x 1.258 x 0.20 (32 x 32 x 5.1 mm)
Weight	oz	0.4 (11 gm)

BUS-63104 PIN CONNECTION TABLE

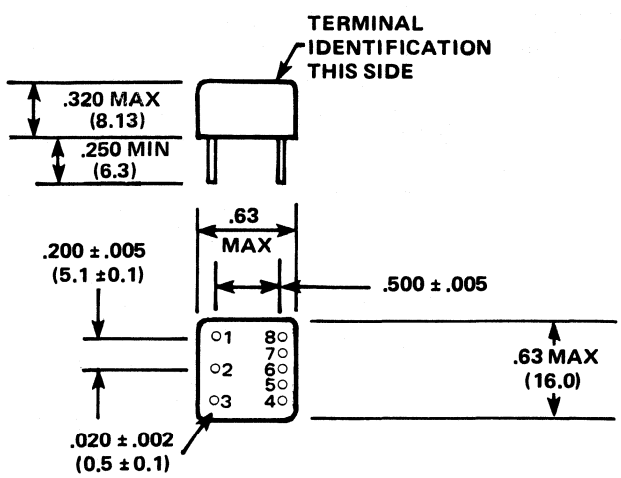
PIN	FUNCTION
1	TX Data Out
2	TX $\overline{Data}$ Out
3	GND
4	+12V to +15VDC
5	EXT Data Thresh
6	INT Data Thresh
7	RX Data Out
8	Strobe
9	GND
10	RX $\overline{Data}$ Out
11	INT $\overline{Data}$ Thresh
12	EXT $\overline{Data}$ Thresh
23	+12 To +15V DC
24	N.C.
25	RX Data In
26	RX $\overline{Data}$ In
27	GND
28	GND (case)
29	-12 To -15VDC
30	+5 VDC
31	TX Inhibit
32	TX $\overline{Data}$ In
33	TX Data In
34	-12 To -15VDC

MECHANICAL OUTLINE BUS-63104
24 PIN SQUARE PACKAGE

Dimensions in inches (millimeters)



MECHANICAL OUTLINE
(BUS-27765)



NOTES:
1. All dimensions are in inches (millimeters)
2. Pin callouts on bottom view are for reference only

Specifications are subject to change without notice.

ORDERING INFORMATION

ORDER:

BUS-63104-883B

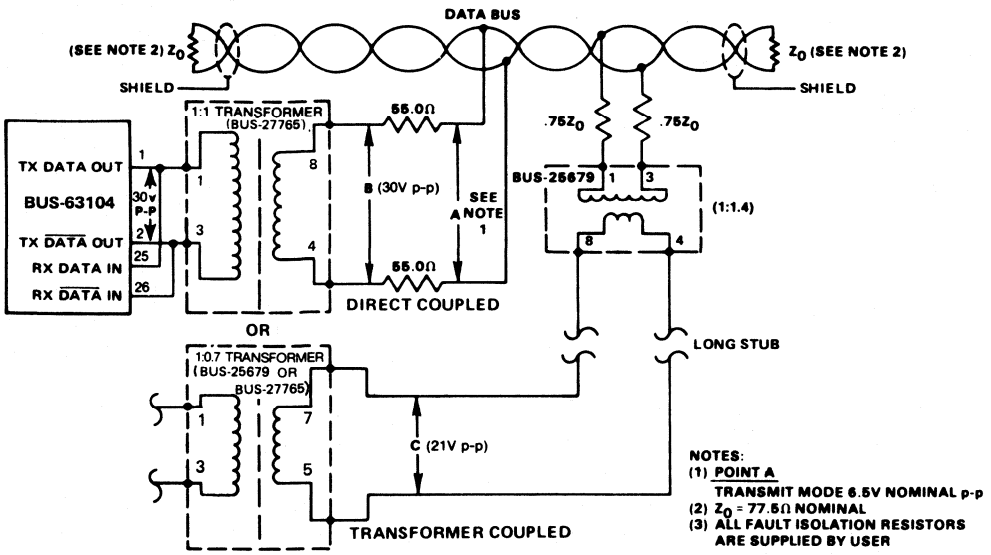


FIGURE 2. TYPICAL TRANSFORMER CONNECTIONS

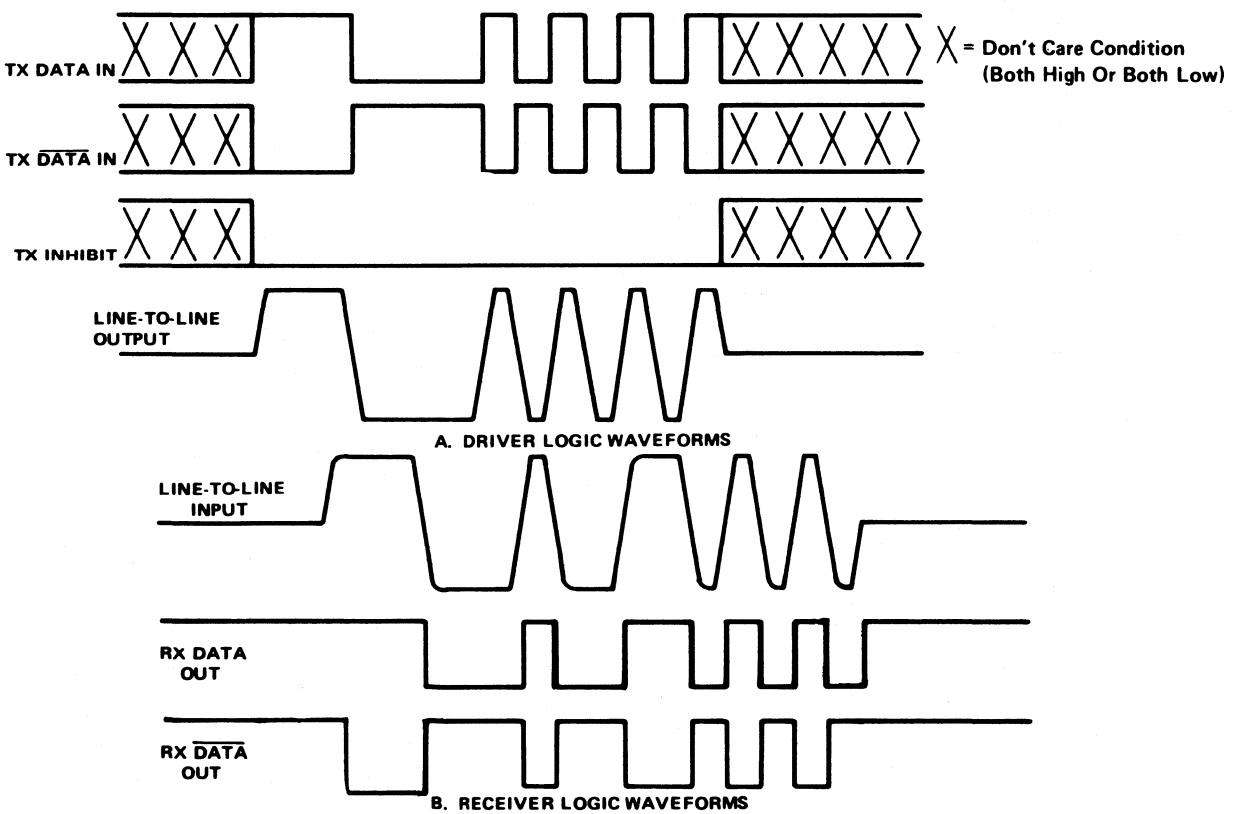
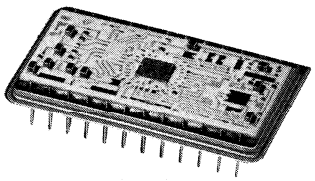


FIGURE 3. LOGIC WAVEFORMS

NOTE: 1) RX DATA and RX DATA lines are high when BUS-63104 is not receiving.
2) When BUS-63104 is used with Harris HD-15530. CMOS Manchester Encoder-Decoder, external inverters must be used on receiver DATA and DATA lines.

SINGLE AND DUAL REDUNDANT MIL-STD-1553 TRANSCEIVERS



DESCRIPTIONS AND APPLICATIONS

The BUS-63105 Series transceivers are complete transmitter and receiver pairs conforming fully to MIL-STD-1553A and B. Available in single (24 pin DIP) and dual redundant (36 pin DIP) configurations, this series is made possible by the development of a custom LSI transceiver chip.

In accordance with MIL-STD-1553A and B, the receiver sections accept phase-modulated bipolar data at the inputs and produce bi-phase TTL signals at the outputs (Figure 1). The outputs, DATA and $\overline{\text{DATA}}$, represent positive and negative excursions of the inputs beyond an internally fixed threshold (Figure 2). These positive and negative thresholds are internally set at the factory for a nominal 1V p-p signal. External strobe inputs are provided to allow the removal of the receivers from the line. A logic "0" applied to the "STROBE" inputs disable the receiver outputs.

The transmitter sections accept bi-phase TTL data at the inputs and produce 27 volt nominal p-p differential signals across a 145Ω load. When coupled to the data bus with the specified transformers, 55.0 ohm fault isolation resistors, and loaded by 70 ohm terminations (plus additional receivers), the data bus signal produced is 6.5 volts p-p nominal. When both DATA and $\overline{\text{DATA}}$ inputs are held low or high, the transmitters present a high impedance to the line. External inhibit inputs are provided to allow the removal of the transmitter outputs from the line. A logic "1" applied to the "INHIBITS" takes priority over the condition of the data inputs and disables the transmitters.

Dual transceiver sections are completely independent, sharing only a common package. All power and signal leads are separate and isolated from one another. There are no common electrical connections.

FEATURES

- *OPTIONS:*
  SINGLE OR DUAL REDUNDANT
  12V OR 15V POWER
  HARRIS OR SMITHS I/O
- *HIGH RELIABILITY—LSI*
- *SMALL SIZE*
  SINGLE – 24 PIN DIP
  DUAL – 36 PIN DIP
- *LOW POWER*
- *SHORT CIRCUIT PROTECTED*
- *INPUT TRANSMITTER PROTECTION TIME OUT CIRCUIT*
- *SUPERIOR FILTERING*

Note: Monobrid® is registered trademark of ILC Data Device Corporation

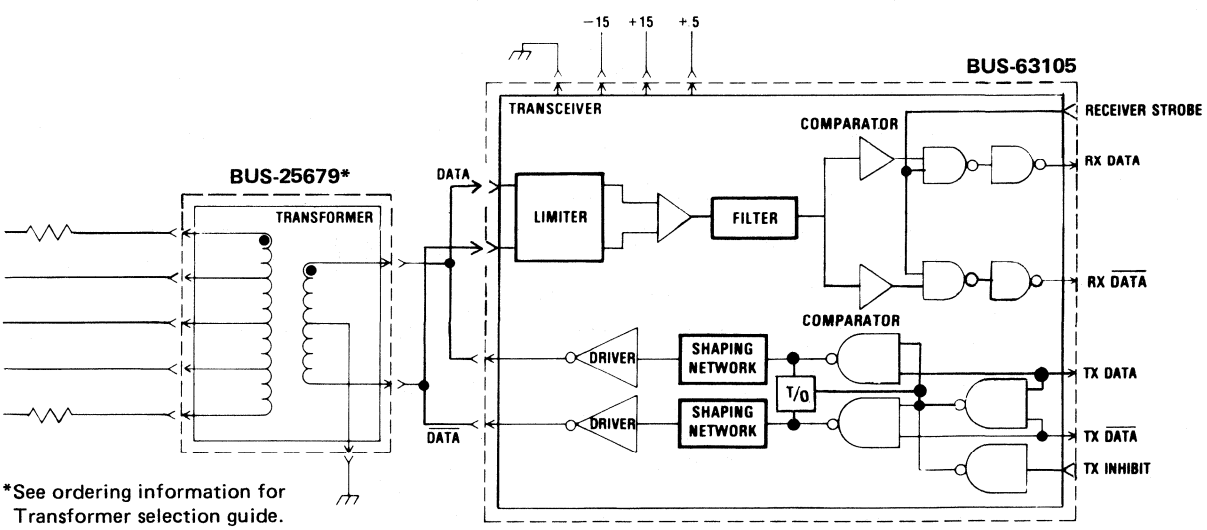
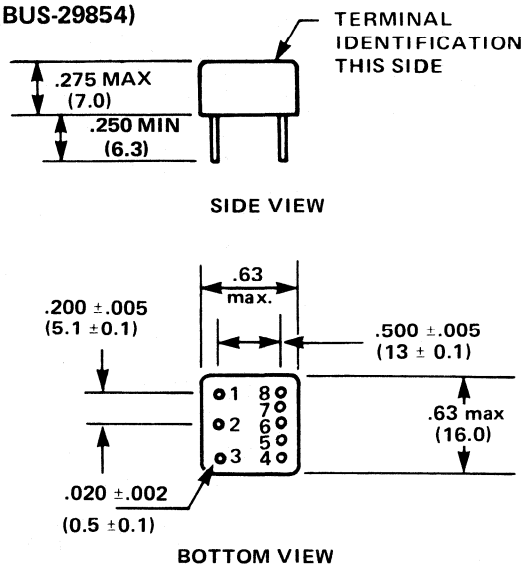


FIGURE 1. BLOCK DIAGRAM

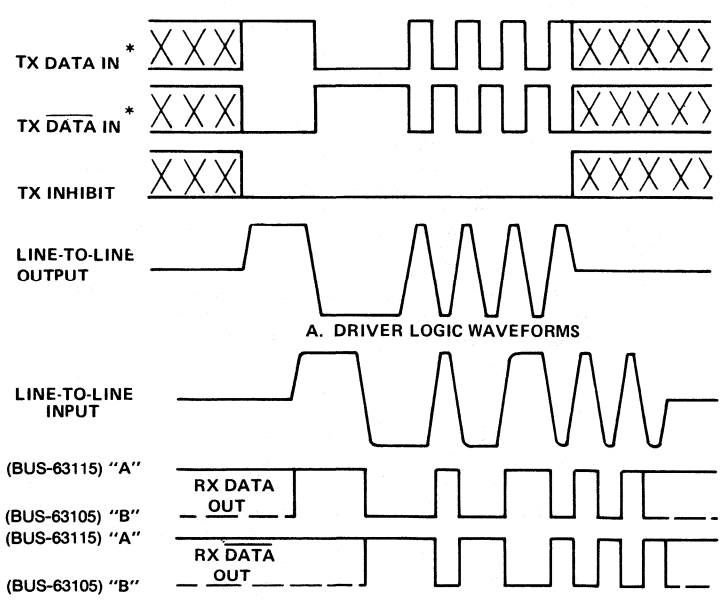
SPECIFICATIONS	
PARAMETER	**VALUE**
RECEIVER (Per Channel)	
Strobe	1 TTL Load
Input Level	40V p-p differential max
Input Impedance	4 KΩ differential min
Threshold Level	1 V p-p nominal, internally set (direct coupled mode)
CMRR	40 dB min. up to 2 MHz Max
Output Level	10 LS TTL Loads
Power Supply Requirements	± 15V (±5%) @ 50 mA max (1) +5V (±10%) @ 17.5 mA max
TRANSMITTER (Per Channel)	
TX Inhibit	1 TTL Load
Input Level	1 TTL Load
Output Level	27V p-p nominal across 145Ω load 20V p-p nominal (measured at point C, Figure 2)
Rise/Fall Time	130 nsec typical
Output Noise	10 mV p-p differential max
Output Impedance (Revceiver Mode)	4 KΩ differential min (at 1 MHz)
Power Supply Requirements	−15V (±5%) @ 90 mA typ @ 25% Duty Cycle 270 mA max @ 100% Duty Cycle +5V (±10%) @ 17.5 mA max
GENERAL	
Operating Temperature Range	−55°C to +125°C (case temp.)
Storage Temperature Range	−55°C to +135°C
Size (24 pin DDIP hybrid)	1.4 x 0.8 x 0.2 inch (36 x 20 x 5mm)
Weight	0.4 oz. typ (11g)
Package	
24 pin DDIP	0.4 oz typ (11g)
36 pin DDIP	1.0 oz typ (28g)

NOTE: (1) For ±12V operation see Ordering Information.

MECHANICAL OUTLINE TRANSFORMER
(BUS-25679)
(BUS-29854)



NOTE:
1. All dimensions are in inches (millimeters)
2. Pin callouts on bottom view are for reference only



*TX DATA and TX DATA lines must be at the same logic state when the transceiver is not transmitting.

FIGURE 2. WAVEFORMS

(See Input Transmitter Protection Time Out Circuit Note.)

OUTPUT LOGIC

The intended application for the BUS-63115 is interfacing with MCE Encoder/Decoder hybrids MT32002, MT32006 or MT32008. The interface waveforms must resemble those shown in "A" of figure 2B. When the transceiver is idle RX Data and RX Data lines are in their high state. The BUS-63105 transceiver is intended to interface with the Harris HD-15530 CMOS Manchester Encoder/Decoder, whose RX Data output waveform is as shown in "B" of figure 2B.

See Ordering Information for transceiver options and transformer selection guide.

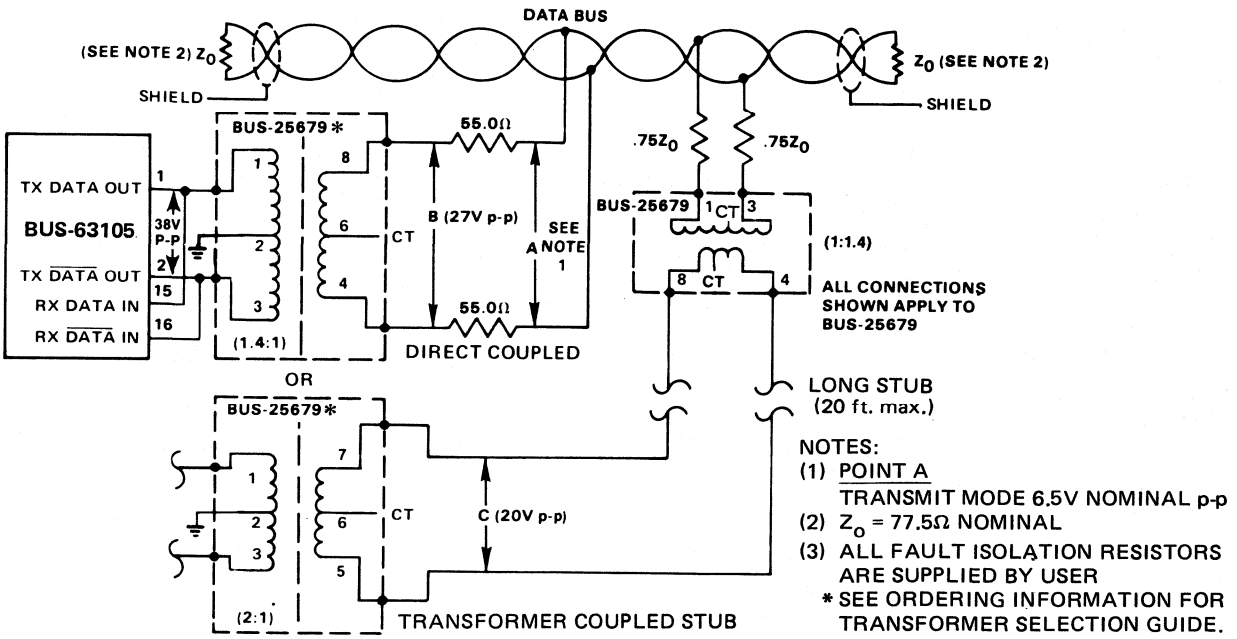
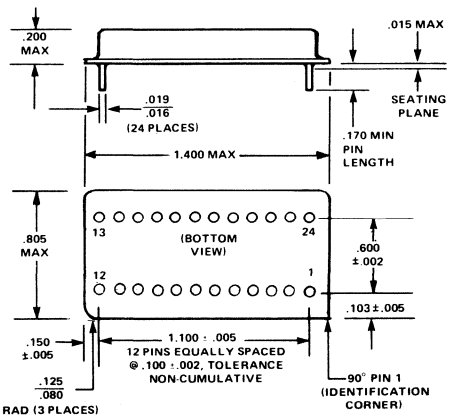


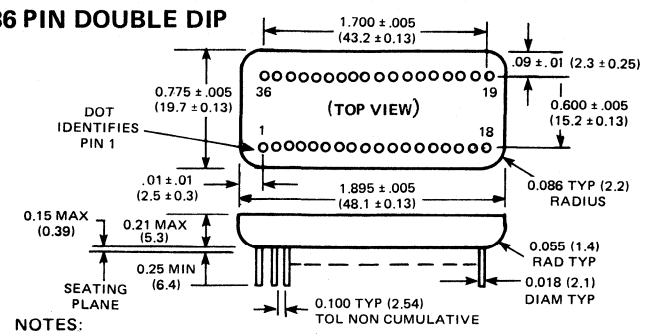
FIGURE 3. TYPICAL TRANSFORMER CONNECTIONS

MECHANICAL OUTLINE—SINGLE CHANNEL 24 PIN DOUBLE DIP



NOTES:
1. Dimensions shown are in inches.
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

MECHANICAL OUTLINE—DUAL REDUNDANT 36 PIN DOUBLE DIP



NOTES:
1. Package is Kovar with electroless nickel plating.
2. Pins are Kovar with gold plating (100μ inch).
3. Case is connected to analog ground.

SINGLE CHANNEL			
PIN	FUNCTION	PIN	FUNCTION
1	TX Data Out	13	+15 VDC
2	TX Data Out	14	N.C.
3	GND†	15	RX Data In
4	N.C.	16	RX Data In
5	N.C.	17	N.C.
6	N.C.	18	GND†
7	RX Data Out	19	−15V DC
8	Strobe	20	+5V DC
9	GND†	21	TX Inhibit
10	RX Data Out	22	TX Data In
11	N.C.	23	TX Data In
12	N.C.	24	Thermal Override††

†GND pins should all be connected externally.
††Thermal Override option is disabled by grounding this pin.

DUAL REDUNDANT					
PIN	FUNCTION		PIN	FUNCTION	
1	TX Data Out	*	19	+15V	**
2	TX Data Out	*	20	RX Data In	**
3	GND†	*	21	RX Data In	**
4	Thermal Override††*		22	GND†	**
5	RX Data Out	*	23	−15V	**
6	Strobe	*	24	+5V	**
7	GND†	*	25	Inhibit	**
8	RX Data Out	*	26	TX Data In	**
9	Case		27	TX Data In	**
10	TX Data Out	**	28	+15V	*
11	TX Data Out	**	29	RX Data In	*
12	GND	**	30	RX Data In	*
13	Thermal Override††**		31	GND†	*
14	RX Data Out	**	32	−15V	*
15	Strobe	**	33	+5V	*
16	GND†	**	34	Inhibit	*
17	RX Data Out	**	35	TX Data In	*
18	N.C.	**	36	TX Data In	*

(*) Channel One (**) Channel Two
†GND pins of each section should all be connected externally.
††Thermal Override is disabled by grounding this pin.

ADDITIONAL FEATURES:

INPUT TRANSMITTER PROTECTION TIME OUT CIRCUIT– If either of the 2 input signals remain high for more than 10-15 μs the transmitter will shut down until the high goes low.

INDEFINITE SHORT CIRCUIT PROTECTION – Output is current limited (*not* fold back) to prevent destruction by overload on the output.

AUTOMATIC THERMAL SHUTDOWN (OPTIONAL)† When internal temperature gets too high the transmitter will shut down to prevent destruction. It will turn back on when temperature returns to an acceptable level. This function can be disabled by pin programming.

ORDERING INFORMATION

BUS-63105-883B

MIL-STD-883 Processing:
- 883B = Conforms to MIL-STD-883 DDC procedures
- Blank = Same, except pre burn in test and burn in are omitted

Options:†
- 5 = Standard, ±15V power
- 7 = ±12V power

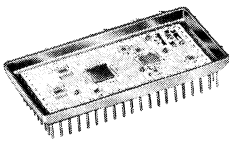
Options:†
- 0 = Single channel, 24 pin DDIP, interface with BUS-8937 and Harris HD-15530
- 1 = Single channel, 24 pin DDIP, interface with MCE (Smith's) chip set (inverted RX Data) and BUS-64100 Bit Processor
- 2 = Dual redundant, 36 pin DDIP, interface with BUS-8937 and Harris HD-15530
- 3 = Dual redundant, 36 pin DDIP, interface with MCE (Smith's) chip set (inverted RX Data) and BUS-64100 Bit Processor.

†Contact factory for thermal shut down option

TRANSFORMER SELECTION GUIDE	
For ±15V Systems Use BUS-25679 and Transceiver	For ±12V Systems Use BUS-29854** and Transceiver
BUS-63105 BUS-63115	BUS-63107 BUS-63117

**BUS-29854 turns ratio:
1:0.83 for direct coupled
1:0.60 for stub coupled

MIL-STD-1553 TERMINAL BIT PROCESSOR



DESCRIPTION

The DDC BUS-64100 is a terminal Bit Processor, which consists of a Manchester II Converter and a DDC advanced custom LSI monolithic chip. Packaged in a single hybrid it has improved reliability and low power dissipation. It is capable of interfacing MIL-STD-1553 transceiver, such as DDC's Monolithic BUS-63115 to an associated subsystem's parallel or serial interface. Its 1 MHz data rate makes it compatible with transceivers that process either McDonnell Douglas MACAIR sinusoidal or trapezoidal waveforms. The BUS-64100 can be used as a common interface for remote terminals, bus monitors or bus controllers.

This unit functions as a decoder per MIL-STD-1553 by transferring all command, status and data words to the subsystem, together with error information, BIT status and necessary handshake signals. It flags Address Recognition, Broadcast and Mode Code decoding terminal fail safe signal and contains a built-in Self-test Circuit.

The subsystem can control the transmission of data through positive handshaking of the logic control lines provided. The unit accepts parallel or serial data then transmits the Command, Status or Data words as directed by the subsystem. By virtue of its extensive input/output logic configuration the BUS-64100 will provide interfacing for BUS Controllers.

The BUS-64100 meets the full specifications of MIL-STD-1553 A & B and those of MACAIR A5690, A3818, A4905 and A5232. The hybrid is available with MIL-STD-883B screening and operates over the full MIL temperature range of −55°C to +125°C.

FEATURES

- *16 BIT OR 8 BIT BYTE PARALLEL OR SERIAL I/O*
- *PERFORMS MIL-STD-1553 FUNCTIONS:*
  - *BROADCAST*
  - *MODE CODE*
  - *OWN ADDRESS*
  - *TIME OUT*
- *ON/OFF LINE SELF-TEST*
- *DUAL RANK REGISTERS*
- *LOW POWER LSI DESIGN*

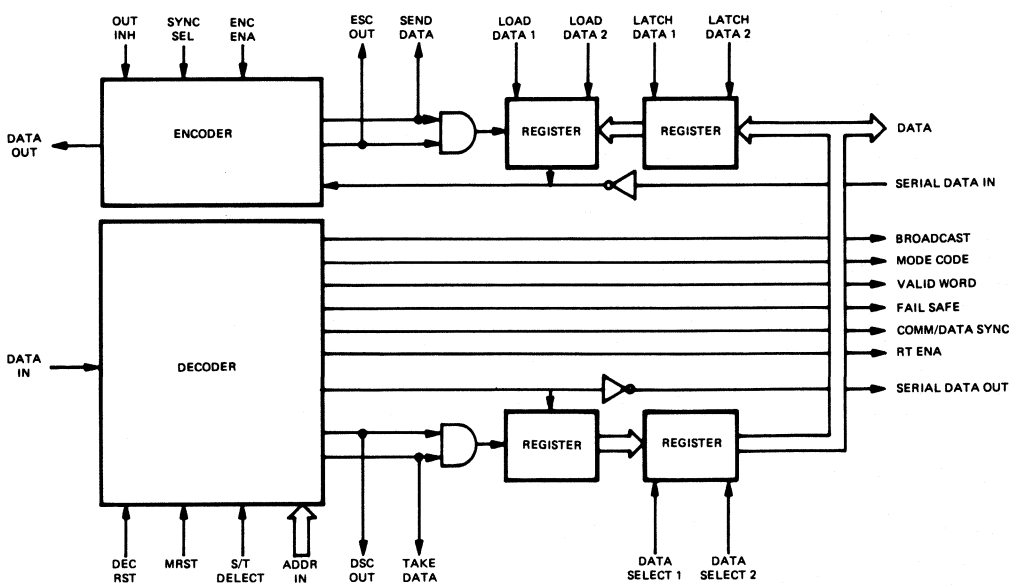


FIGURE 1. BUS-64100 BLOCK DIAGRAM

SPECIFICATIONS

PARAMETER	UNITS	VALUE
LOGIC		
V_{OH} and V_{OL}		See connection and loading table
V_{IH}	V	2 min, +5.5 max
V_{IL}	V	0.7 max. –0.3 min
I_{IH} and I_{IL}	mA	–20 min to +4 mA max
EXTERNAL CLOCK (PIN 17)		
V_{IHC} (Pin 17)	V	VCC –0.5 min/Vcc +.3 max
V_{ILC}	V	GND +0.5 max/GND –.3 min
Loading	Pf	20
I_{IH} and I_{IL}		See Pin 17 connection and loading table
INTERNAL CLOCK OUTPUT (PIN 18)		
V_{OHC}	V	VCC –0.3 min
V_{OLC}	V	GND +0.3 max
I_{OH} and I_{OL}		See Pin 18 connection and loading table
Clock output current	mA	15 max

PARAMETER	UNITS	VALUE
POWER REQUIREMENTS		
Voltage	V	+7.0 max +5.0 ±10% typ
Current	mA	165 typ, 260 max. †
†Consult factory for option with 5VDC current drain of 60 mA.		
XTAL OSCILLATOR (PIN 29)		
XTAL		MIL-C-3098/42 Type CR64/u
XTAL Frequency	MHz	12
I_{OSC}	mA	8 typ
I_{OSC}	mA	13 max
THERMAL CHARACTERISTICS		
Operating	°C	–55 to +125 (Case)
Storage	°C	–65 to +150
PHYSICAL CHARACTERISTICS		
Size	in.	2.155 x 1.155 x 0.200 max (54.7 x 29.3 x 5.1 mm)
Weight	oz.	0.8 max (28g)

ENCODER OPERATION

To initiate a transmission the BUS-64100 must be presented with low logic on the Encoder Enable (ENC ENA) input line. This initializes the applicable internal logic and activates the Encoder Shift Clock. Once the clock is started a stable Sync Select input signal must be provided during a low to high clock transition (figure 2). Parallel input data present on the bidirectional input/output lines is processed through the input registers when the latches, pins 49 and 52 (Latch Data 1 and 2) are high. A low on the Latch Data pins will hold the parallel input data in the register and free the parallel lines for a decoding operation or a self-test condition. The Latch Data command must occur before the Send Data output pulse transitions (low to high). To effect serial shifting of input data to the Encoder the logic on pins 51 and 53 (Load Data) must be set in coincidence with the Send Data output. When Send Data is low the serial to parallel shift registers lock their inputs permitting the Encoder to shift the valid data to the Encoder in a serial stream. By connecting the Load Data input to Send Data output and maintaining high logic on Latch Data the user achieves synchronous control of the parallel to serial shift registers for continuous word transmission. Asynchronous control of transmit data must conform to the parameters shown in Figure 2.

Send Data will remain high for 16 high to low Encoder Shift Clock transitions while the data is shifted out. Termination of a transmission is accomplished by setting the Encoder Enable high prior to the parity bit period. The encoder output may be inhibited at any time during the cycle. When logic low is applied to Output Inhibit, Data and $\overline{\text{Data}}$ are driven low, terminating the transmission. All other control functions are unaffected by the Output Inhibit. A 1 μs (min) logic low presented to Master Reset ($\overline{\text{MRST}}$) completely interrupts a transmission.

The BUS-64100 is configured with dual serial-to-parallel (receive) and parallel-to-serial (transmit), shift registers and dual 8 bit latches to provide 8 bit (2 byte) microprocessor compatibility. By tying parallel I/O lines together, ie. byte 1 MSB to byte 2 MSB and corresponding LSB's for each byte, the sequential operation of Latch Data and $\overline{\text{Load Data}}$ faciliates data transfer in 8 bit bytes.

The BUS-64100 is capable of processing subsystem transmit data in serial format. This requires that transmit data be inputted at the Encoder Shift Clock (ESC) rate and timed with the MSB clocked into the encoder on the low to high transition of Send Data. The parallel to serial input register is made transparent by holding $\overline{\text{Load Data}}$ 1 low throughout the transmission. High logic is imposed on Latch Data 1 to permit the throughput of data on each Encoder Shift Clock pulse.

In accordance with MIL-STD-1553 the BUS-64100 provides a "hardware implemented" time out (Fail Safe) function which terminates transmissions that would exceed 800 μs. After a continuous transmission of 768 μs the BUS-64100 will drive both Data and $\overline{\text{Data}}$ lines low and cause the Time Out (Fail Safe) line to go high.

DECODER OPERATION

The BUS-64100 is designed to begin processing input signals (serial biphase TTL) from compatible MIL-STD-1553 transceiver whenever valid sync and two Manchester II data bits are detected (Figure 3). The decoder outputs a logic state consistent with the sync polarity 50 ns after this

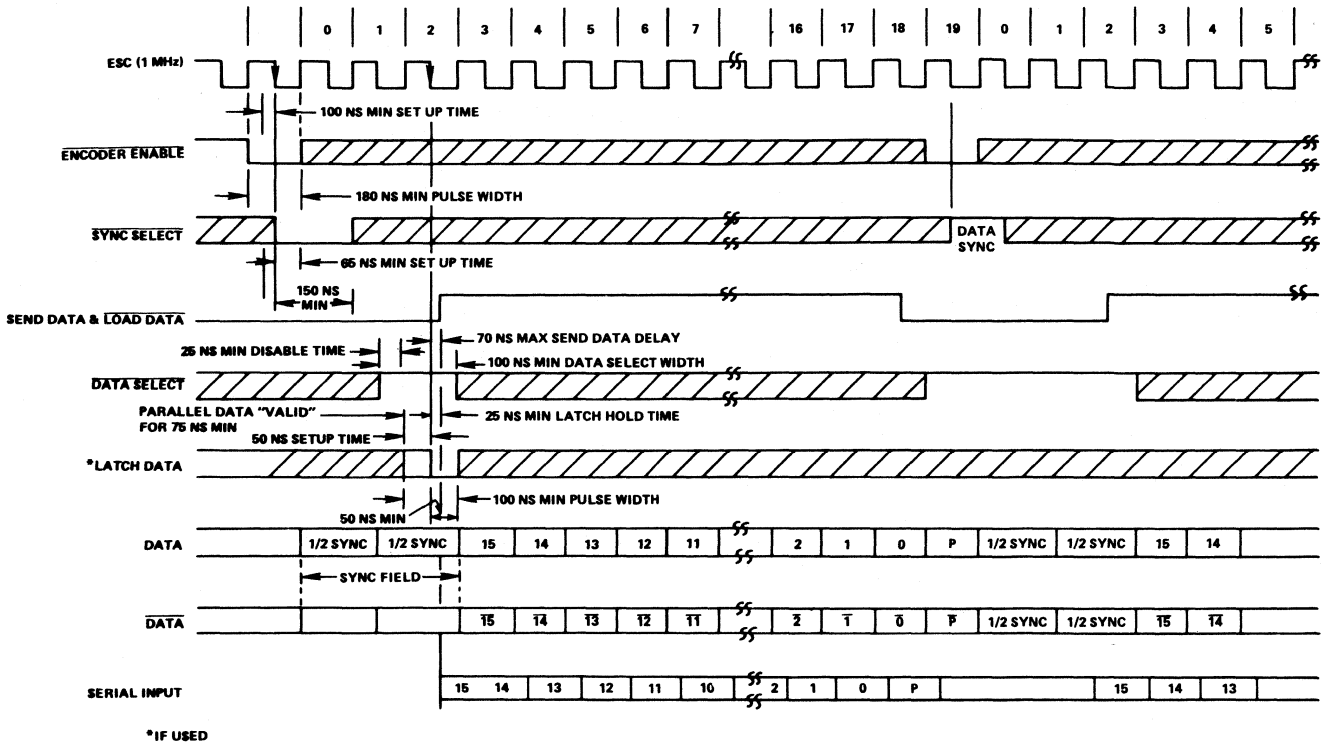
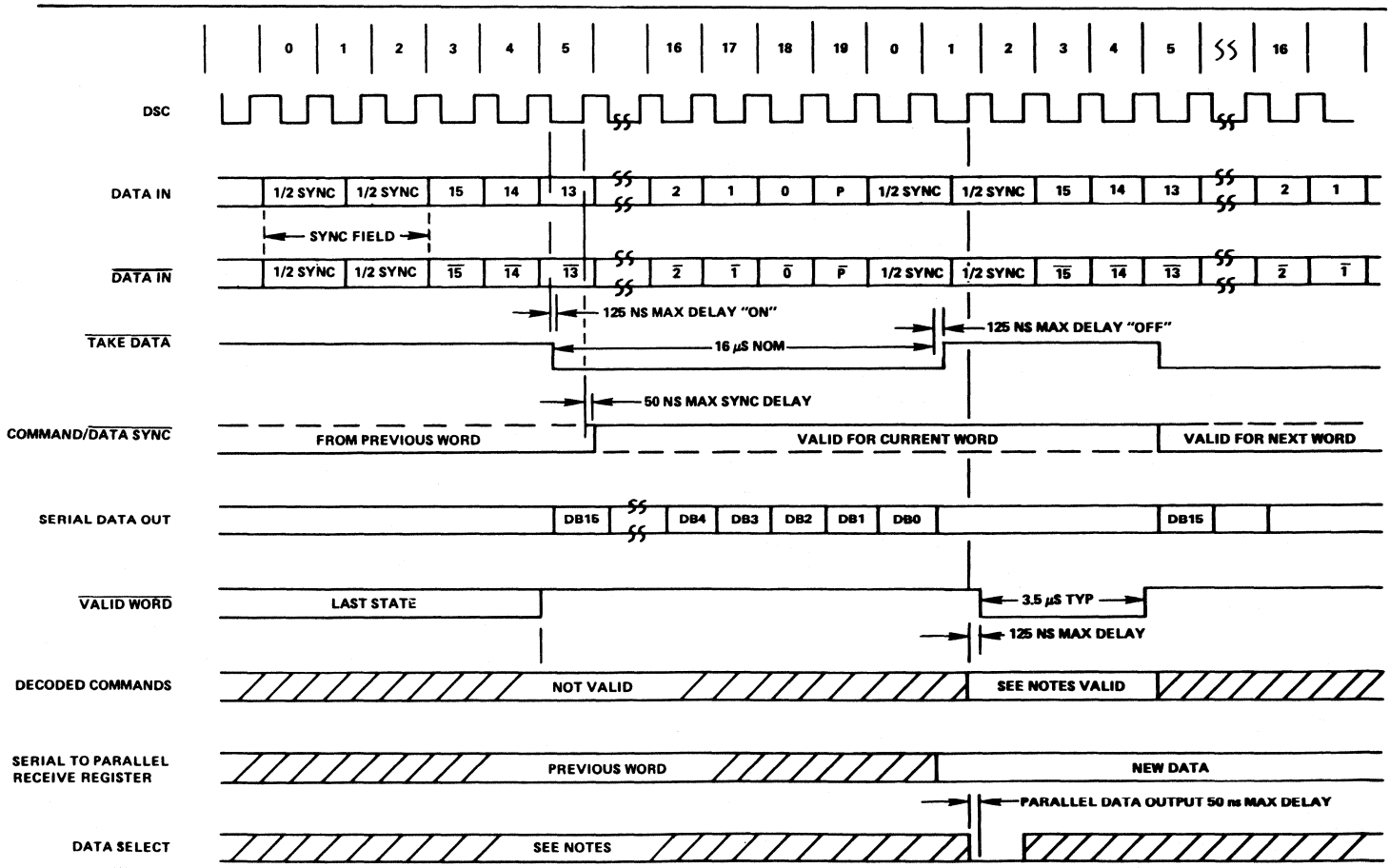


FIGURE 2. ENCODER TIMING



NOTES:

1. Decoded commands are valid during $\overline{\text{VALID WORD}}$ with the following delays (max): Broadcast = 33ns, RT Enable = 65ns.
2. $\overline{\text{DATA SELECT}}$ may be applied at any time that the 16 parallel lines are free, but the parallel data is not updated until 50ns (max) after $\overline{\text{TAKE DATA}}$ goes high.

FIGURE 3. DECODING TIMING

detection. This signal is presented on pin 16 (Command/$\overline{\text{Data}}$ Sync. High logic represents Command or Status Sync and low logic indicates Data Sync.

Once the output on pin 16 is set it will remain so until a Master Reset (pin 38), a $\overline{\text{Decoder Reset}}$ (pin 33) or a new sync field is inputted. The $\overline{\text{Take Data}}$ output logic goes low during this period, permitting serial data to be outputted on pin 36. At the same time the Decoder Shift Clock (DSC) transfers 16 serial bits into the serial-to-parallel shift register.

The $\overline{\text{Master Reset}}$, and when used, the $\overline{\text{Decoder Reset}}$ pulse must be applied for at least 1 μs. The Decoder Reset clears the decoder for reception of a new word, sets the Valid Word line high and Command/$\overline{\text{Data}}$ Sync line low. The $\overline{\text{Master Reset}}$ accomplishes the same clearing functions (receive mode) as the Decoder Reset ($\overline{\text{DEC RST}}$). The Command/$\overline{\text{Data}}$ Sync transition causes the $\overline{\text{Take Data}}$ line to go low resulting in serial data shifting from the decoder to the serial-to-parallel shift register. This commences 125 ns (max) after Command/$\overline{\text{Data}}$ Sync is set. $\overline{\text{Take Data}}$ remains low for 16 Decoder Shift Clock periods. Serial data is clocked out to the Serial Output line (pin 36), while it is being transferred into the serial to parallel shift registers. Once all bits are loaded into the register the Take Data line transitions high to permit transfer of parallel data to the output latches. The data will remain available in the latches until the next low to high transition of $\overline{\text{Take Data}}$. Read out of latched data is accomplished by setting the $\overline{\text{Data Select}}$ lines low (pins 7 and 43). 125 ns max after the $\overline{\text{Take Data}}$ low to high transition.

If a single word is received Valid Word will go high 20 μs after it was set low. Decoder Reset (low logic) will initialize the Valid Word signal to high logic. Decoded commands such as RT Enable, Broadcast and all Mode Codes are subject to the logic state of Valid Word. They will be set high and flagged out on their respective pins when Valid Word goes low.

As in the transmit cycle the bidirectional parallel data lines may be operated in 2, 8 bit bytes for interfacing with an 8 bit microprocessor based subsystem. The LSB for byte 1 is tied to the LSB of byte 2 ie. DØ to D8 and corresponding MSB's of byte 1 are tied to MSB's of byte 2 (D7 to D15).

When interfacing to a serial data system the data is valid beginning on the low to high transition of the Decoder Shift Clock (DSC) after Take Data transitions high to low.

INTERNAL/EXTERNAL CLOCK OPERATION

The BUS-64100 is designed to accept an external 12 MHz clock source or operate on its internal clock. Operation of the internal oscillator requires an external 12 MHz parallel resonant fundamental-mode crystal such as MIL-C-3098/42, TYPE CR64/U. This crystal must be connected to XTAL input (pin 29) and ground. Oscilator/clock Input power requirements are 5V at 13 mA on pin 30. The internal clock can be used to source 1 mA at .3V of VCC and ground. The internal clock output (pin 18) must be tied to the clock input (pin 17) for internal clock operation.

For external clock operation, a 12 MHz oscillator, capable of driving 20 pF to within 0.5V of VCC and ground with a rise and fall time of less than 10 ns is required. No connections are necessary to +5V (pin 30), XTAL (pin 29), clock-out (pin 18) for normal operation from an external clock.

WRAP AROUND SELF TEST

The versatility of the BUS-64100 is realized when the unit is operated in the self test off line configuration. The Self-test input line (S/T Select), when set high, will internally connect DATA and $\overline{\text{DATA}}$ output lines to the decoder's inputs. This S/T Select logic maybe used to inhibit the transceiver, preventing transmissions on the data bus, because DATA and $\overline{\text{DATA}}$ outputs will be active in this mode.

In accordance with MIL-STD-1553B the BUS-64100 has the facilities to conclude transmissions that are not regulated by normal sync field timing or whose duration exceeds 768 μs. An internal timer measures the period between valid sync fields. The BUS-64100 will drive the DATA OUT and $\overline{\text{DATA OUT}}$ low until either a valid command word (with proper address) is received or a Master Reset goes low.

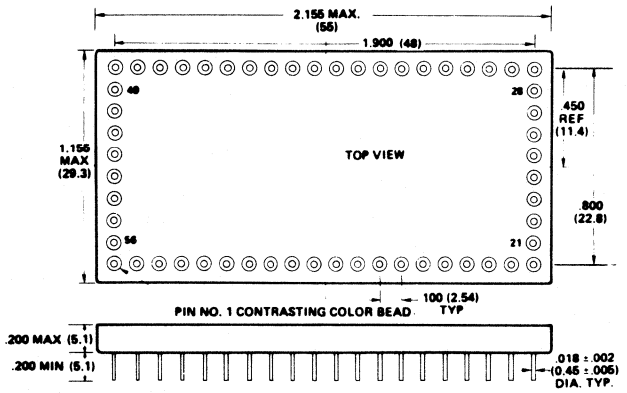
FALSE RT ENABLE:

The BUS-64100 can be used for continuous monitoring, but care must be taken so that it doesn't interpret its own Status Word as a new Command Word received. RT ENABLE flags reception of a valid command (status) word containing the terminal's correct address.

The RT ENABLE may be inhibited to prevent reception of a status word by inverting the SEND DATA signal and applying it to $\overline{\text{DEC RST}}$.

Continuous monitoring of transmissions requires the RT ENABLE transition (high to low) to latch the status word and free the BUS-64100 to transmit. This function is accomplished by presenting a 1 μs (min.) logic low on $\overline{\text{DEC RST}}$ (Pin 33) from an external source immediately after RT ENABLE goes high.

MECHANICAL OUTLINE



PIN NO.	NAME	I_{IH} (μa)	I_{IL} (ma)	I_{OH} (μa)	I_{OL} (ma)	DESCRIPTION
1	Vcc				**	+5V Power Input
2	D8	40	−0.4	−1000	10.0	Part of 16 Bit TRI-STATE I/O
3	D9					
4	D10					
5	D11					
6	D12	40	−0.4	−1000	10.0 **	Part of 16 Bit TRI-STATE I/O
7	$\overline{\text{DATA SELECT 1}}$		20	−0.4		A LOW on this input applies the contents of the SECOND RANK REC'V REG to the D8 thru D15 I/O pins.
8	A3*	−1500	−3.2			Part of 5 Bit ADDRESS INPUT
9	A2*					
10	A1*	−1500	−3.2			Part of 5 Bit ADDRESS INPUT
11	GROUND					Logic and power return
12	A4*	−1500	−3.2			MSB of 5 Bit ADDRESS INPUT
13	$\overline{\text{A0}}$*	−1500	−3.2			LSB of 5 Bit ADDRESS INPUT
14	$\overline{\text{VALID WORD}}$			−400	4.0	A LOW on this output indicates receipt of a valid word.
15	FAIL SAFE			−400	4.0	A HIGH on this output indicates termination of a transmitted message that exceeded 768 μs.
16	COMM/$\overline{\text{DATA}}$ SYNC			−380	3.8	A HIGH on this output indicates COMMAND (or STATUS) word reception. A LOW indicates DATA word reception.
17	CLOCK IN	±1	±.001			Input for 12 MHz clock (20 pf load). See text for clock requirements.
18	CLOCK OUT			−1000	1.0	Output of OSCILLATOR AND CLOCK DRIVER (see text for description.)
19	S/T SELECT	40	−0.8			A HIGH on this input sets the unit in the self-test mode.
20	CASE					CASE CONNECTION
21	DATA IN	20	−0.4			A HIGH on this input represents a positive state on the bus.
22	$\overline{\text{DATA IN}}$	20	−0.4			A HIGH on this input represents a negative state on the bus. (Pins 21 & 22 must both be high when the bus is inactive).
23	$\overline{\text{ENC ENA}}$	20	−0.4			A LOW on this input initiates a transmit cycle.
24	$\overline{\text{SYNC SEL}}$	20	−0.4			Actuates COMMAND (or STATUS) sync for an input LOW and DATA sync for an input HIGH.
25	DATA OUT			−360	3.2	A HIGH on this output produces a positive state on the bus.
26	$\overline{\text{DATA OUT}}$			−360	3.2	A HIGH on this output produces a negative state on the bus.
27	SEND DATA			−360	3.6	A HIGH on this output indicates data shifting during the transmit cycle.
28	ESC OUT			−1000	1.2	LOW and HIGH transitions on this output during HIGH SEND DATA cause the transmit cycle data shifting to occur.
29	XTAL					A 12 MHz (parallel resonant) crystal is connected between this pin and ground.
30	+5V OSC/ CLOCK POWER					+5V power for OSCILLATOR AND CLOCK DRIVER.
31	DSC OUT			−1000	1.2	LOW to HIGH transistions on this output during LOW $\overline{\text{TAKE DATA}}$ cause receive cycle data shifting to occur.
32	RT ENABLE			−400	4.0	A HIGH on this output indicates reception of a valid COMMAND (or STATUS) word containing the terminal's address. It also resets the FAIL SAFE.

NOTES: In the above table, the symbols are defined as follows:
I_{IH} = maximum input HIGH current with V_{in} = 2.5 volts
I_{IL} = maximum input LOW current with V_{in} = 0.4 volts
I_{OH} = maximum output HIGH current for V_{out} = 2.5 volts minimum
I_{OL} = maximum output LOW current for V_{out} = 0.4 volts maximum

*Indicates use of an internal pull-up resistor

**Option available with I_{OL} = 0.8 mA which reduces 5VDC current drain to 60 mA.

PIN NO.	NAME	I_{IH} (μa)	I_{IL} (ma)	I_{OH} (μa)	I_{OL} (ma)	DESCRIPTION
33	$\overline{\text{DEC RST}}$	20	−0.4			A LOW on this input (for 1 μs minimum) resets the decoder to a condition ready for a new word, resets the $\overline{\text{COMM/DATA}}$ SYNC output LOW, and resets the $\overline{\text{VALID WORD}}$ output HIGH.
34	GROUND					Logic and power return.
35	$\overline{\text{OUTPUT INH}}$	20	−0.4			A LOW on this input holds output pins 25 and 26 LOW.
36	SERIAL DATA OUT			−400	4.0	The received serial data in NRZ format is available at this pin during LOW $\overline{\text{TAKE DATA}}$.
37	$\overline{\text{TAKE DATA}}$			−360	3.2	A LOW on this output indiciates data shifting during the receive cycle. A LOW to HIGH transition on this pin always transfers the current contents of the FIRST RANK REC'V REG to the SECOND RANK REC'V REG.
38	$\overline{\text{MRST}}$	60	−1.2			A LOW on this input (for 1μs minimum) interrupts and clears the transmit cycle, resets the $\overline{\text{FAIL SAFE}}$, and also performs the same functions as $\overline{\text{DEC RST}}$.
39	BROADCAST*			−300	1.6	A HIGH on this output indicates reception of a valid COMMAND (or STATUS) word containing all ONES in the address field.
40	$\overline{\text{MODE CODE}}$*			−600	8.0	A LOW on this output indicates reception of a valid COMMAND (or STATUS) word containing all ONES or all ZEROS in the sub-address field.
41	D6	40	−0.4	−1000	10.0**	Part of 16 Bit TRI-STATE I/O
42	D7	40	−0.4	−1000	10.0**	Part of 16 Bit TRI-STATE I/O
43	$\overline{\text{DATA SELECT 2}}$	20	−0.4			A LOW on this input applies the contents of the SECOND RANK REC'V REG to the DØ thru D7 I/O pins.
44	D5	40	−0.4	−1000	10.0**	Part of 16 Bit TRI-STATE I/O
45	DØ					LSB of 16 Bit TRI-STATE I/O
46	D1					Part of 16 Bit TRI-STATE I/O
47	D2					Part of 16 Bit TRI-STATE I/O
48	D3	40	−0.4	−1000	10.0**	Part of 16 Bit TRI-STATE I/O
49	LATCH DATA 2	20	−0.4			A HIGH on this input allows the I/O data on DØ thru D7 to appear at the output of the FIRST RANK XMT REG. A LOW on this input holds the register outputs in their last state.
50	D4	40	−0.4	−1000	10.0**	Part of 16 Bit TRI-STATE I/O.
51	$\overline{\text{LOAD DATA 2}}$	60	−1.2			A LOW on this input loads the DØ thru D7 data into the SECOND RANK XMT REG. A HIGH on this input then locks out the data inputs to permit serial shifting.
52	LATCH DATA 1	20	−0.4			A HIGH on this input allows the I/O data on D8 thru D15 to appear at the output of the FIRST RANK XMT REG. A LOW on this input holds the register outputs in their last state.
53	$\overline{\text{LOAD DATA 1}}$	60	−1.2			A LOW on this input loads the D8 thru D15 data into the SECOND RANK XMT REG. A HIGH on this input then locks out the data inputs to permit serial shifting.
54	D13	40	−0.4	−1000	10.0**	Part of 16 Bit TRI-STATE I/O
55	D14	40	−0.4	−1000	10.0**	Part of 16 Bit TRI-STATE I/O
56	D15	40	−0.4	−1000	10.0**	MSB OF 16 Bit TRI-STATE I/O and OPTIONAL SERIAL INPUT.

NOTES: In the above table, the symbols are defined as follows:
I_{IH} = maximum input HIGH current with V_{in} = 2.5 volts
I_{IL} = maximum input LOW current with V_{in} = 0.4 volts
I_{OH} = maximum output HIGH current for V_{out} = 2.5 volts minimum
I_{OL} = maximum output LOW current for V_{out} = 0.4 volts maximum

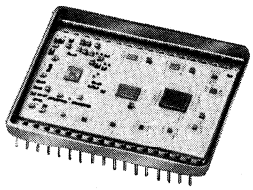
*indicates use of an internal pull-up resistor
**Option available with I_{OL} = 0.8 mA which reduces 5VDC current drain to 60 mA.

ORDERING INFORMATION

ORDER: BUS-64100-883B

Note: Consult factory for low current drain option.

MIL-STD-1553 DUMB RTU HYBRID



DESCRIPTION

The BUS-65101 MIL-STD-1553 Dumb Remote Terminal Unit (RTU) consists of a transceiver, and encoder/decoder, control logic, dual rank I/O registers and internal clock oscillator packaged in a 1.6" x 1.9" hermetic hybrid. It provides all the functions required to interface between a MIL-STD-1553 serial MUX data bus and a subsystem parallel 3-state data highway. Utilizing several DDC custom monolithic ICs, the BUS-65101 provides sufficient handshaking, control and data lines to permit versatile operation as a remote terminal, a bus controller or a bus monitor, in either single or dual redundant data bus configurations.

As a transmitter, the BUS-65101 accepts 8 bit or 16 bit parallel data from the subsystem, and outputs serial Manchester II coded Command, Status or Data words, under subsystem control. As a receiver, it accepts serial MIL-STD-1553 transmissions and transfers all Command, Status and Data words to the 8 bit or 16 bit data highway, under subsystem control. The BUS-65101 also provides flags to the subsystem when Broadcast, Mode Code, and Own Address (with parity) commands are decoded.

The BUS-65101 contains a terminal fail-safe timeout circuit which flags message lengths exceeding 768 microseconds, and terminates serial data transmission. Wraparound self-test is initiated by a control line which causes the encoder serial output to be connected to the decoder input. The BUS-65101 provides a serial output of decoded words, thus allowing Command Word look-ahead, for the fastest terminal response.

FEATURES

- *INCLUDES:*
  - *TRANSCEIVER*
  - *ENCODER/DECODER*
  - *DUAL RANK I/O REGISTERS*
  - *FAIL-SAFE TIMER*
  - *CLOCK OSCILLATOR*
- *SMALL 1.6 " x 1.9 " HYBRID*
- *PROVIDES FLAGS FOR:*
  - *OWN ADDRESS (WITH PARITY)*
  - *MODE CODE*
  - *BROADCAST*
  - *TIME OUT*
  - *VALID WORD*
  - *SYNC TYPE*
- *16 BIT OR 8 BIT 3-STATE PARALLEL I/O AND SERIAL OUT*
- *WRAPAROUND BUILT-IN TEST*
- *SIMPLE CONTROLS FOR SINGLE OR DUAL REDUNDANT DATA BUS CONFIGURATIONS*

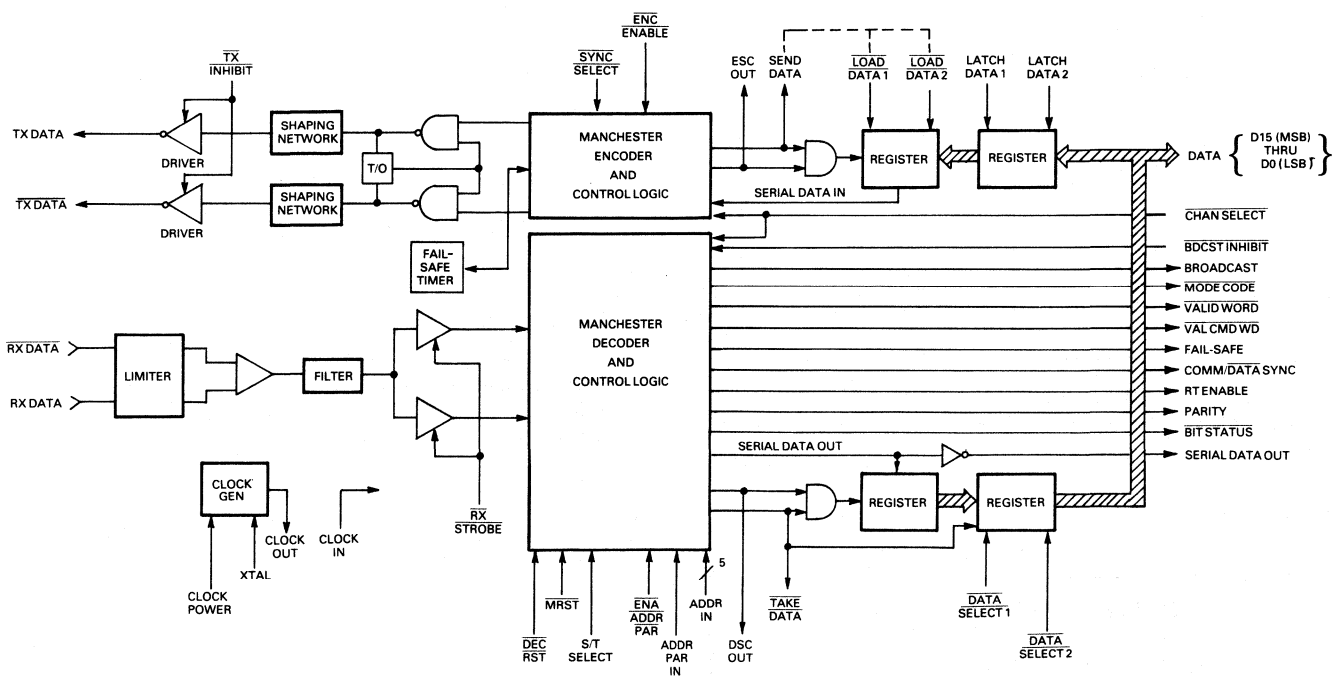


FIGURE 1. BUS-65101 BLOCK DIAGRAM

SPECIFICATIONS – Values at nominal power supply voltages.		
PARAMETER	**UNITS**	**VALUE**
RECEIVER		
Differential Input Impedance (DC to 1MHz)	KΩ	4 min
Differential Input Voltage	V_{p-p}	40 max
Input Threshold (Direct Coupled)	V_{p-p}	1 typ
CMRR (DC to 2MHz)	dB	40 min
CMV (DC to 2MHz)	V	±10 min
RX STROBE Characteristics	TTL Loads	1 typ
TRANSMITTER		
Differential Output Voltage		
Direct Coupled (across 145Ω Load)	V_{p-p}	30 typ
Transformer Coupled (at Stub)	V_{p-p}	21 typ
Output Rise and Fall Times	ns	130 typ
Output Noise	mV_{p-p}	10 max
TX INHIBIT Characteristics	TTL Loads	1 typ
LOGIC		
I_{IH}, I_{IL}, I_{OH}, I_{OL}		See pin function & loading table.
V_{OH}	V	2.5 min
V_{OL}	V	0.4 max
V_{IH}	V	2.0 min
V_{IL}	V	0.7 max
CLOCK		
V_{OHC} (Internal Clock)	V	Supply −0.3Vmin
V_{OLC} (Internal Clock)	V	Ground +0.3V max
V_{IHC} (External Clock)	V	Supply −0.5V min
V_{ILC} (External Clock)	V	Ground +0.5V max
POWER SUPPLIES		
+5V OSC/CLOCK Supply		
Voltage Tolerance	%	±10
Current Drain	mA	8 typ; 13 max
+5V Logic Supply		
Voltage Tolerance	%	±10
Current Drain	mA	250 max
+15V (or +12V) Supply		
Voltage Tolerance	%	±5
Current Drain	mA	65 max
−15V Supply (BUS-65102)		
Voltage Tolerance	%	±5
Current Drain		
Idle	mA	65 max
25% Transmit	mA	105 max
100% Transmit	mA	250 max
−12V Supply (BUS-65101)		
Voltage Tolerance	%	±5
Current Drain		
Idle	mA	65 max
25% Transmit	mA	125 max
100% Transmit	mA	330 max
TEMPERATURE RANGE (Case)		
Operating	°C	−55 to +125
Storage	°C	−55 to +135
PHYSICAL		
Size	in. (mm)	1.6x1.9x0.21 (40.4x46.9x5.3)
Weight	oz (gm)	1 max (28)

GENERAL

As shown in the block diagram of Figure 1, the BUS-65101 provides all functions required to implement a Dumb Remote Terminal Unit (RTU). It is designed for the greatest flexibility and ease of use. BUS-65101 can be operated with either an internal or external clock. Simple control lines are provided to interface with either an 8 bit or 16 bit parallel data highway, in either single channel or dual redundant configurations.

Control lines are available to implement either on line or off line wraparound built-in test. BUS-65101 can be configured to perform a parity check on its hard-wired terminal address. It provides numerous output flags to simplify the user interface. These flags indicate various decoded messages, as well as the results of error checks. Sync selection, along with the flexible controls, allows the BUS-65101 to operate as a Bus Controller as well as a Remote Terminal.

INTERNAL OR EXTERNAL CLOCK

BUS-65101 may be operated with either its internal clock or an external clock. Internal clock operation requires that a 12 MHz parallel-resonant fundamental-mode crystal, such as MIL-C-3098/42 TYPE CR64/U, be connected between pin 18 (XTAL) and ground. In addition, +5 volt power must be connected to pin 2 (OSC/CLOCK POWER), and CLOCK OUT (pin 19) must be connected to CLOCK IN (pin 24).

For external clock operation, no connection is made to pin 2 (OSC/CLOCK POWER), and the external clock is applied to pin 24 (CLOCK IN). Pin 19 (CLOCK OUT) is not connected. The external clock must be capable of driving a load of 20 picofarads to within 0.5 volts of the +5 volt power supply and to within 0.5 volts of ground. Standard TTL voltage levels will not work properly. It must have a rise time and fall time of less than 10 nanoseconds. For compliance with MIL-STD-1553, the external clock frequency must be 12 MHz.

8 BIT OR 16 BIT INTERFACE

The BUS-65101 may be configured to interface with either 8 bit or 16 bit parallel data highways. For 16 bit operation, the 16 data lines (D15 through D0) are used directly. LATCH DATA 1 and LATCH DATA 2 are tied together, as are DATA SELECT 1 and DATA SELECT 2. This allows data transfer in 16 bit bytes.

For 8 bit parallel data highways, the 16 data lines must be tied together in eight pairs (D15 to D7, D8 to D0, etc.) The two LATCH DATA and DATA SELECT signals are used independently. This allows transfer in two 8 bit bytes.

ADDRESS WITH PARITY

The BUS-65101 provides five lines for hard-wired terminal address. Internal pull-up resistors are provided on these lines, so logic "1" lines may be left open-circuited. Logic "0" lines must be grounded. The BUS-65101 may be configured to check the parity of these five address lines. This function can be selected by using the ENA PAR CHECK line. The address parity line (TMADDP) is hard-wired for odd address parity if the function is used. The ODD PARITY output flag indicates a valid check for odd parity of the six address lines.

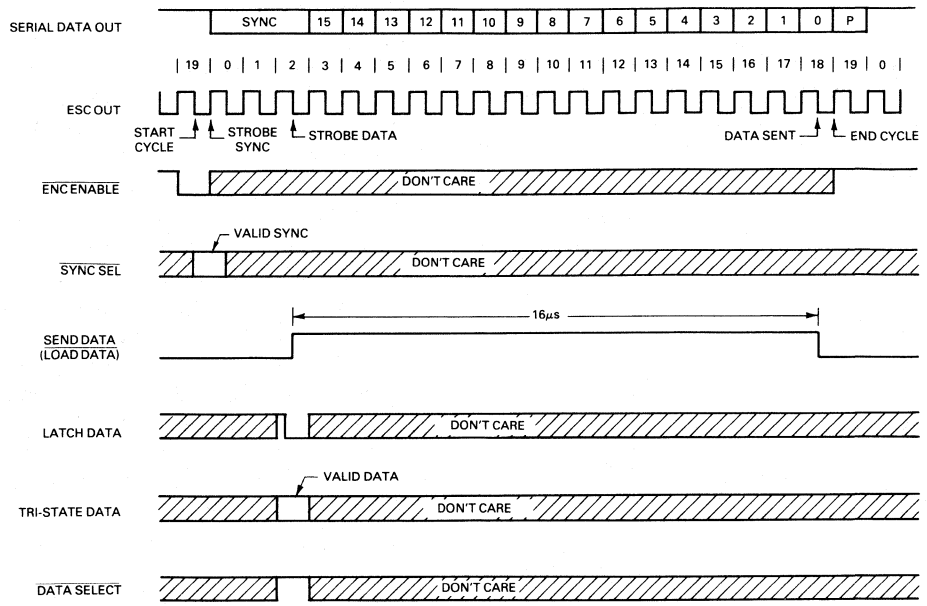


FIGURE 2. TRANSMIT MODE TIMING

DUAL REDUNDANT OPERATION

The BUS-65101 may be used in a dual redundant configuration with a minimum of additional circuitry. A CHAN SELECT signal is provided which simultaneously disables the LATCH DATA, DATA SELECT, and ENC ENABLE lines of the BUS-65101. Therefore, CHAN SELECT can be used to multiplex a single set of LATCH DATA, DATA SELECT and ENC ENABLE control signals between two BUS-65101 units, which have these signals tied together in parallel.

WRAPAROUND BUILT-IN TEST

The BUS-65101 may be configured to implement either on line or off line wrap around built-in test. By enabling the receiver with RX STROBE during a normal transmission, the encoded word will be fed back into the decoder by the receiver. In this on line wrap around mode of operation, the BUS-65101 compares each decoded word that is fed back with the original word that was encoded. The BIT STATUS output flag indicates when the two words are not the same.

Care must be taken when using this on line wrap around test technique because an outgoing status word will be interpreted by the decoder as a new command word. Since the status word has the correct address and the same sync as a command word, the BUS-65101 will set RT ENABLE and VAL CMD WD. For on line wrap around operation, it is therefore necessary to reset RT ENABLE after transmission of a status word. This can be accomplished by inverting SEND DATA and applying it to DEC RST during status word transmission. If it is required that the status word be fed back, RT ENABLE should be reset immediately after it goes HIGH by applying a LOW to DEC RST for 1 microsecond (minimum). The status word will be available at the receive register.

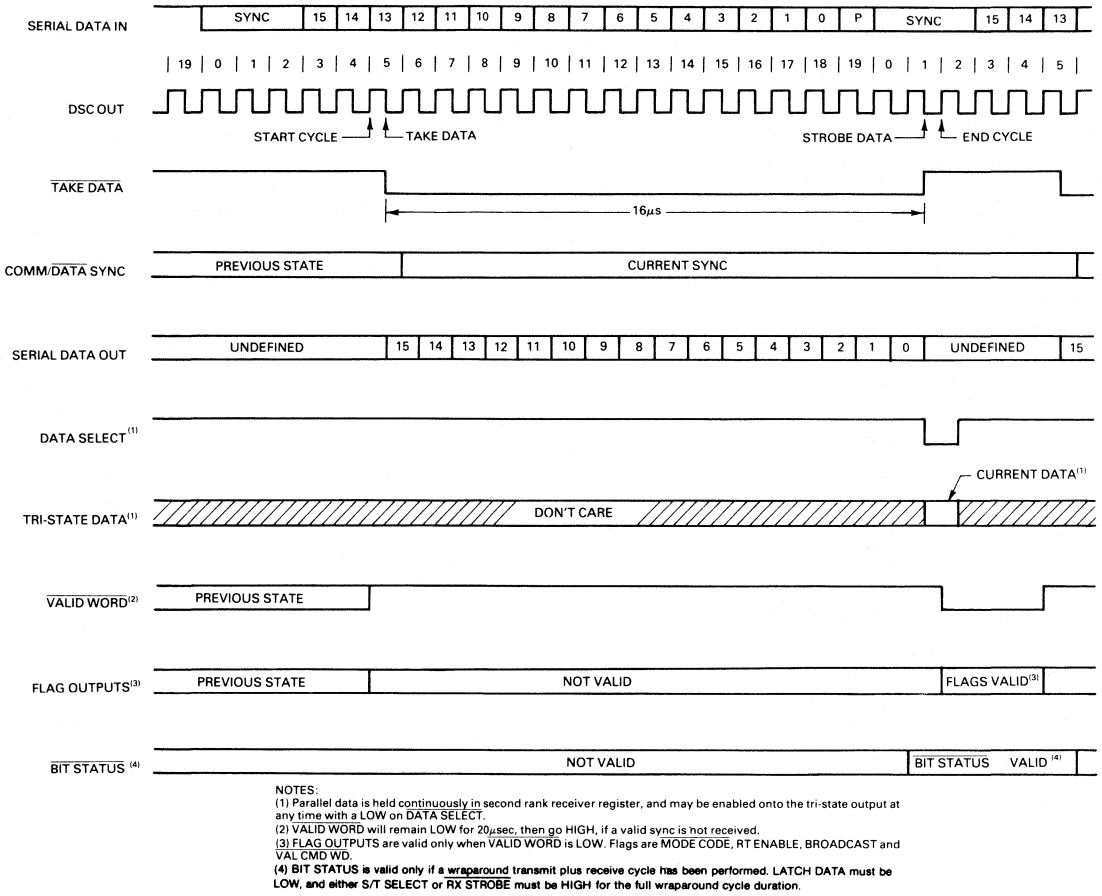
The BUS-65101 can be placed in an off line wrap around test mode by use of the S/T SELECT signal. In this mode, the transceiver is disabled and the encoder output is fed directly to the decoder input. All other functions remain the same, and the BUS-65101 compares each word that is decoded with the original word that was encoded. The BIT STATUS line also indicates the result of this comparison for the off line wrap around test.

FAIL-SAFE TIMEOUT

The BUS-65101 contains a timer which continuously monitors the length of each transmitted message. This timer detects a transmitted message which exceeds 768 microseconds and causes the transmission to terminate. At the same time, the FAIL-SAFE flag is set to indicate a Terminal Fail-Safe Timeout. Further transmissions are inhibited until the FAIL-SAFE flag is reset by MRST or a valid command word with the correct address is received.

OUTPUT FLAGS

The BUS-65101 provides numerous output flags to offer the greatest user flexibility. VALID WORD indicates receipt of a word with valid sync, Manchester coding and parity. RT ENABLE indicates a valid word and correct address. VAL CMD WD indicates a valid word and a Command Sync. BROADCAST indicates a valid command word and an address of 11111. The BROADCAST flag may be inhibited by using the BDCST INHIBIT line. MODE CODE indicates a valid command word and a subaddress of 11111 or 00000.



NOTES:
(1) Parallel data is held continuously in second rank receiver register, and may be enabled onto the tri-state output at any time with a LOW on DATA SELECT.
(2) VALID WORD will remain LOW for 20μsec, then go HIGH, if a valid sync is not received.
(3) FLAG OUTPUTS are valid only when VALID WORD is LOW. Flags are MODE CODE, RT ENABLE, BROADCAST and VAL CMD WD.
(4) BIT STATUS is valid only if a wraparound transmit plus receive cycle has been performed. LATCH DATA must be LOW, and either S/T SELECT or RX STROBE must be HIGH for the full wraparound cycle duration.

FIGURE 3. RECEIVE MODE TIMING

INITIALIZATION

To ensure error-free operation, it is desirable to reset the BUS-65101 to its initialized state upon power turn-on. The MRST (master reset) signal is provided for this purpose. Both the decoder and encoder, as well as all flags, are reset by a LOW on MRST. This function interrupts and overrides all other control signals. The MRST function can also be used during fault recovery routines.

TRANSCEIVER OPERATION

The BUS-65101 contains a transceiver similar to DDC's model BUS-63105. When connected to a serial MUX data bus via transformer and isolation resistors, as shown in Figure 6, the BUS-65101 transceiver will fully comply with MIL-STD-1553. The correct DDC part numbers for transformers used in direct-coupled and transformer-coupled operation are shown in Figure 6 and Ordering Information.

Transceiver TX INHIBIT and RX STROBE signals are provided to afford flexible operation. These signals may be used to disable the transmitter and receiver, respectively. The BUS-65101 transceiver contains a transmitter protection timeout circuit. If either of the two transmitter inputs remain high for longer than 15 microseconds, the timeout circuit will shut off the transmitter until the fault condition disappears. Short circuit protection is provided, with current limited outputs, for an indefinite period.

ENCODER OPERATION

Figure 2 illustrates the transmit mode timing. Encoder detail timing is shown in Figure 4. The transmit cycle is initiated by a LOW on ENC ENABLE. The first HIGH to LOW (falling edge) transition of ESC OUT, when ENC ENABLE is LOW, starts the cycle which lasts for 20 clock periods of the 1 MHz ESC OUT. The next LOW to HIGH transition of ESC OUT strobes the SYNC SELECT line. A HIGH on SYNC SELECT produces a data sync and a LOW produces a command/status sync.

A LOW to HIGH transition of SEND DATA occurs at the fourth falling edge of ESC OUT. This indicates the completion of the sync interval and the start of the serial data interval. Parallel data must be stable at the second rank transmit register prior to the rising edge of SEND DATA, which occurs 3 microseconds (minimum) after the HIGH to LOW transition of ENC ENABLE. LATCH DATA is used to transfer parallel data to the first rank transmit register. LATCH DATA must be brought LOW and DATA SELECT brought HIGH prior to the rising edge of SEND DATA. If

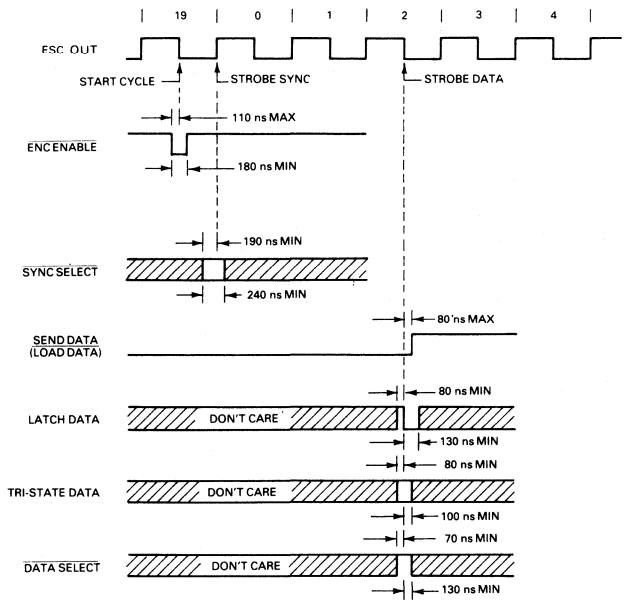


FIGURE 4. ENCODER DETAIL TIMING

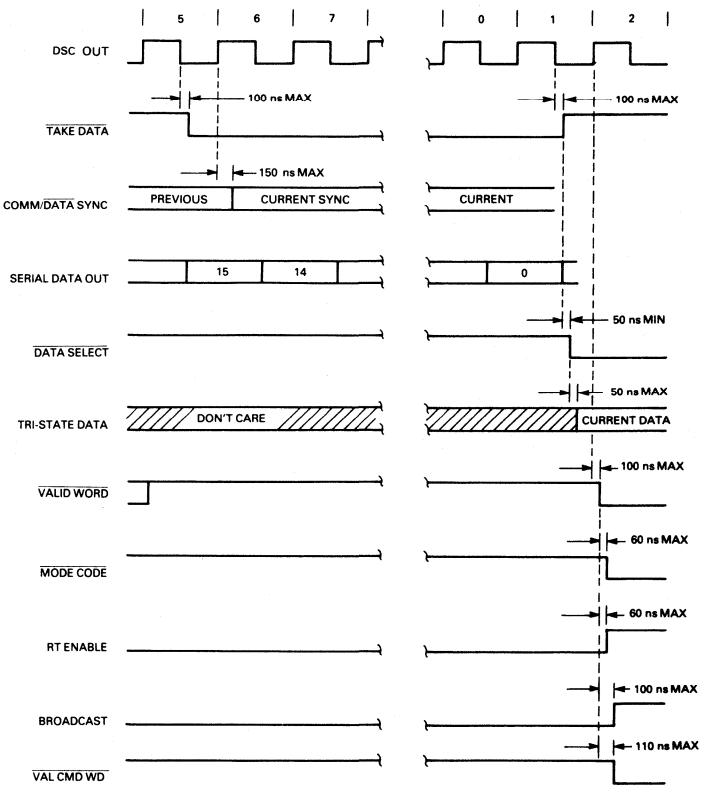


FIGURE 5. DECODER DETAIL TIMING

SEND DATA is connected directly to LOAD DATA, it will lock out the second rank transmit register and serial data shifting into the encoder will proceed properly.

For multiple word transmissions, the next word may be transferred to the transmit register any time after SEND DATA goes HIGH, but no later than the next LOW to HIGH transition of SEND DATA. SEND DATA remains HIGH for 16 periods of ESC OUT, during which time the data word is serially shifted to the Manchester encoder. The encoder adds the parity bit during the next ESC OUT period after SEND DATA goes LOW. To terminate transmission after any word, ENC ENABLE must go to HIGH no later than the first rising edge of ESC OUT after SEND DATA goes LOW.

The entire transmit cycle may be interrupted and initialized by applying a 1 microsecond (minimum) negative pulse to MRST. It is possible to input data to the encoder in serial form by forcing both transmit registers to be transparent. With LATCH DATA 1 held HIGH and LOAD DATA 1 held LOW, serial data input on D15 will be be applied directly to the encoder serial input. ESC OUT must be used to shift in the serial data, MSB first, starting at the LOW to HIGH transition of SEND DATA.

DECODER OPERATION

Figure 3 illustrates the receive mode timing. Decoder detail timing is shown in Figure 5. A receive cycle, which lasts for 20 clock periods of the 1 MHz DSC OUT, is initiated when the decoder recognizes a valid sync and two valid Manchester data bits. TAKE DATA goes LOW at the first HIGH to LOW (falling edge) transition of DSC OUT, following the second valid data bit. COMM/DATA SYNC is updated at the next rising edge of DSC OUT after TAKE DATA goes LOW. COMM/DATA SYNC remains in its new state until the next valid word or until DEC RST or MRST goes LOW.

TAKE DATA remains LOW for 16 periods of DSC OUT, during which time the 16 serial data bits are shifted into the first rank receive register. The serial data is simultaneously available at SERIAL DATA OUT as it is being shifted. At the completion of decoded data shifting, TAKE DATA goes HIGH, which transfers the data to the second rank receive register. This data may be enabled onto the parallel data highway by a LOW on DATA SELECT at any time until the next rising edge of TAKE DATA.

At the first rising edge of DSC OUT after TAKE DATA goes HIGH, VALID WORD is updated. It will go LOW if the decoded word was valid. VALID WORD will go HIGH at the start of the next receive cycle, or after 20 microseconds if no additional words are received. All output flags are enabled by VALID WORD, and therefore they are valid only as long as VALID WORD is LOW.

PIN FUNCTION AND LOADING TABLE

PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
1	GND					Power supply and logic return.
2	+5V OSC/ CLOCK POWER					+5V Power for oscillator and clock driver.
3	NC					No connection.
4	$\overline{\text{TX INHIBIT}}$	20	−0.4			A LOW on this input inhibits the transmitter.
5	$\overline{\text{SYNC SELECT}}$	20	−0.4			A HIGH on this input results in a transmitted DATA sync. A LOW on this input results in a transmitted COMMAND (or STATUS) sync.
6	SERIAL DATA OUT			−0.4	4.0	Received serial data in NRZ format is available at this output when $\overline{\text{TAKE DATA}}$ is LOW.
7	ESC OUT			−0.4	4.0	LOW to HIGH transitions on this output when SEND DATA is HIGH causes the transmit cycle data shifting to occur.
8	NC					No connection.
9	COMM/$\overline{\text{DATA}}$ SYNC			−.36	3.6	A LOW on this output indicates receipt of a DATA word. A HIGH indicates receipt of a COMMAND (or STATUS) word.
10	$\overline{\text{MRST}}$	40	−0.8			A LOW on this input (1 μsec minimum) resets the decoder to its initialized condition (same function as $\overline{\text{DEC RST}}$), resets FAIL-SAFE, and stops and clears the transmit cycle. This function interrupts and overrides all other controls.
11	$\overline{\text{VALID WORD}}$			−0.4	4.0	A LOW on this output indicates receipt of a valid word.
12	$\overline{\text{BIT STATUS}}$			−0.4	4.0	A LOW on this output, during wrap around self test only, indicates that the last word decoded was identical to the last word encoded.
13	LATCH DATA 1	20	−0.4			A HIGH on this input causes parallel tri-state I/O data on D8 through D15 to appear at the output of the first rank transmit register. A LOW locks out the register inputs.
14	$\overline{\text{VAL CMD WD}}$			−0.4	4.0	A LOW on this output indicates the receipt of a valid command word.
15	$\overline{\text{BDCST INH}}$	20	−0.4			A LOW on this input inhibits the indication of the BROADCAST output flag.
16	TMADD1*	20	−0.4			Part of 5 bit hard-wired terminal address input.
17	TMADD3*	20	−0.4			Part of 5 bit hard-wired terminal address input.
18	XTAL					A 12 MHz parallel resonant crystal is connected between this input and ground.
19	CLOCK OUT			−1	1.0	Output of oscillator and clock driver (see text).
20	$\overline{\text{TAKE DATA}}$			−0.4	4.0	A LOW on this output indicates that received data is being shifted into the first rank register and is available at SERIAL DATA OUT. A LOW to HIGH transition transfers the contents of the first rank receiver register to the second rank register.
21	$\overline{\text{DEC RST}}$	20	−0.4			A LOW on this input (1μsec minimum) resets the decoder to its initialized state, resets COMM/$\overline{\text{DATA}}$ SYNC to a LOW, and resets VALID WORD to a HIGH.
22	DSC OUT			−0.4	4.0	LOW to HIGH transitions on this output when $\overline{\text{TAKE DATA}}$ is LOW causes causes receive cycle data shifting to occur.
23	SEND DATA			−0.4	4.0	A HIGH on this output indicates that transmit cycle data shifting is occuring
24	CLOCK IN	±1	±.001			12 MHz clock input (20pF load) (see text).
25	S/T SELECT	20	−0.4			A HIGH on this input enables off line wrap around self test. The transceiver is disabled and the encoder output is connected to the decoder input (see text).
26	FAIL-SAFE			−0.4	4.0	A HIGH on this output indicates that a transmitted message has exceeded 768 μsec, and that transmission has been terminated. FAIL-SAFE is reset by either RT ENABLE or $\overline{\text{MRST}}$.
27	RT ENABLE			−0.4	4.0	A HIGH on this output indicates receipt of a valid COMMAND word containing the correct 5 bit terminal address plus address parity. FAIL-SAFE is reset when RT ENABLE goes HIGH.
28	$\overline{\text{MODE CODE}}$			−0.4	4.0	A LOW on this output indicates the reception of a valid COMMAND word whose sub-address field contains all ONES or all ZEROES.
29	LATCH DATA 2	20	−0.4			A HIGH on this input causes parallel tri-state I/O data on D0 through D7 to appear at the output of the first rank transmit register. A LOW locks out the register inputs.
30	$\overline{\text{ENC ENABLE}}$	20	−0.4			A LOW on this input causes the transmit cycle to start at the next HIGH to LOW transition of ESC OUT

PIN FUNCTION AND LOADING TABLE (Continued)

PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
31	BROADCAST			−0.4	4.0	A HIGH on this output indicates reception of a valid COMMAND word whose address field contains all ONES, if BDCST INH is HIGH.
32	TMADD0*	20	−0.4			LSB of 5-bit hard-wired terminal address input.
33	TMADD2*	20	−0.4			Part of 5-bit hard-wired terminal address input.
34	TMADD4*	20	−0.4			MSB of 5-bit hard-wired terminal address input.
35	TMADDP*	20	−0.4			Parity bit of hard-wired terminal address. Hard-wired for odd parity.
36	CHAN SELECT	100	−2.0			A LOW on this input enables DATA SELECT 1, DATA SELECT 2, LATCH DATA 1, LATCH DATA 2, and ENC ENABLE inputs.
37	ODD PARITY			−0.36	3.6	A HIGH on this output indicates a valid check for odd parity of terminal address plus parity bits, if ENA PAR CHECK is a LOW.
38	D15	20	−0.2	−12	12	MSB of 16 bit parallel tri-state I/O.
39	D13	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
40	D11	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
41	D9	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
42	D7	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
43	D5	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
44	D3	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
45	D1	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
46	LOAD DATA 2	20	−0.4			A positive transition on this input causes the data of the D0 through D7 outputs of the first rank transmit register to be loaded into the second rank transmit register.
47	+5V					+5V power supply input.
48	$+V_{cc}$					+12V power supply input. (BUS-65101)
49	RX DATA IN					Inverted receiver input.
50	RX STROBE	40	−1.6			A LOW on this input disables the receiver output.
51	TX DATA OUT					Transmitter output.
52	CASE					Case connection.
53	DATA SELECT 2	20	−0.4			A LOW on this input causes the output of the second rank receiver register to appear on D0 through D7 of the parallel tri-state I/O.
54	DATA SELECT 1	20	−0.4			A LOW on this input causes the output of the second rank receiver register to appear on D8 through D15 of the parallel tri-state I/O.
55	ENA PAR CHECK	20	−0.4			A LOW on this input enables the function of ODD PARITY.
56	D14	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
57	D12	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
58	D10	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
59	D8	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
60	D6	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
61	D4	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
62	D2	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
63	D0	20	−0.2	−12	12	LSB of 16 bit parallel tri-state I/O.
64	LOAD DATA 1	20	−0.4			A positive transition on this input causes the data of the D8 through D15 outputs of the first rank transmit register to be loaded into the second rank transmit register.
65	GND					Power supply and logic return
66	$-V_{cc}$					-12V power supply input. (BUS-65101)
67	RX DATA IN					Receiver input.
68	TX DATA OUT					Inverted transmitter output.

NOTES: In the above table, the symbols are defined as follows:
I_{IH}=maximum input HIGH current with V_{in}=2.5 volts.
I_{IL}=maximum input LOW current with V_{in}=0.4 volts.
I_{OH}=maximum output HIGH current for V_{out}=2.5 volts minimum.
I_{OL}=maximum output LOW current for V_{out}=0.4 volts maximum.

*Indicates use of an internal pull-up resistor.

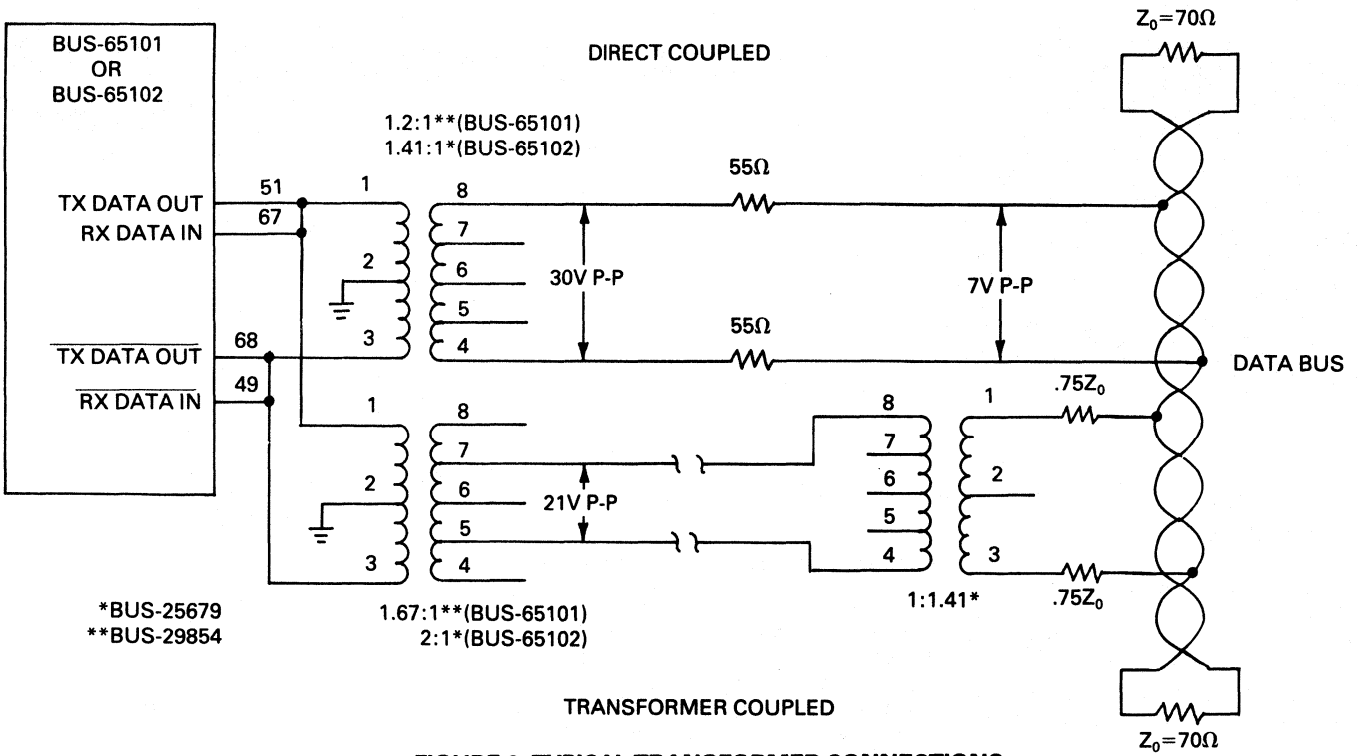
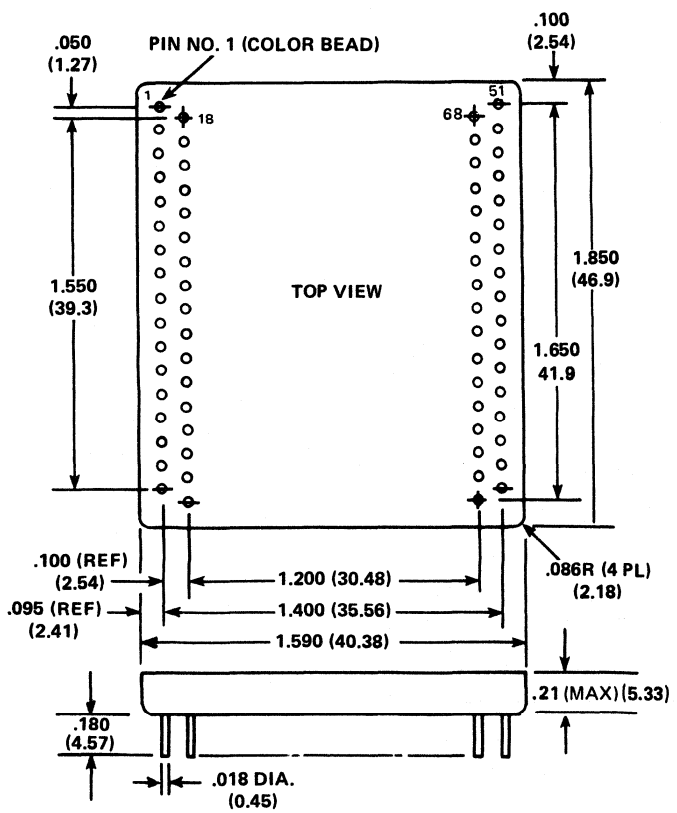


FIGURE 6. TYPICAL TRANSFORMER CONNECTIONS

MECHANICAL OUTLINE



Note: Dimensions in inches (millimeters)

ORDERING INFORMATION

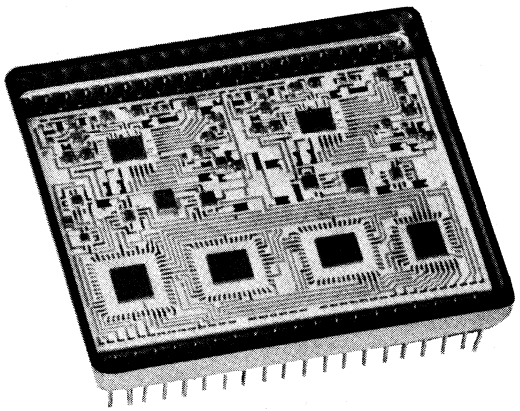
BUS-65101-883B

- MIL-STD-883 Processing:
  - 883B = Conforms to MIL-STD-883 DDC Procedures
  - Blank = Same, except burn-in is omitted
- Power Supply Option:
  - 1 = ±12 VDC
  - 2 = ±15 VDC

Note:

Use BUS-29854 transformer with BUS-65101 (direct-coupled).
Use BUS-25679 transformer with BUS-65102 (direct-coupled).

DDC
ILC DATA DEVICE CORPORATION



DUAL REDUNDANT MIL-STD-1553 RTU HYBRID

DESCRIPTION

The BUS-65122 is a dual redundant MIL-STD-1553 Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. It is fully compliant with MIL-STD-1553B and features implementation of all mode codes, wrap-around test, and terminal fail-safe time out.

The BUS-65122 contains all of the functions required to provide a terminal interface between a dual redundant MIL-STD-1553 serial data bus and a subsystem tri-state data highway. Utilizing a high level of integration, the BUS-65122 has monolithic transceivers (two) encoder/decoders (two), protocol sequencer, and 32 word FIFO.

The dual transceivers in the BUS-65122 are completely independent, including separate power and grounds, and feature low power dissipation, transmitter short circuit protection and low bit error rate (BER). The 32 word FIFO in the BUS-65122 minimizes subsystem overhead by allowing a full message to be transferred to the terminal without waiting for serial transmission, and by checking the validity of a full message before transfer to the subsystem.

FEATURES

- *SMALL SIZE*
- *LOW POWER*
- *FULL COMPLIANCE WITH MIL-STD-1553B*
- *ALL MODE CODES*
- *WRAP AROUND TEST*
- *TIME OUT*
- *32 WORD FIFO*

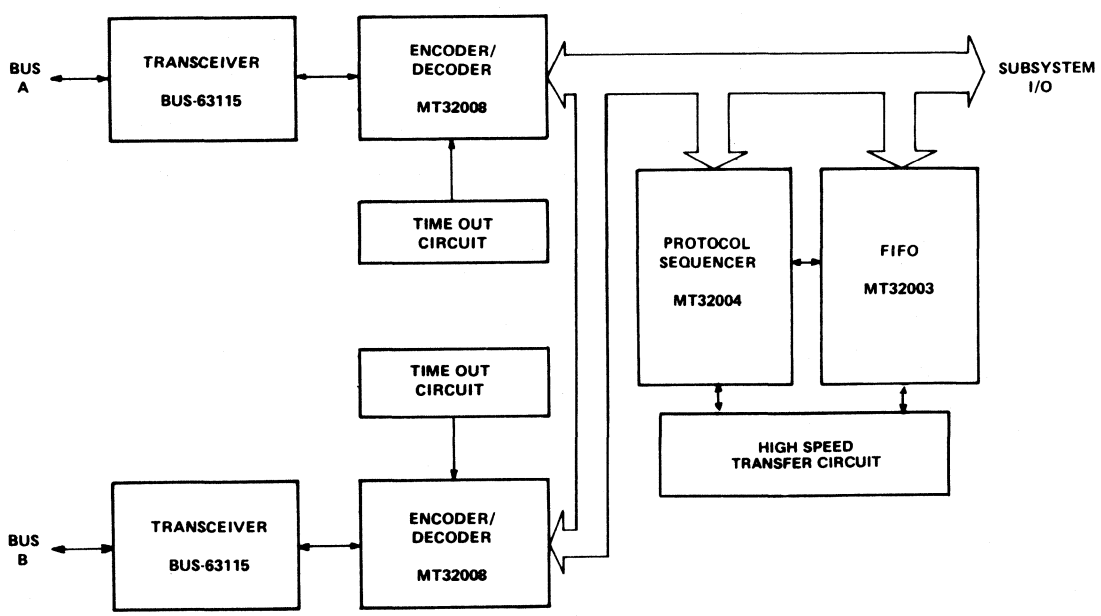


FIGURE 1. BLOCK DIAGRAM

RTU FUNCTIONS

TRANSCEIVER

The BUS-63115 monolithic Transceiver receives and transmits the phase-modulated bipolar, 1 MHz, Manchester II coded data via the BUS-25679 Transformers. The receiver section accepts this data and produces a biphase TTL signal at the complementary outputs TX DATA OUT and TX DATA OUT. These outputs are both high when idle to complement the MT32008, Encoder/Decoder. The receiver threshold is internally set at the factory for a nominal 1V p-p signal, measured on the bus. External strobe inputs are provided to turn off each of the receivers. A logic "0" applied to the RCVR STROBE will disable the appropriate receiver outputs.

The BUS-63115 transmitter sections accept biphase TTL data at the input and produce a 27 volts p-p differential signal across a 145Ω load, when measured at the transformer's output to the bus.

When TX DATA and TX DATA are either both low or both high, the transmitter presents a high impedance to the line. The BUS-63115 has a 10-15 μs built-in time-out circuit to prevent the transmitter from remaining on during idle times due to a non-complementary state at the TX DATA and TX DATA lines. The transmitter output is current limited (Not Fold Back) for protection against indefinite short circuits.

DECODER

The Decoders (half of MT32008) accept the biphase TTL signal from the transceivers, decode it and load it into the receiver shift register, where address detection as well as Manchester code, odd parity and sync detection are validated. The decoder generates ANOTHER WORD after every valid sync field plus the first three data bits. If the decoder validates the command word, its own address and proper parity, then the Command Sync (CMD SYNC, VALID WORD, and THIS RT flags will all go low at the same time. If the address is all "1"s, i.e., a broadcast command, then BDCST DETECT will go low (instead of THIS RT) with the other flags. The signals ANOTHER WORD and VALID WORD will repeat their sequence for each data word following the command word. During VALID WORD, the decoded data is shifted into the input buffer register and if VAL CMD WD REC was output by the protocol sequencer, the decoded data becomes available on the 16 bit parallel highway (T0 thru T15) for 20 microseconds.

ENCODER

The Encoders (half of MT32008) take the 16 bit parallel data, add the correct sync field and odd parity bit, and then output it to the BUS-63115 transceivers as biphase TTL complementary data. The correct redundant data bus Encoder must acknowledge that THIS RT ADDR LS matches THIS RT ADDR IP LS in order to insure that it has been selected. The Select Enable (SEL EN) signal goes high when the redundant bus addresses match. Once SEL EN is valid, data is loaded into the output buffer register by the LOAD BUFFER command. The SEND DATA signal activates the shift and load control logic. This signal initiates the actual biphase TTL transmission while also generating the BUFFER FULL status flag.

FIFO

The MT32003 is a 16 bit wide by 32 word long first-in-first-out (FIFO) memory LSI chip. This device is an integral accessory to the protocol sequencer. The memory is controlled by six control lines: Data Input Ready (DIR), Data Output Ready (DOR), Shift-In (SI), Shift-Out (SO), RESET and ENABLE.

The VAL CMD WD REC signal will reset or clear the FIFO for the next cycle. The only exception to this is when the WRAP ENABLE is made valid by the subsystem after receipt of a valid subaddress code of 11110. When enabled, no DATA STRB will be provided. Data will be held in the FIFO until the next RX command word requests this data. The controller can then compare the received data with the data originally sent out, thus providing a dynamic RT test.

PROTOCOL SEQUENCER

The MT32004 Protocol Sequencer chip interfaces directly with the MT32008 Encoder/Decoders, MT32003 FIFO and the subsystem through control lines and the 16 bit parallel three-state highway. Functionally, the Sequencer contains a FIFO status circuit, command register, last command register, built-in-test (BIT) register and status register, all of which can be accessed on the highway. It contains all the mode code control logic, receive control logic transmit control logic as well as its own time-out counter for 8, 17, 21 and 34 microsecond interval checking. The MT32004 also contains a word counter and receive count register which are compared automatically. A similar comparison is made when the command address register is compared to the status address. Finally, the Sequencer has incorporated a power on reset feature for initializing all the internal counters and registers on power up.

In the receive mode the Protocol Sequencer monitors all the decoder control lines in preparation of a new valid command word. When a valid command word is received, processing will commence.

Once a valid command word is established and the RT address is correct, VAL CMD WD REC becomes active for 500 ns. The decoded command word is available on the T0-T15 highway during this period.

The Protocol Sequencer then enables the input buffer (EN IP BUFFER) so that the data can be loaded into the command register. Bits T5 to T9 are examined to detect either a mode code or wrap around command. On all commands, except the wrap around transmit command, the FIFO is cleared. If a mode code is not detected then the least significant 5 bits contain the number of data words to be received or transmitted. The five bits are loaded into a word counter, the contents of the command register are loaded into the last command register, and the status register is cleared. Bit ten of the command register is then examined for transmit (TX) or receive (RX) mode.

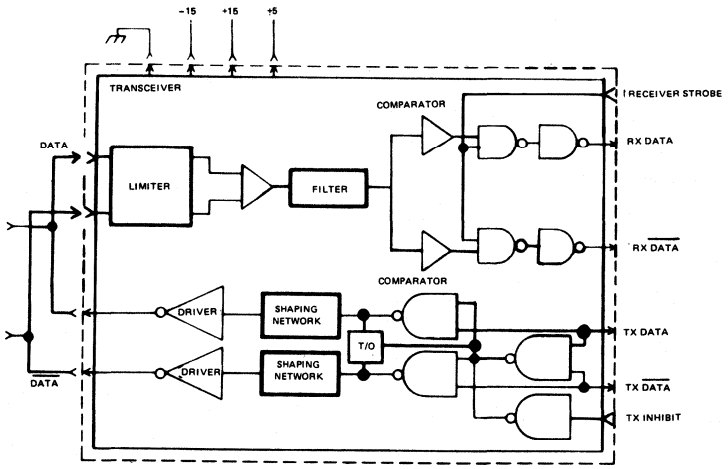


FIGURE 2. TRANSCEIVER BLOCK DIAGRAM

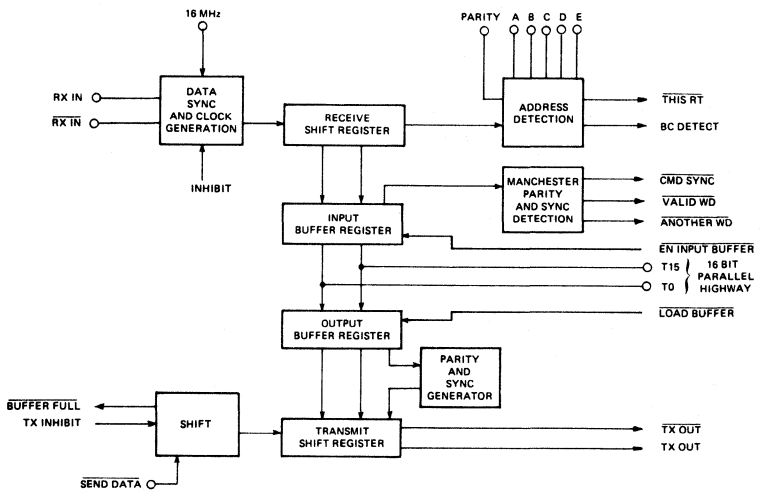


FIGURE 3. ENCODER/DECODER BLOCK DIAGRAM

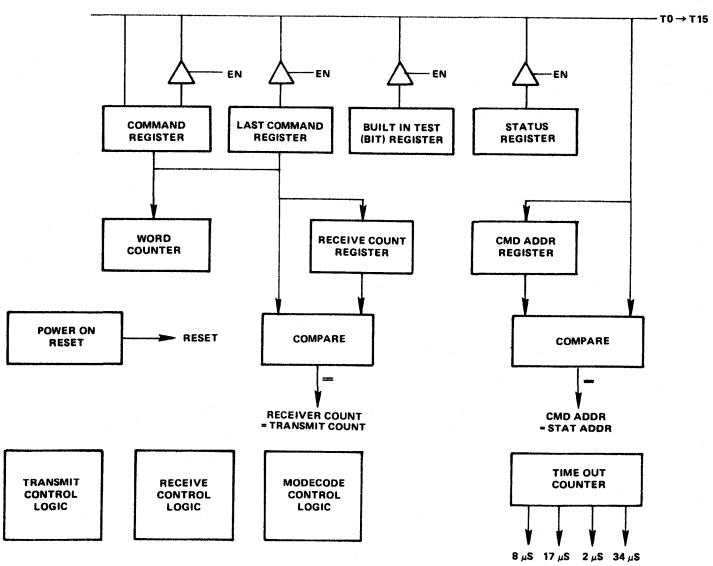


FIGURE 4. PROTOCOL SEQUENCER BLOCK DIAGRAM

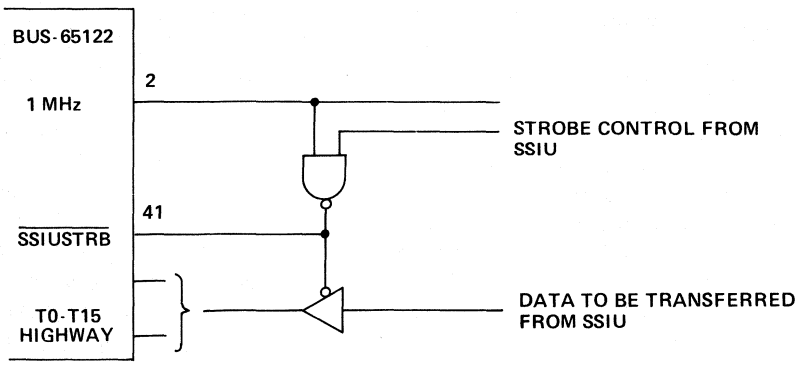


FIGURE 5. CIRCUIT FOR $\overline{\text{SSIU STRB}}$ GENERATION

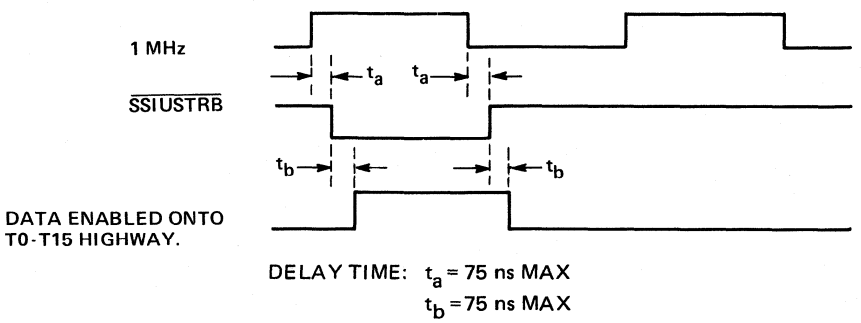


FIGURE 6. TIMING FOR $\overline{\text{SSIU STRB}}$

TRANSFER FORMATS

RT TO BUS CONTROL TRANSFER

A broadcast address received with a valid command word in the transmit (TX) mode is not valid. If it occurs, the message error bit and broadcast command received bit in the status register will be set (bits T10 and T4) and the sequence terminated.

If the command is a valid TX then the status register is enabled onto the T0-T15 highway and the sequence halts for approximately 8 μs to see if another valid word has been detected (which is a fault condition). If another valid word is detected ($\overline{\text{ANOTHER WORD}}$) then the message error bit in the status register is set and the sequence is terminated. If $\overline{\text{ANOTHER WORD}}$ is not detected, the contents of the status registers are loaded into the output buffer of MT32008 via load buffer for 125 ns and simultaneously the $\overline{\text{SEND DATA}}$ signal is valid for 250 ns. At the end of the $\overline{\text{SEND DATA}}$ pulse the transmit sequence will begin sending out the status word.

Since the $\overline{\text{SEND DATA}}$ output pulse is used internally to transfer the status word to the encoder, it may also be used to gate a subsystem status bit, such as $\overline{\text{SUBSYSTEM BUSY}}$ or $\overline{\text{SUBSYSTEM FLAG}}$, onto the tri-state highway for subsequent transmission. The response time measured from the middle of the last received bit of the TX command to middle of the first bit of the status word sync is approximately 10.8 μs.

While the status word transmission is taking place the terminal flag (TF) latch is cleared, and the contents of the command register are transferred to the subsystem interface unit (SSIU). The contents of the command register are enabled onto the highway during the 8.5 μs command strobes ($\overline{\text{CMD STRB}}$) period.

If the $\overline{\text{SUBSYSTEM BUSY}}$ signal is activated by the subsystem, the busy bit of the status register will be set. After the $\overline{\text{CMD STRB}}$ period the sequence will terminate so no data will be transmitted.

When the $\overline{\text{CMD STRB}}$ period ends the sequencer will halt until the subsystem enables the first data word onto the 16 bit Highway by activating the $\overline{\text{SSIU STRB}}$. This data is loaded into the output buffer and the word counter is decremented by one. The SSIU continues transferring its 16 bit parallel words to the MT32004 by enabling the data onto the highway and sending an $\overline{\text{SSIU STRB}}$.

Figure 5 shows the recommended circuit for generating $\overline{\text{SSIU STRB}}$. The circuit is required because $\overline{\text{SSIU STRB}}$ must be synchronized with the positive phase of the 1 MHz clock.

The first data word is loaded directly into the output buffer ready to be transmitted. While the first word is being transmitted the BUFFER FULL signal will become not valid, allowing the second data word to be shifted out of the FIFO and loaded into the output buffer ready for transmission. This occurs when the SSIU STRB is not valid so that the sequencer can take control of the 16 bit highway to transfer the data from the FIFO. The subsystem (SSIU) must only enable its three-state interface during the SSIU STRB valid time. This data shifting sequence is repeated as the word counter is decremented by one for every SSIU STRB until the word counter equals zero. When the word counter equals zero the shift in signals to the FIFO are disabled and the sequence is terminated.

If another SSIU STRB occurs within 17 μs after the word counter equals zero, Bit 1 of the built-in-test (BIT) register is set and the sequence is terminated.

BUS CONTROLLER TO RT TRANSFER

If a valid RX command word is received, bit T10 of the command register is set to "0" and the Protocol Sequencer is ready to receive data. Data being received must be continuous with no interword gaps. The first word received immediately after the command word is checked for no interword gap and that it is a valid data word. If it turns out to be another command word, then an RT to RT command has been issued (Refer to RT to RT transfer).

If an intermessage gap is detected on the incoming data words, the message error bit in the status register is set and the sequence will terminate.

If there are fewer or more valid data words (detected by counting ANOTHER WORD received than were indicated in the command word, the message error bit in the status register is set and the sequence is terminated.

When the complete message is contained in the FIFO and a broadcast command has not been detected, the contents of the status register are enabled onto the highway and the (status word) transmit sequence is initiated. The terminal flag (TF) is cleared during transmission of the status word.

If the command was a broadcast then the transmit status sequence is bypassed and the broadcast received bit in the status register is set. The CMD STRB output is activated for 8.5 μs so that SSIU transfer may take place. When the CMD STRB transfer ends, the FIFO is enabled so that its contents can be transferred onto the highway by the DATA STRB. The SSIU may stop the normal data transfer by holding DATA STRB low. When the DATA STRB is released by the SSIU the next word is shifted to the front of the FIFO. This transfer cycle is repeated until the FIFO is emptied.

RT TO RT TRANSFER

The bus controller initiates an RT to RT transfer by sending a receive command word to RTU #1 followed by a transmit command to RTU #2. The RTU #2 will reply with a status word followed by the requested contiguous data words. RTU #2 will initiate the receive sequence on receipt of a valid receive command word with its own RT address and will monitor the RTU #2 TX command for validity and no interword gap. If it meets these two requirements, then the contents of RTU #1 input buffer (the transmit command word for RTU #2) will be enabled onto the 16 bit highway. If a valid TX Command Word is not received contiguously then the message error bit in the status register will be set and the sequence terminated.

When valid, the most significant 5 bits (the RTU #2 address) are loaded into the 5 bit command address register and the sequence on RTU #1 will halt for 20.5 μs. If during this time a valid data word or command word for another RT occurs, this would be a fault condition and the message error (ME) bit in the status register will be set and the sequence terminated. A valid command word received with RTU #1 address will override the complete sequence and reset the sequencer. The sequencer will wait 14 μs and if RTU #2 has not transmitted its status word by this time (whose contents are now in RTU #1's input buffer) the ME bit in the status register will be set and the sequence will terminate.

If there is no fault condition, the RTU #2 address on the highway is compared with the contents of the command address register. If they are not the same, then this is a fault condition which sets the ME bit and the sequence is terminated. If they do match, the sequence will continue.

WRAP AROUND

The wrap around test is initiated by receipt of a valid RX command word containing the code 11110 in the subsystem address (bits T5 thru T9). The contents of the word counter are loaded into the receive count register. The WRAP ENABLE input must be set high for the Protocol Sequencer to perform this function.

The wrap around test will perform like a standard Bus Control to RT transfer, except the sequence terminates after the status word and no DATA STRB's are provided since no transfers to SSIU will be made. The received data will remain stored in the FIFO.

The bus controller will send a TX command word and the sequencer will perform as a RT to Bus Controller, but the FIFO is not cleared by this TX command word. While the status word is being transmitted the contents of the receive count register are compared to the contents of the word counter. If the contents are not equal the ME bit in the status register is set and the sequence will terminate. If they are the same the FIFO is enabled and the contents are transmitted one word at a time.

MODE CODE IMPLEMENTATION

When a valid command word containing a mode code is received, the FIFO is cleared and the mode code sequence is initiated. In all mode codes, except transmit last command, the contents of the command register are loaded into the last command register.

DYNAMIC BUS CONTROL (CODE 00000) T/R =1

This mode code can be generated from an external CPU which is capable of performing bus control. When VAL CMD WD REC is present the SSIU can set DYNAMIC BUS ACCEPTANCE which will set bit T1 of the status word, thereby, accepting the bus control function.

SYNCHRONIZE WITHOUT DATA WORD (CODE 00001) T/R =1

The T/R bit of the RX command word must be set to a one for this mode code. If it is set to a zero then the ME bit in the status register is set and the sequence terminated. This same fault condition will result if it is set to a zero and a broadcast command is detected.

At the end of status word transmission all zeros are enabled onto the highway and a 250 ns active low pulse is applied to the synchronize output. (The TF latch and Status register are cleared upon receipt of a valid command).

TRANSMIT STATUS WORD (CODE 00010) T/R = 1

If a VAL CMD WD REC is received, the status register is enabled onto the highway (but is not cleared) and transmitted. The TF latch is cleared after the transmit sequence and then the sequence is terminated.

INITIATE SELF TEST (CODE 00011) T/R = 1

This mode code has an error checking and status word transmission sequence the same as the "synchronize without data word" previously described.

At the same time as SEND DATA a 500 ns BITE OUT pulse is sent to the external time-out circuits. The correct time-out circuit is enabled by the active MT32008 SEL EN signal. After a period of 672 μs to 800 μs the signal BITE IN should time-out and return high. If this occurs too early or too late the least significant bit of the built-in-test register is set to a "1". The sequence then terminates.

TRANSMITTER SHUTDOWN (CODE 00100) T/R = 1

At the end of the error checking and status word transmission sequence THIS RT ADDR IP on the bi-directional address highway are examined. If it was set to 00 then it is reset to 01. If it was set to 01 then it is reset to 00. This disables the transmitter of the addressed encoder by generating a SEL TX DIS signal. Gating the correct encoder is handled by the SEL EN signal, which is generated by comparing this RT ADDR to THIS RT ADDR IP after it has been reset.

OVERRIDE TRANSMITTER SHUTDOWN (CODE 00101) T/R = 1

This command performs the same sequence as in transmitter shutdown, but the pulse is applied to signal SEL TX EN. This will re-enable the redundant bus. The sequence will then terminate.

INHIBIT TERMINAL FLAG BIT (CODE 00110) T/R = 1

The TF bit is used to detect any power resets or interruptions to the VDD power (+5 Volts). Once latched, the Protocol Sequencer must generate "CLEAR TF" (internal to chip). The TF bit is not reset until "CLEAR STATUS" (internal to chip) occurs. If the "CLEAR STATUS" occurs while the latch is still set then the status bit will return back to the set condition when "CLEAR STATUS" is removed. With a valid inhibit TF bit command word, the standard error checking and status word transmission will take place and the sequence will then terminate. As the terminal flag (TF) bit of the status register is used to detect power on, it is not inhibited (it has an embedded latch).

OVERRIDE INHIBIT TERMINAL FLAG BIT (CODE 00111) T/R = 1

The error checking and status word transmission sequence is initiated and the sequence is then terminated. Override inhibit TF is not performed due to "INHIBIT TF" (internal to chip) not operating.

RESET REMOTE TERMINAL (CODE 01000) T/R = 1

The standard error checking and status word transmission sequence starts. After receipt of VAL CMD WD REC a reset signal will clear the FIFO, and reset the MT32008 Encoder/Decoder and MT32004 Protocol Sequencer.

RESERVED MODE CODES (CODES 01001 TO 01111) T/R = 1

A valid reserved mode code will enable, but not clear, the status register and set the ME bit. The status word is transmitted, the TF latch is cleared and the sequence then terminates. If it was a broadcast command, then the broadcast received bit of the status register is set and the sequence terminates without transmitting the status.

TRANSMIT VECTOR WORD (CODE 10000) T/R = 1

The T/R bit must be a one in order to clear the status register. A zero T/R bit will set the ME bit in the status register and the sequence will terminate. If a broadcast command is received, the ME bit and the broadcast received bit of the status register are set and the sequence is terminated.

The vector word transmit sequence is initiated by SEND DATA and LOAD BUFFER. The TF latch is then cleared and the sequence will wait until the status register is being transmitted via signal BUFFER FULL.

The EN VECTOR WORD output signal becomes valid for 250 ns in which time the SSIU vector word must be enabled onto the highway. The sequence then terminates. EN VECTOR WORD signal returns high until the next command word is received.

SYNCHRONIZE WITH DATA WORD (CODE 10001) T/R = 0

If T/R bit is set to a one, the ME bit in the status register is set and the sequence will terminate. If the T/R bit is set to zero the status register is cleared. If a broadcast command is received, the broadcast received bit of the status register is set.

The RX command word is checked to insure a contiguous data word follows. If it doesn't, the ME bit of the status register is set and the sequence terminates. When a valid data word is received it is stored in the FIFO and a further check is made to ensure that only one data word is received via signal ANOTHER WORD. If another word is detected, the ME bit is set and the sequence is terminated.

The "synchronize with data word" enables the status register onto the highway for transmission. The TF latch is then cleared, the contents of the FIFO are enabled onto the highway and a 250 ns pulse is simultaneously applied to the SYNCHRONIZE output.

TRANSMIT LAST COMMAND (CODE 10010) T/R = 1

The mode code error checking sequence is the same as "transmit Vector Word". It differs by enabling the contents of the last command registers onto the 16 bit highway to be transmitted. Also, the status register is not cleared before transmission, and the TF latch is cleared after the status word transmission.

TRANSMIT BIT WORD (CODE 10011) T/R = 1

This mode code is error checked and sequenced in the same way as "Transmit Vector Word", but the contents of the built-in-test register are enabled onto the highway for transmission. The BIT word register is then cleared and the sequence terminated.

SELECTED TRANSMITTER SHUTDOWN (CODE 10100) T/R = 0

(U.S. Air Force has cancelled the use of this code). This mode code is error checked and sequenced in the same manner as "Synchronize with Data Word".

If a valid data word is received, it is stored in the FIFO. The least significant 2 bits (T0 & T1) of the data word are compared to THIS RT ADDRESS of the receiving MT-32008. If they are the same this is a fault condition and the ME bit is set. The status register is then transmitted.

If the bits are not the same, then the two least significant bits of the FIFO contains THIS RT ADDRESS of the MT32008 to be shut down.

The sequencer will then change the THIS RT ADDR IP signals to the contents of T0 and T1 (i.e., SEL EN becomes valid for the MT32008 to be shut down), while a pulse on signal SEL TX DIS terminates the sequence.

OVERRIDE SELECTED TRANSMITTER SHUTDOWN (CODE 10101) T/R = 0

Same as above except that a pulse is applied to signal SEL TX EN.

RESERVED MODE CODES (CODES 10110 TO 11111)

If a valid reserved mode code is received then the ME bit of the status register is set. The status register is then enabled, but not cleared, and then transmitted. The TF latch is cleared and the sequence terminates. If it is a broadcast command, then the broadcast received bit of the status register is set and the sequence terminates without transmitting the status.

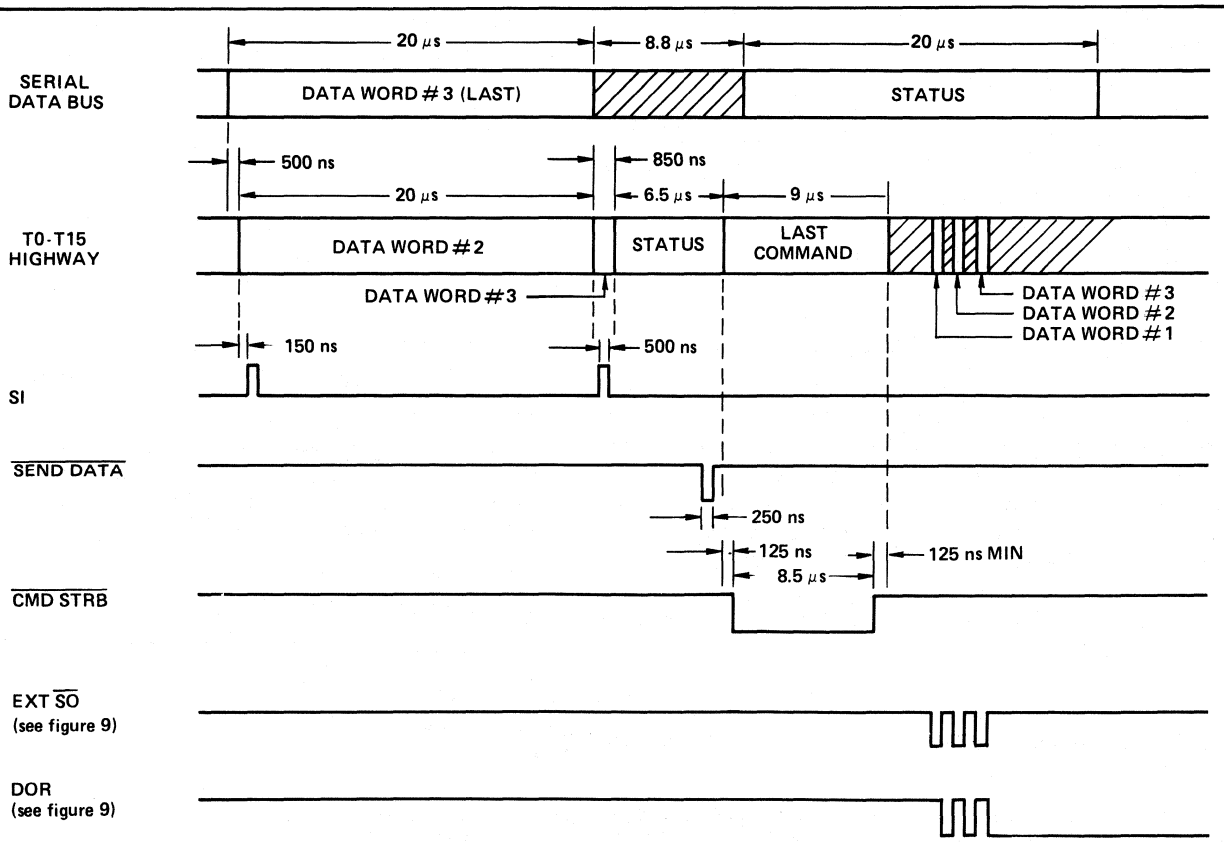


FIGURE 7. RECEIVE MODE TIMING (3 DATA WORDS)

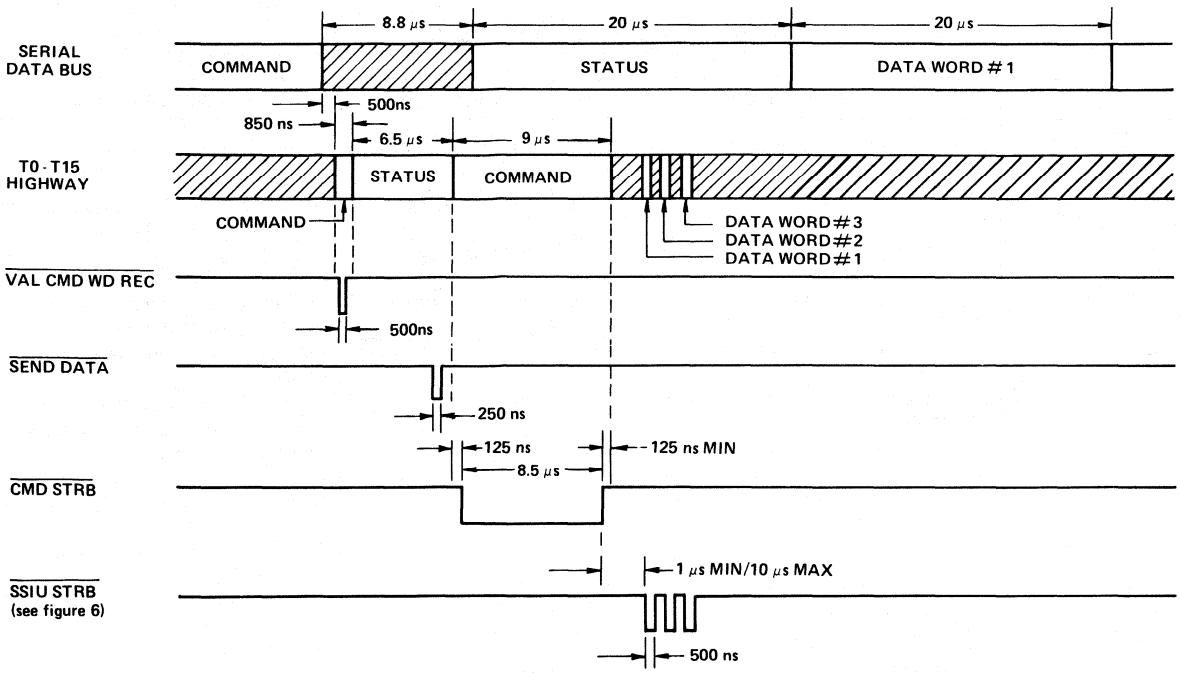


FIGURE 8. TRANSMIT MODE TIMING (3 DATA WORDS)

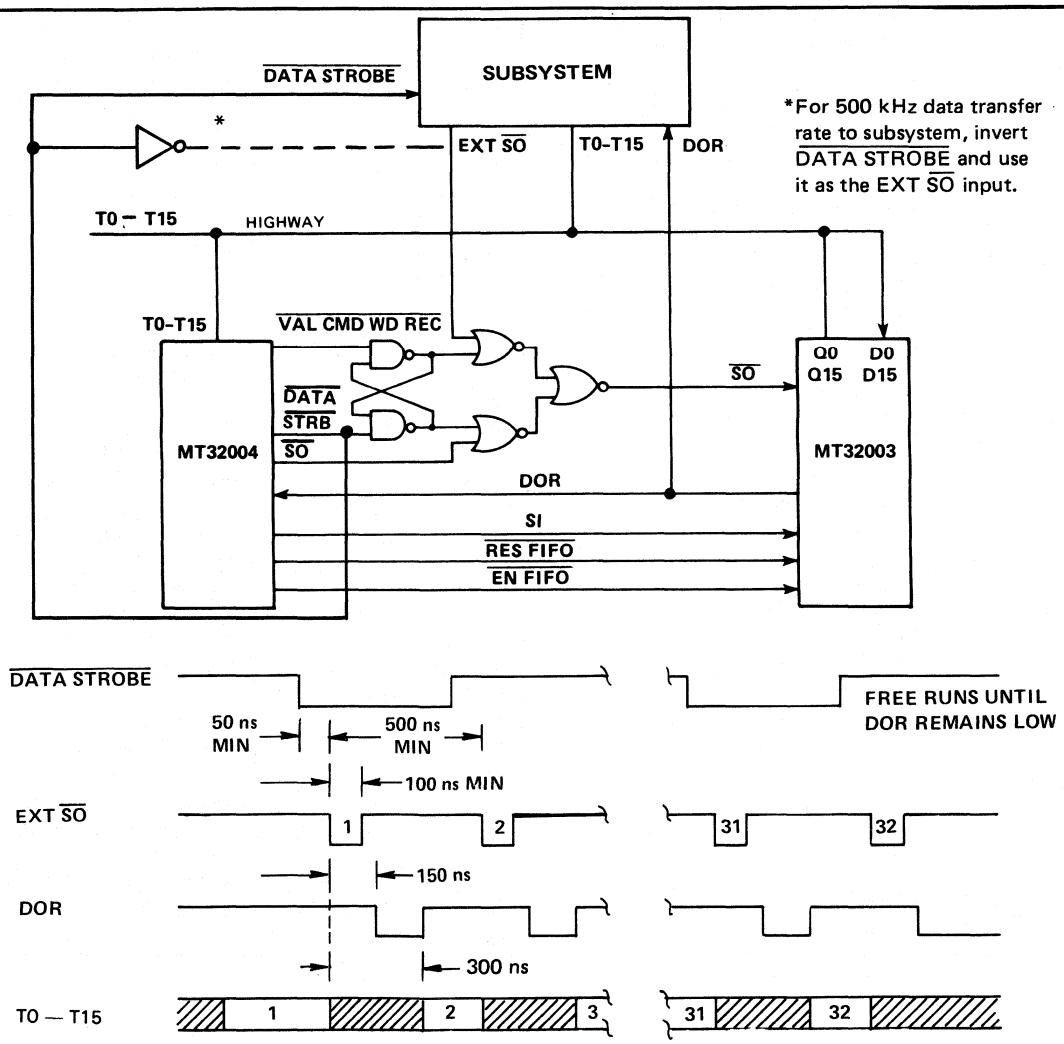


FIGURE 9. HIGH SPEED TRANSFER CIRCUIT

Pin Function Table

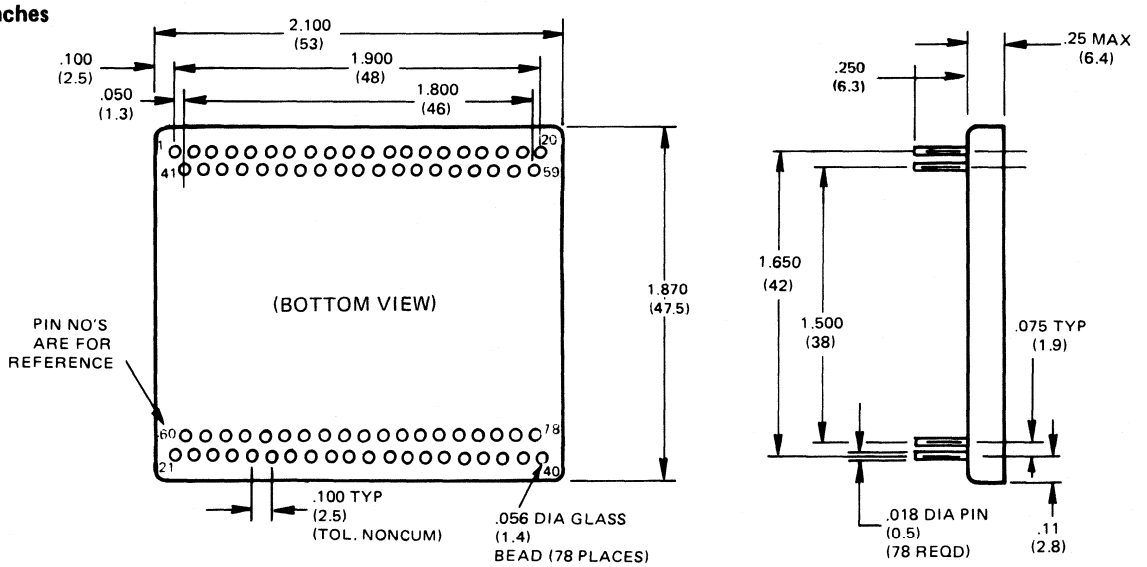
PIN	FUNCTION	DESCRIPTION	PIN	FUNCTION	DESCRIPTION
1	VAL CMD WD REC	Output pulse identifies valid command word received.	39	DATA SYNC IN-B	Connect to +5V supply.
2	1 MHZ OUT	1MHz clock output.	40	B GND	Ground for bus B circuits.
3	DATA STROBE	Output pulse that identifies terminal data is ready to be transferred to subsystem.	41	SSIU STROBE	Input pulse identifies subsystem data is enabled on the highway.
4	C GND	Ground for non-redundant circuits.	42	CMD STROBE	Output pulse identifies command word is enabled on the highway.
5	SYNCHRONIZE	Output pulse identifies synchronize (mode code) command received.	43	EN VECT WORD	Output pulse enables subsystem vector word onto the highway.
6	SUBSYSTEM BUSY	Low input level inhibits transfer of data onto the highway.	44	SUBSYSTEM FLAG	Low input level identifies subsystem fault condition.
7	DYNAMIC BUS ACC	Low input level identifies subsystem acceptance of bus control.	45	+5V C	+5VDC to non-redundant circuits.
8	RESET	Low input level resets the encoder/decoder. Must be wired - OR connection with open collector drive and resistor pullup.	46	SERVICE REQ	Low input level identifies subsystem request for service.
			47	WRAP ENABLE	High input level causes receipt of subsystem address 11110 to initiate wrap-around test.
9	ADDR D	Terminal address bit D (hard wired).	48	ADDR E	Terminal address bit E (MSB) (hard wired).
10	ADDR B	Terminal address bit B (hard wired).	49	ADDR C	Terminal address bit C (hard wired).
11	ADDR P	Address parity (hard wired).	50	ADDR A	Terminal address bit A (LSB) (hard wired).
12	T0	Bit 0 (LSB) of 16 bit tri-state data highway.	51	16 MHZ IN	16 MHz clock input. Duty cycle is 40% min/60%max. Frequency tolerance is ±0.01%. TTL compatible logic levels.
13	T2	Bit 2 of 16 bit tri-state data highway.			
14	T4	Bit 4 of 16 bit tri-state data highway.			
15	T6	Bit 6 of 16 bit tri-state data highway.			
16	T8	Bit 8 of 16 bit tri-state data highway.	52	T1	Bit 1 of 16 bit tri-state data highway.
17	T10	Bit 10 of 16 bit tri-state data highway.	53	T3	Bit 3 of 16 bit tri-state data highway.
18	T12	Bit 12 of 16 bit tri-state data highway.	54	T5	Bit 5 of 16 bit tri-state data highway.
19	T14	Bit 14 of 16 bit tri-state data highway.	55	T7	Bit 7 of 16 bit tri-state data highway.
20	DOR	High output level identifies that next terminal data word is enabled on the highway.	56	T9	Bit 9 of 16 bit tri-state data highway.
			57	T11	Bit 11 of 16 bit tri-state data highway.
21	SEND DATA	Output pulse indicates that the status word is on the tri-state data highway, and is being transferred to the encoder for transmission.	58	T13	Bit 13 of 16 bit tri-state data highway.
			59	T15	Bit 15 (MSB) of 16 bit tri-state data highway.
			60	TX DATA OUT — A	Transmitter output to bus A transformer.
22	NC	No connection.	61	TX DATA OUT — A	Transmitter inverted output to bus A transformer.
23	NC	No connection.			
24	RX DATA OUT—A	Factory test point.	62	+15V — A	+15VDC for bus A circuits.
25	RX DATA OUT—A	Factory test point.	63	EXT SO	Input pulse causes next terminal data word to be enabled onto the highway.
26	NC	No connection.	64	+5V — A	+5VDC for bus A circuits.
27	NC	No connection.	65	-15V — A	-15VDC for bus A circuits.
28	NC	No connection.	66	RX DATA IN — A	Receiver inverted input from bus A transformer.
29	RCVR STROBE-A	Low input level disables receiver on bus A.	67	RX DATA IN — A	Receiver input from bus A transformer.
30	RX/TX-A	Connect to +5V supply.	68	DATA SYNC IN — A	Connect to +5V supply.
31	NC	No connection.	69	A GND	Ground for bus A circuits.
32	NC	No connection.	70	TX DATA OUT — B	Transmitter output to bus B transformer.
33	NC	No connection.	71	TX DATA OUT — B	Transmitter inverted output to bus B transformer.
34	SI	Positive output pulse latches decoded data into FIFO.	72	+15V — B	+15VDC for bus B circuits.
			73	+5V — B	+5VDC for bus B circuits.
35	NC	No connection.	74	-15V — B	-15VDC for bus B circuits.
36	BITE IN	Low output during self-test indicates Fail-Safe Timeout interval.	75	RX DATA IN — B	Receiver inverted input from bus B transformer.
			76	RX DATA IN — B	Receiver input from bus B transformer.
37	RX DATA OUT - B	Factory test point.	77	RCVR STROBE — B	Low input level disables receiver on bus B.
38	RX DATA OUT - B	Factory test point.	78	RX/TX — B	Connect to +5V supply.

SPECIFICATIONS – Values at nominal power supply voltages over operating range.

PARAMETER	UNITS	VALUE						
Logic								
V_{IH} high level input voltage	V	2.4 min						
V_{IL} low level input voltage	V			0.8 max				
V_{OH} high level output voltage	V	4.5 min						
V_{OL} low level output voltage	V			0.4 max				
I_{OH} high level output current	µA	400 min						
I_{OH} low level output current	mA	−1.6 min						
I_{IL} low level input current	mA			1.6 max				
I_{IH} high level input current	µA			10 max				
C_{IN} input capacitance	pf			10 max				
C_{OUT} output capacitance	pf			10 max				
Temperature Range								
Operating (Case)	°C	−55 to +125						
Storage	°C	−55 to +125						
Power Supplies								
Voltage	V	+15		−15		+5		
Tolerance	%	5%		5%		10%		
Redundant DC		A	B	A	B	A	B	C
Current (MAX) Idle	mA	65	65	65	65	60	60	50
25% transmit	mA	65	65	150	150	60	60	50
100% transmit	mA	65	65	290	290	60	60	50

MECHANICAL OUTLINE

Dimensions in inches (millimeters)



ORDERING INFORMATION

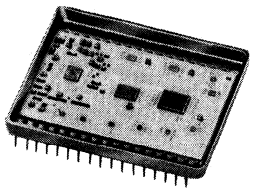
BUS-65122-883B

Power Supply Option:

2 = ±15VDC
3 = ±12VDC

DDC
ILC DATA DEVICE CORPORATION

UNIVERSAL MACAIR/1553 DUMB RTU HYBRID



DESCRIPTION

The BUS-65201 Universal MACAIR/1553 Dumb Remote Terminal Unit (RTU) consists of a transceiver, and encoder/decoder, control logic, dual rank I/O registers and internal clock oscillator packaged in a 1.6" x 1.9" hermetic hybrid. It provides all the functions required to interface between a MACAIR (sinusoidal) or MIL-STD-1553 (trapezoidal) serial MUX data bus and a subsystem parallel 3-state data highway. Utilizing several DDC custom monolithic ICs, the BUS-65201 provides sufficient handshaking, control and data lines to permit versatile operation as a remote terminal, a bus controller or a bus monitor, in either single or dual redundant data bus configurations.

As a transmitter, the BUS-65201 accepts 8 bit or 16 bit parallel data from the subsystem, and outputs serial Manchester II coded Command, Status or Data words, under subsystem control. As a receiver, it accepts serial MIL-STD-1553 or MACAIR transmissions and transfers all Command, Status and Data words to the 8 bit or 16 bit data highway, under subsystem control. The BUS-65201 also provides flags to the subsystem when Broadcast, Mode Code, and Own Address (with parity) commands are decoded.

The BUS-65201 contains a terminal fail-safe timeout circuit which flags message lengths exceeding 768 microseconds, and terminates serial data transmission. Wraparound self-test is initiated by a control line which causes the encoder serial output to be connected to the decoder input. The BUS-65201 provides a serial output of decoded words, thus allowing Command word look-ahead, for the fastest terminal response.

FEATURES

- *INCLUDES:*
  - *UNIVERSAL TRANSCEIVER*
  - *ENCODER/DECODER*
  - *DUAL RANK I/O REGISTERS*
  - *FAIL-SAFE TIMER*
  - *CLOCK OSCILLATOR*
- *SMALL 1.6" x 1.9" HYBRID*
- *PROVIDES FLAGS FOR:*
  - *OWN ADDRESS (WITH PARITY)*
  - *MODE CODE*
  - *BROADCAST*
  - *TIME OUT*
  - *VALID WORD*
  - *SYNC TYPE*
- *16 BIT OR 8 BIT 3-STATE PARALLEL I/O AND SERIAL OUT*
- *WRAPAROUND BUILT-IN TEST*
- *SIMPLE CONTROLS FOR SINGLE OR DUAL REDUNDANT DATA BUS CONFIGURATIONS*

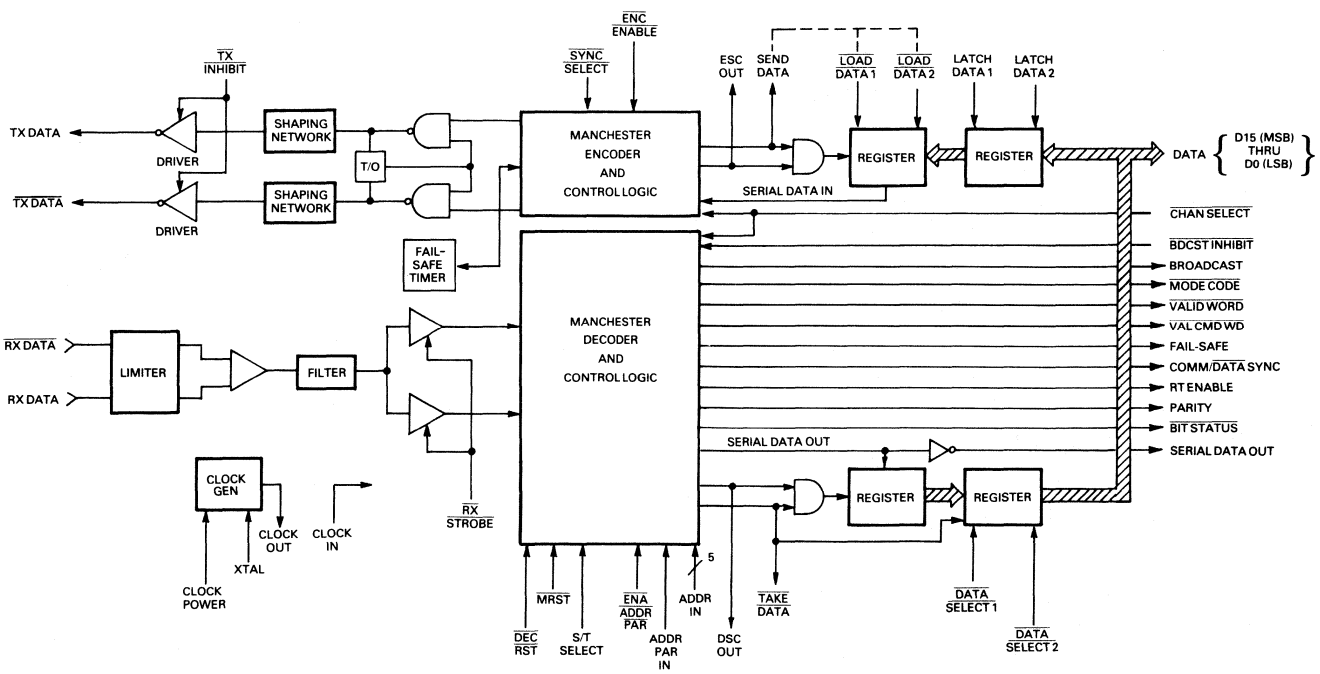


FIGURE 1. BUS-65201 BLOCK DIAGRAM

SPECIFICATIONS – Values at nominal power supply voltages.

PARAMETER	UNITS	VALUE
RECEIVER		
Differential Input Impedance (DC to 1MHz)	KΩ	5 min
Differential Input Voltage	V_{p-p}	40 max
Input Threshold (Direct Coupled)	V_{p-p}	0.5 min
CMRR (DC to 2MHz)	dB	40 min
CMV (DC to 2MHz)	V	±10 min
RX STROBE Characteristics	TTL Loads	1 typ
TRANSMITTER		
Differential Output Voltage		
Direct Coupled (across 145Ω Load)	V_{p-p}	30 typ
Transformer Coupled (at Stub)	V_{p-p}	21 typ
Sinusoidal Output Rise and Fall Times	ns	250 typ
Output Noise	mV_{p-p}	10 max
TX INHIBIT Characteristics	TTL Loads	1 typ
LOGIC		
I_{IH}, I_{IL}, I_{OH}, I_{OL}		See pin function & loading table.
V_{OH}	V	2.5 min
V_{OL}	V	0.4 max
V_{IH}	V	2.0 min
V_{IL}	V	0.7 max
CLOCK		
V_{OHC} (Internal Clock)	V	Supply −0.3V min
V_{OLC} (Internal Clock)	V	Ground +0.3V max
V_{IHC} (External Clock)	V	Supply −0.5V min
V_{ILC} (External Clock)	V	Ground +0.5V max
POWER SUPPLIES		
+5V OSC/CLOCK Supply		
Voltage Tolerance	%	±10
Current Drain	mA	8 typ; 13 max
+5V Logic Supply		
Voltage Tolerance	%	±10
Current Drain	mA	250 max
$+V_{cc}$ and $-V_{cc}$ Supply		
Voltage Tolerance	V	12 to 15
Current Drain		
Idle	mA	75 max
25% Transmit	mA	105 max
100% Transmit	mA	190 max
TEMPERATURE RANGE (Case)		
Operating	°C	−55 to +125
Storage	°C	−55 to +135
PHYSICAL		
Size	in. (mm)	1.6x1.9x0.21 (40.4x46.9x5.3)
Weight	oz (gm)	1 max (28)

GENERAL

As shown in the block diagram of Figure 1, the BUS-65201 provides all functions required to implement a Dumb Remote Terminal Unit (RTU). It is designed for the greatest flexibility and ease of use. BUS-65201 can be operated with either an internal or external clock. Simple control lines are provided to interface with either an 8 bit or 16 bit parallel data highway, in either single channel or dual redundant configurations. Control lines are available to implement either on line or off line wraparound built-in test. BUS-65201 can be configured to perform a parity check on its hard-wired terminal address. It provides numerous output flags to simplify the user interface. These flags indicate various decoded messages, as well as the results of error checks. Sync selection, along with the flexible controls, allows the BUS-65201 to operate as a Bus Controller as well as a Remote Terminal.

INTERNAL OR EXTERNAL CLOCK

BUS-65201 may be operated with either its internal clock or an external clock. Internal clock operation requires that a 12 MHz parallel-resonant fundamental-mode crystal, such as MIL-C-3098/42 TYPE CR64/U, be connected between pin 18 (XTAL) and ground. In addition, +5 volt power must be connected to pin 2 (OSC/CLOCK POWER), and CLOCK OUT (pin 19) must be connected to CLOCK IN (pin 24).

For external clock operation, no connection is made to pin 2 (OSC/CLOCK POWER), and the external clock is applied to pin 24 (CLOCK IN). Pin 19 (CLOCK OUT) is not connected. The external clock must be capable of driving a load of 20 picofarads to within 0.5 volts of the +5 volt power supply and to within 0.5 volts of ground. Standard TTL voltage levels will not work properly. It must have a rise time and fall time of less than 10 nanoseconds. For compliance with MIL-STD-1553 and MACAIR specifications, the external clock frequency must be 12 MHz.

8-BIT OR 16-BIT INTERFACE

The BUS-65201 may be configured to interface with either 8 bit or 16 bit parallel data highways. For 16 bit operation, the 16 data lines (D15 through D0) are used directly. LATCH DATA 1 and LATCH DATA 2 are tied together, as are DATA SELECT 1 and DATA SELECT 2. This allows data transfer in 16 bit bytes.

For 8 bit parallel data highways, the 16 data lines must be tied together in eight pairs (D15 to D7, D8 to D0, etc.) The two LATCH DATA and DATA SELECT signals are used independently. This allows transfer in two 8 bit bytes.

ADDRESS WITH PARITY

The BUS-65201 provides five lines for hard-wired terminal address. Internal pull-up resistors are provided on these lines, so logic "1" lines may be left open-circuited. Logic "0" lines must be grounded. The BUS-65201 may be configured to check the parity of these five address lines. This function can be selected by using the ENA PAR CHECK line. The address parity line (TMADDP) is hard-wired for odd address parity if the function is used. The ODD PARITY output flag indicates a valid check for odd parity of the six address lines.

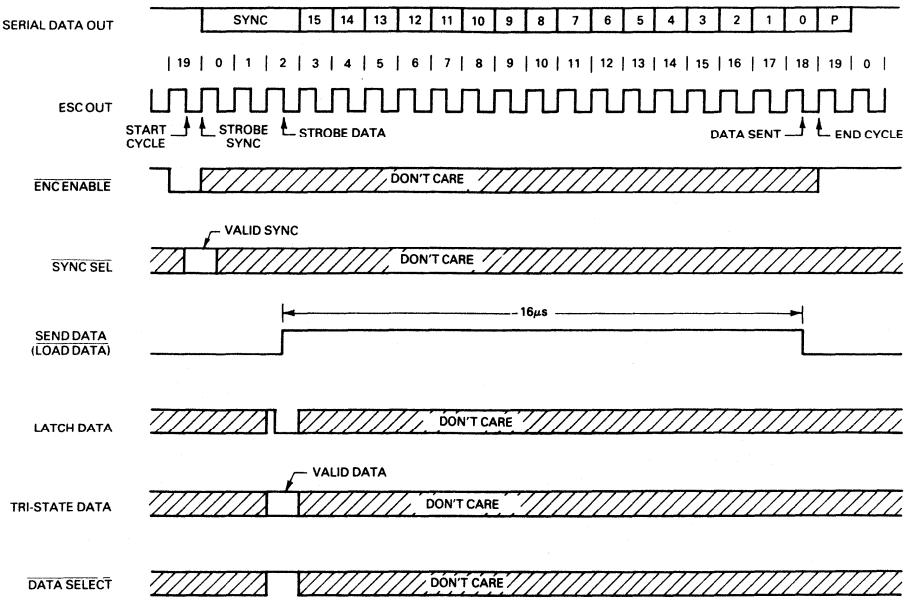


FIGURE 2. TRANSMIT MODE TIMING

DUAL REDUNDANT OPERATION

The BUS-65201 may be used in a dual redundant configuration with a minimum of additional circuitry. A CHAN SELECT signal is provided which simultaneously disables the LATCH DATA, DATA SELECT, and ENC ENABLE lines of the BUS-65201. Therefore, CHAN SELECT can be used to multiplex a single set of LATCH DATA, DATA SELECT and ENC ENABLE control signals between two BUS-65201 units, which have these signals tied together in parallel.

WRAPAROUND BUILT-IN TEST

The BUS-65201 may be configured to implement either on line or off line wrap around built-in test. By enabling the receiver with RX STROBE during a normal transmission, the encoded word will be fed back into the decoder by the receiver. In this on line wrap around mode of operation, the BUS-65201 compares each decoded word that is fed back with the original word that was encoded. The BIT STATUS output flag indicates when the two words are not the same.

Care must be taken when using this on line wrap around test technique because an outgoing status word will be interpreted by the decoder as a new command word. Since the status word has the correct address and the same sync as a command word, the BUS-65201 will set RT ENABLE and VAL CMD WD. For on line wrap around operation, it is therefore necessary to reset RT ENABLE after transmission of a status word. This can be accomplished by inverting SEND DATA and applying it to DEC RST during status word transmission. If it is required that the status word be fed back, RT ENABLE should be reset immediately after it goes HIGH by applying a LOW to DEC RST for 1 microsecond (minimum). The status word will be available at the receive register.

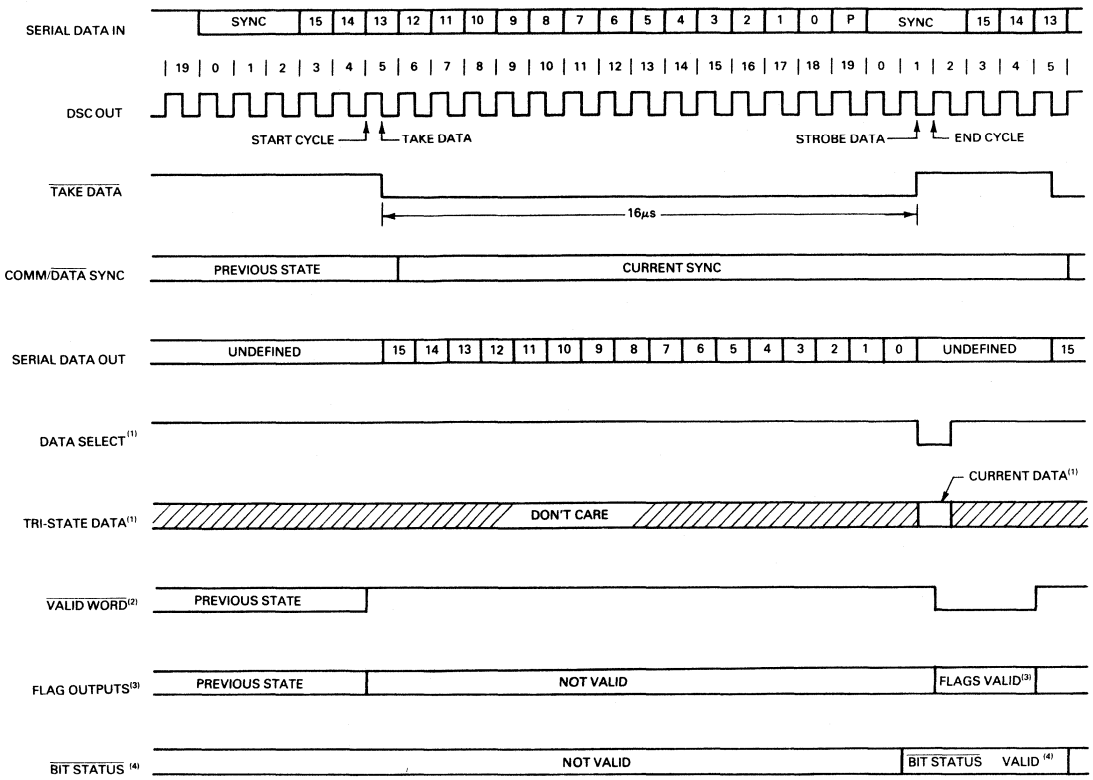
The BUS-65201 can be placed in an off line wrap around test mode by use of the S/T SELECT signal. In this mode, the transceiver is disabled and the encoder output is fed directly to the decoder input. All other functions remain the same, and the BUS-65201 compares each word that is decoded with the original word that was encoded. The BIT STATUS line also indicates the result of this comparison for the off line wrap around test.

FAILSAFE TIMEOUT

The BUS-65201 contains a timer which continuously monitors the length of each transmitted message. This timer detects a transmitted message which exceeds 768 microseconds and causes the transmission to terminate. At the same time, the FAIL-SAFE flag is set to indicate a Terminal Fail-safe Timeout. Further transmissions are inhibited until the FAIL-SAFE flag is reset by MRST or a valid command word with the correct address is received.

OUTPUT FLAGS

The BUS-65201 provides numerous output flags to offer the greatest user flexibility. VALID WORD indicates receipt of a word with valid sync, Manchester coding and parity. RT ENABLE indicates a valid word and correct address. VAL CMD WD indicates a valid word and a Command Sync. BROADCAST indicates a valid command word and an address of 11111. The BROADCAST flag may be inhibited by using the BDCST INHIBIT line. MODE CODE indicates a valid command word and a subaddress of 11111 or 00000.



NOTES:
(1) Parallel data is held continuously in second rank receiver register, and may be enabled onto the tri-state output at any time with a LOW on DATA SELECT.
(2) VALID WORD will remain LOW for 20μsec, then go HIGH, if a valid sync is not received.
(3) FLAG OUTPUTS are valid only when VALID WORD is LOW. Flags are MODE CODE, RT ENABLE, BROADCAST and VAL CMD WD.
(4) BIT STATUS is valid only if a wraparound transmit plus receive cycle has been performed. LATCH DATA must be LOW, and either S/T SELECT or RX STROBE must be HIGH for the full wraparound cycle duration.

FIGURE 3. RECEIVE MODE TIMING

INITIALIZATION

To ensure error-free operation, it is desirable to reset the BUS-65201 to its initialized state upon power turn-on. The MRST (master reset) signal is provided for this purpose. Both the decoder and encoder, as well as all flags, are reset by a LOW on MRST. This function interrupts and overrides all other control signals. The MRST function can also be used during fault recovery routines.

TRANSCEIVER OPERATION

The BUS-65201 contains a transceiver similar to DDC's model BUS-63102. When connected to a serial MUX data bus via transformer and isolation resistors, as shown in Figure 6, the BUS-65201 transceiver will fully comply with MACAIR (sinusoidal) and MIL-STD-1553 (trapezoidal) specifications. The correct DDC part numbers for transformers used in direct-coupled and transformer-coupled operation are shown in Figure 6 and Ordering Information.

Transceiver TX INHIBIT and RX STROBE signals are provided to afford flexible operation. These signals may be used to disable the transmitter and receiver, respectively. The BUS-65201 transceiver contains a transmitter protection timeout circuit. If either of the two transmitter inputs remain high for longer than 15 microseconds, the timeout circuit will shut off the transmitter until the fault condition disappears. Short circuit protection is provided, with current limited outputs, for an indefinite period.

ENCODER OPERATION

Figure 2 illustrates the transmit mode timing. Encoder detail timing is shown in Figure 4. The transmit cycle is initiated by a LOW on ENC ENABLE. The first HIGH to LOW (falling edge) transition of ESC OUT, when ENC ENABLE is LOW, starts the cycle which lasts for 20 clock periods of the 1 MHz ESC OUT. The next LOW to HIGH transition of ESC OUT strobes the SYNC SELECT line. A HIGH on SYNC SELECT produces a data sync and a LOW produces a command/status sync.

A LOW to HIGH transition of SEND DATA occurs at the fourth falling edge of ESC OUT. This indicates the completion of the sync interval and the start of the serial data interval. Parallel data must be stable at the second rank transmit register prior to the rising edge of SEND DATA, which occurs 3 microseconds (minimum) after the HIGH to LOW transition of ENC ENABLE. LATCH DATA is used to transfer parallel data to the first rank transmit register. LATCH DATA must be brought LOW and DATA SELECT brought HIGH prior to the rising edge of SEND DATA. If

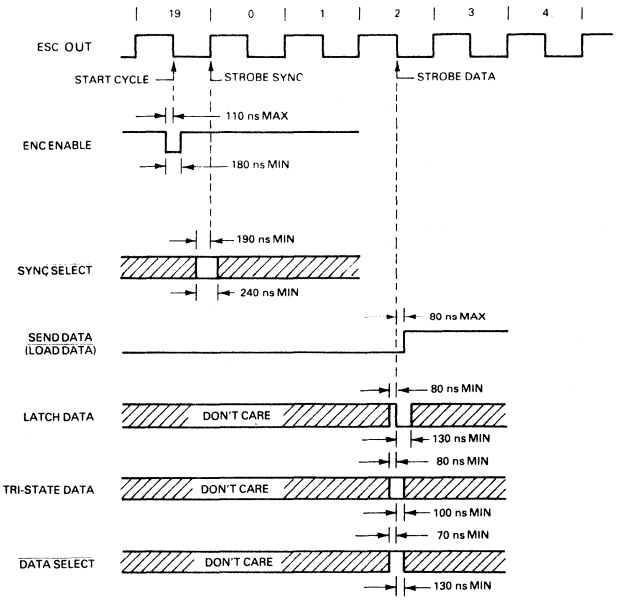


FIGURE 4. ENCODER DETAIL TIMING

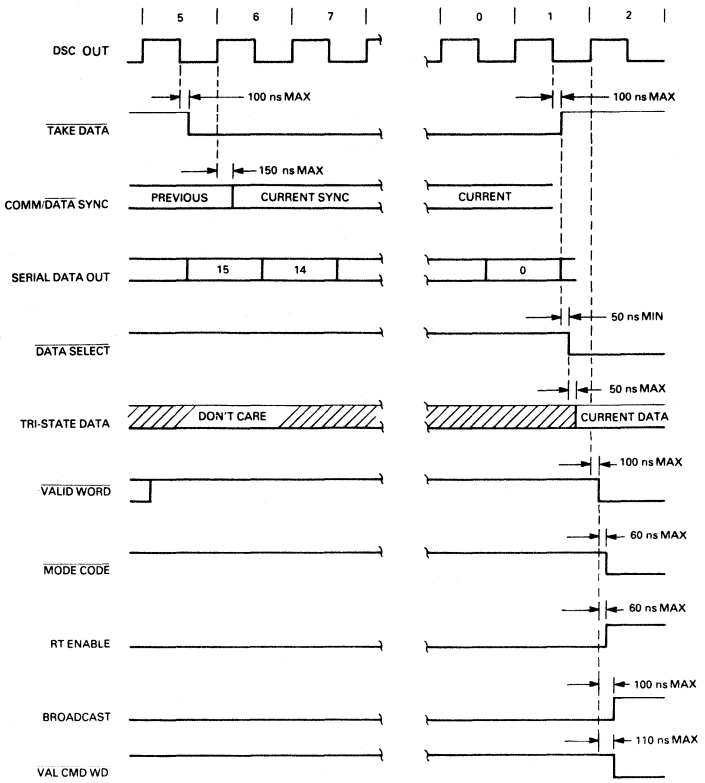


FIGURE 5. DECODER DETAIL TIMING

SEND DATA is connected directly to LOAD DATA, it will lock out the second rank transmit register and serial data shifting into the encoder will proceed properly.

For multiple word transmissions, the next word may be transferred to the transmit register any time after SEND DATA goes HIGH, but no later than the next LOW to HIGH transition of SEND DATA. SEND DATA remains HIGH for 16 periods of ESC OUT, during which time the data word is serially shifted to the Manchester encoder. The encoder adds the parity bit during the next ESC OUT period after SEND DATA goes LOW. To terminate transmission after any word, ENC ENABLE must go to HIGH no later than the first rising edge of ESC OUT after SEND DATA goes LOW.

The entire transmit cycle may be interrupted and initialized by applying a 1 microsecond (minimum) negative pulse to MRST. It is possible to input data to the encoder in serial form by forcing both transmit registers to be transparent. With LATCH DATA 1 held HIGH and LOAD DATA 1 held LOW, serial data input on D15 will be be applied directly to the encoder serial input. ESC OUT must be used to shift in the serial data, MSB first, starting at the LOW to HIGH transition of SEND DATA.

DECODER OPERATION

Figure 3 illustrates the receive mode timing. Decoder detail timing is shown in Figure 5. A receive cycle, which lasts for 20 clock periods of the 1 MHz DSC OUT, is initiated when the decoder recognizes a valid sync and two valid Manchester data bits. TAKE DATA goes LOW at the first HIGH to LOW (falling edge) transition of DSC OUT, following the second valid data bit. COMM/DATA SYNC is updated at the next rising edge of DSC OUT after TAKE DATA goes LOW. COMM/DATA SYNC remains in its new state until the next valid word or until DEC RST or MRST goes LOW.

TAKE DATA remains LOW for 16 periods of DSC OUT, during which time the 16 serial data bits are shifted into the first rank receive register. The serial data is simultaneously available at SERIAL DATA OUT as it is being shifted. At the completion of decoded data shifting, TAKE DATA goes HIGH, which transfers the data to the second rank receive register. This data may be enabled onto the parallel data highway by a LOW on DATA SELECT at any time until the next rising edge of TAKE DATA.

At the first rising edge of DSC OUT after TAKE DATA goes HIGH, VALID WORD is updated. It will go LOW if the decoded word was valid. VALID WORD will go HIGH at the start of the next receive cycle, or after 20 microseconds if no additional words are received. All output flags are enabled by VALID WORD, and therefore they are valid only as long as VALID WORD is LOW.

PIN FUNCTION AND LOADING TABLE

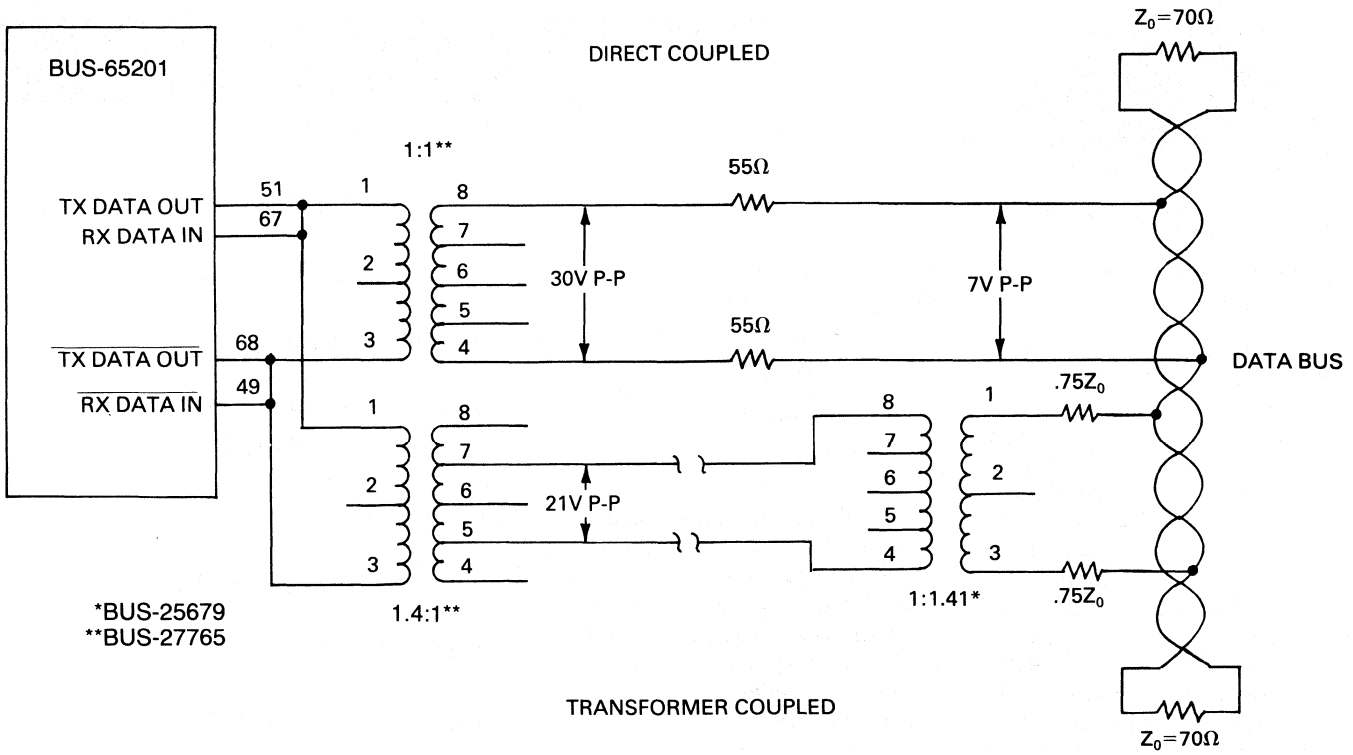
PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
1	GND					Power supply and logic return.
2	+5V OSC/ CLOCK POWER					+5V Power for oscillator and clock driver.
3	NC					No connection.
4	$\overline{\text{TX INHIBIT}}$	20	−0.4			A LOW on this input inhibits the transmitter.
5	$\overline{\text{SYNC SELECT}}$	20	−0.4			A HIGH on this input results in a transmitted DATA sync. A LOW on this input results in a transmitted COMMAND (or STATUS) sync.
6	SERIAL DATA OUT			−0.4	4.0	Received serial data in NRZ format is available at this output when $\overline{\text{TAKE DATA}}$ is LOW.
7	ESC OUT			−0.4	4.0	LOW to HIGH transitions on this output when SEND DATA is HIGH causes the transmit cycle data shifting to occur.
8	NC					No connection.
9	COMM/$\overline{\text{DATA}}$ SYNC			−.36	3.6	A LOW on this output indicates receipt of a DATA word. A HIGH indicates receipt of a COMMAND (or STATUS) word.
10	$\overline{\text{MRST}}$	40	−0.8			A LOW on this input (1 μsec minimum) resets the decoder to its initialized condition (same function as $\overline{\text{DEC RST}}$), resets FAIL-SAFE, and stops and clears the transmit cycle. This function interrupts and overrides all other controls.
11	$\overline{\text{VALID WORD}}$			−0.4	4.0	A LOW on this output indicates receipt of a valid word.
12	$\overline{\text{BIT STATUS}}$			−0.4	4.0	A LOW on this output, during wrap around self test only, indicates that the last word decoded was identical to the last word encoded.
13	LATCH DATA 1	20	−0.4			A HIGH on this input causes parallel tri-state I/O data on D8 through D15 to appear at the output of the first rank transmit register. A LOW locks out the register inputs.
14	$\overline{\text{VAL CMD WD}}$			−0.4	4.0	A LOW on this output indicates the receipt of a valid command word.
15	$\overline{\text{BDCST INH}}$	20	−0.4			A LOW on this input inhibits the indication of the BROADCAST output flag.
16	TMADD1*	20	−0.4			Part of 5 bit hard-wired terminal address input.
17	TMADD3*	20	−0.4			Part of 5 bit hard-wired terminal address input.
18	XTAL					A 12 MHz parallel resonant crystal is connected between this input and ground.
19	CLOCK OUT			−1	1.0	Output of oscillator and clock driver (see text).
20	$\overline{\text{TAKE DATA}}$			−0.4	4.0	A LOW on this output indicates that received data is being shifted into the first rank register and is available at SERIAL DATA OUT. A LOW to HIGH transition transfers the contents of the first rank receiver register to the second rank register.
21	$\overline{\text{DEC RST}}$	20	−0.4			A LOW on this input (1μsec minimum) resets the decoder to its initialized state, resets COMM/$\overline{\text{DATA}}$ SYNC to a LOW, and resets $\overline{\text{VALID WORD}}$ to a HIGH.
22	DSC OUT			−0.4	4.0	LOW to HIGH transitions on this output when $\overline{\text{TAKE DATA}}$ is LOW causes causes receive cycle data shifting to occur.
23	SEND DATA			−0.4	4.0	A HIGH on this output indicates that transmit cycle data shifting is occuring
24	CLOCK IN	±1	±.001			12 MHz clock input (20pF load) (see text).
25	S/T SELECT	20	−0.4			A HIGH on this input enables off line wrap around self test. The transceiver is disabled and the encoder output is connected to the decoder input (see text).
26	FAIL-SAFE			−0.4	4.0	A HIGH on this output indicates that a transmitted message has exceeded 768 μsec, and that transmission has been terminated. FAIL-SAFE is reset by either RT ENABLE or $\overline{\text{MRST}}$.
27	RT ENABLE			−0.4	4.0	A HIGH on this output indicates receipt of a valid COMMAND word containing the correct 5 bit terminal address plus address parity. FAIL-SAFE is reset when RT ENABLE goes HIGH.
28	$\overline{\text{MODE CODE}}$			−0.4	4.0	A LOW on this output indicates the reception of a valid COMMAND word whose sub-address field contains all ONES or all ZEROES.
29	LATCH DATA 2	20	−0.4			A HIGH on this input causes parallel tri-state I/O data on D0 through D7 to appear at the output of the first rank transmit register. A LOW locks out the register inputs.
30	$\overline{\text{ENC ENABLE}}$	20	−0.4			A LOW on this input causes the transmit cycle to start at the next HIGH to LOW transition of ESC OUT

PIN FUNCTION AND LOADING TABLE (Continued)

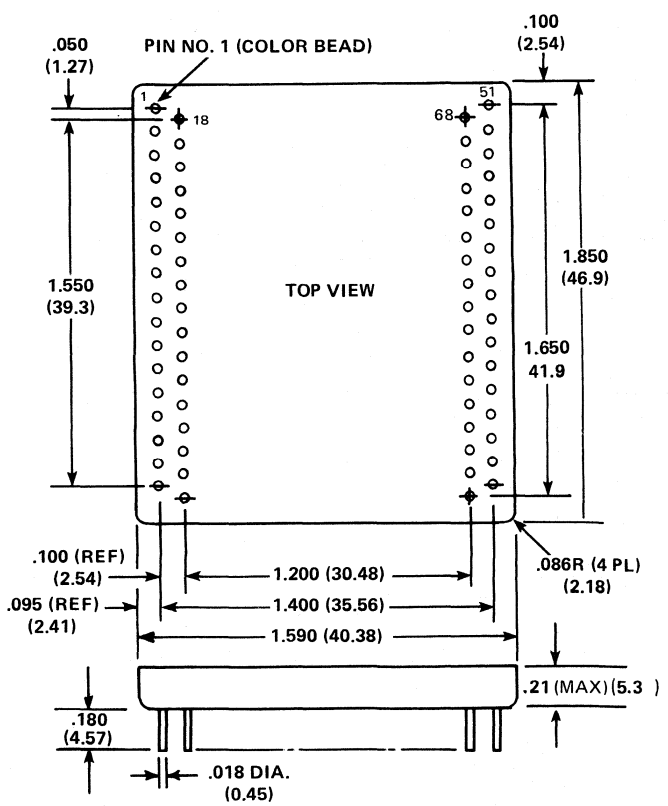
PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
31	BROADCAST			−0.4	4.0	A HIGH on this output indicates reception of a valid COMMAND word whose address field contains all ONES, if BDCST INH is HIGH.
32	TMADD0*	20	−0.4			LSB of 5-bit hard-wired terminal address input.
33	TMADD2*	20	−0.4			Part of 5-bit hard-wired terminal address input.
34	TMADD4*	20	−0.4			MSB of 5-bit hard-wired terminal address input.
35	TMADDP*	20	−0.4			Parity bit of hard-wired terminal address. Hard-wired for odd parity.
36	CHAN SELECT	100	−2.0			A LOW on this input enables DATA SELECT 1, DATA SELECT 2, LATCH DATA 1, LATCH DATA 2, and ENC ENABLE inputs.
37	ODD PARITY			−0.36	3.6	A HIGH on this output indicates a valid check for odd parity of terminal address plus parity bits, if ENA PAR CHECK is a LOW.
38	D15	20	−0.2	−12	12	MSB of 16 bit parallel tri-state I/O.
39	D13	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
40	D11	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
41	D9	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
42	D7	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
43	D5	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
44	D3	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
45	D1	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
46	LOAD DATA 2	20	−0.4			A positive transition on this input causes the data of the D0 through D7 outputs of the first rank transmit register to be loaded into the second rank transmit register.
47	+5V					+5V power supply input.
48	$+V_{cc}$					+12V to +15V power supply input.
49	RX DATA IN					Inverted receiver input.
50	RX STROBE	40	−1.6			A LOW on this input disables the receiver output.
51	TX DATA OUT					Transmitter output.
52	CASE					Case connection.
53	DATA SELECT 2	20	−0.4			A LOW on this input causes the output of the second rank receiver register to appear on D0 through D7 of the parallel tri-state I/O.
54	DATA SELECT 1	20	−0.4			A LOW on this input causes the output of the second rank receiver register to appear on D8 through D15 of the parallel tri-state I/O.
55	ENA PAR CHECK	20	−0.4			A LOW on this input enables the function of ODD PARITY.
56	D14	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
57	D12	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
58	D10	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
59	D8	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
60	D6	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
61	D4	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
62	D2	20	−0.2	−12	12	Part of 16 bit parallel tri-state I/O.
63	D0	20	−0.2	−12	12	LSB of 16 bit parallel tri-state I/O.
64	LOAD DATA 1	20	−0.4			A positive transition on this input causes the data of the D8 through D15 outputs of the first rank transmit register to be loaded into the second rank transmit register.
65	GND					Power supply and logic return
66	$-V_{cc}$					−12V to −15V power supply input.
67	RX DATA IN					Receiver input.
68	TX DATA OUT					Inverted transmitter output.

NOTES: In the above table, the symbols are defined as follows:
I_{IH}=maximum input HIGH current with V_{in}=2.5 volts.
I_{IL}=maximum input LOW current with V_{in}=0.4 volts.
I_{OH}=maximum output HIGH current for V_{out}=2.5 volts minimum.
I_{OL}=maximum output LOW current for V_{out}=0.4 volts maximum.

*Indicates use of an internal pull-up resistor.



MECHANICAL OUTLINE



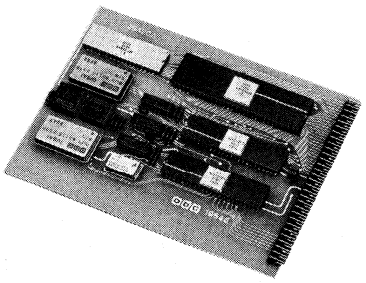
Note: Dimensions in inches (millimeters)

ORDERING INFORMATION

BUS-65201-883B

MIL-STD-883 Processing:
883B=Conforms to MIL-STD-883 DDC Procedures
Blank=Same, except burn-in is omitted

Note:
Use BUS-27765 transformer with BUS-65201 (direct-coupled)



DUAL REDUNDANT MIL-STD-1553 RTU INTERFACE CARD

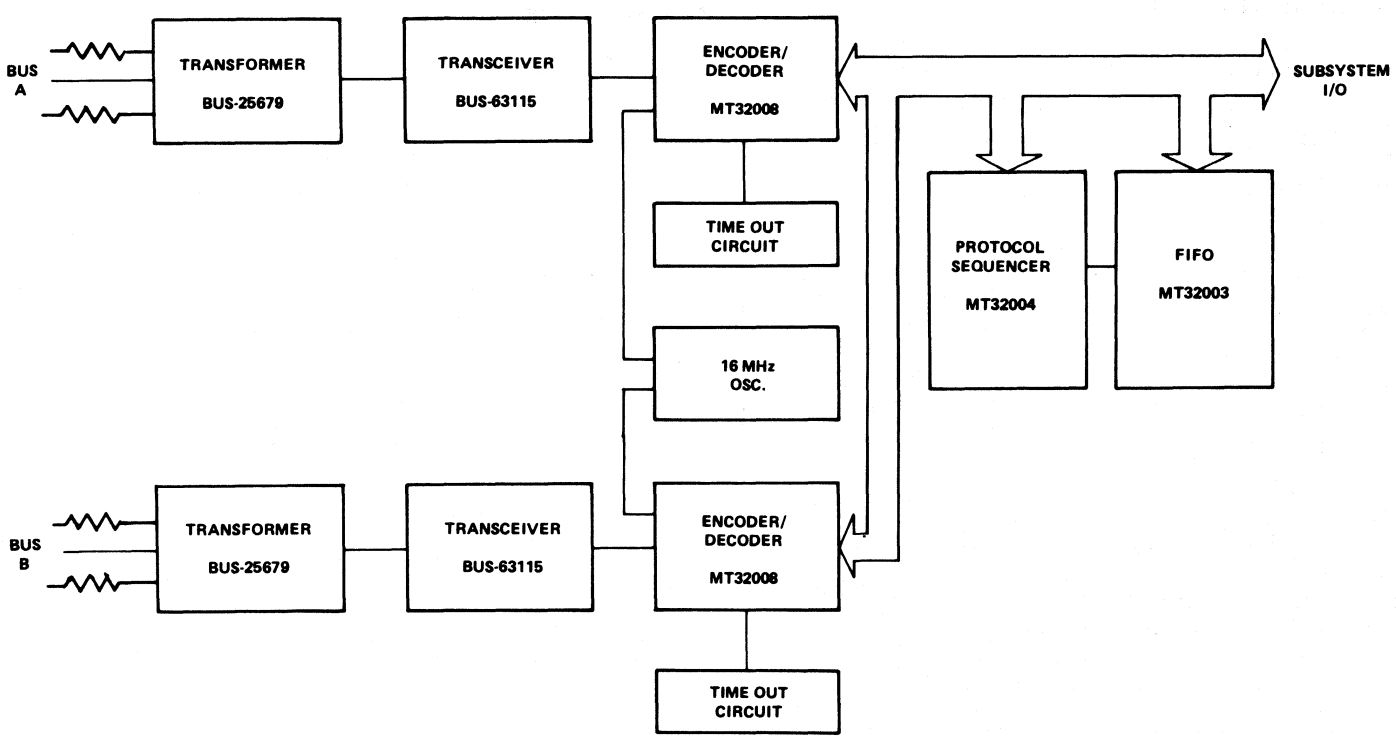
DESCRIPTION

The BUS-65400 is a Dual Redundant RTU card assembly which will interface directly to a dual redundant MIL-STD-1553B MUX BUS on one side and to a subsystem on the other. It can be purchased and incorporated directly into the user's subsystem or used as a component and circuit evaluation board in the design phases of a program. The BUS-65400 board includes isolation resistors, Transformers BUS-25679, Transceivers (BUS-65115)), Encoder/ Decoder (MT-32008), a Protocol Sequencer (MT-32004), a 32 word FIFO (MT32003) and dual watch-dog time-out circuits. The BUS-65400 meets all the requirements of MIL-STD-1553B, including wrap-around test and all assigned mode codes.

This data sheet describes the operation of the entire dual redundant RTU and each of its major components. Detailed descriptions and complete specifications for each device are available to assist in SCD preparation or for a more complete understanding of component and system operation.

FEATURES

- *SMALL SIZE*
- *LOW POWER*
- *FULL COMPLIANCE WITH MIL-STD-1553B*
- *ALL MODE CODES*
- *WRAP AROUND TEST*
- *INCLUDES FIFO*
- *DUAL REDUNDANT*



BUS-65400 FUNCTIONAL DIAGRAM

RTU COMPONENTS

TRANSCEIVER

The BUS-63115 monolithic Transceiver receives and transmits the phase-modulated bipolar, 1 MHz, Manchester II coded data via the BUS-25679 Transformers. The receiver section accepts this data and produces a biphase TTL signal at the complementary outputs TX DATA OUT and TX DATA OUT. These outputs are both high when idle to complement the MT32008, Encoder/Decoder. The receiver threshold is internally set at the factory for a nominal 1V p-p signal, measured on the bus. External strobe inputs (RCVR STROBE—pins 42 and 32) are provided on the board to turn off each of the receivers. A logic "0" applied to the RCVR STROBE will disable the appropriate receiver outputs.

The BUS-63115 transmitter sections accept biphase TTL data at the input and produce a 27 volts p-p differential signal across a 145Ω load, when measured at the transformer's output to the bus.

When TX DATA and TX DATA are either both low or both high, the transmitter presents a high impedance to the line. The BUS-63115 has a 10–15 μs built-in time-out circuit to prevent the transmitter from remaining on during idle times due to a non-complementary state at the TX DATA and TX DATA lines. The transmitter output is current limited (Not Fold Back) for protection against indefinite short circuits.

DECODER

The Decoders (half of MT32008) accept the biphase TTL signal from the transceivers, decode it and load it into the receiver shift register, where address detection as well as Manchester code, odd parity and sync detection are validated. The decoder generates ANOTHER WORD after every valid sync field plus the first three data bits. If the decoder validates the command word, its own address (hardwired on pins 4, 34, 5, 35, 6 and 33), and proper parity, then the Command Sync (CMD SYNC, VALID WORD, and THIS RT flags will all go low at the same time. If the address is all "1"s, i.e., a broadcast command, then BDCST DETECT will go low (instead of THIS RT) with the other flags. The signals ANOTHER WORD and VALID WORD will repeat their sequence for each data word following the command word. During VALID WORD, the decoded data is shifted into the input buffer register and becomes available on the 16 bit parallel (T0 thru T15) highway for 20 microseconds The subsystem is made aware of this occurance by the VAL CMD WD REC signal (pin 59) outputted by the MT32004, which will be discussed later.

ENCODER

The Encoders (half of MT32008) take the 16 bit parallel data, add the correct sync field and odd parity bit, and then output it to the BUS-63115 transceivers as biphase TTL complementary data. The correct redundant data bus Encoder must acknowledge that THIS RT ADDR LS matches THIS RT ADDR IP LS in order to insure that it has been selected. The Select Enable (SEL EN) signal goes high when the redundant bus addresses match. Once SEL EN is valid, data is loaded into the output buffer register by the LOAD BUFFER command. The SEND DATA signal activates the shift and load control logic. This signal initiates the actual biphase TTL transmission while also generating the BUFFER FULL status flag.

BUS CONTROLLER NOTE

The MT32008 Encoder/Decoder has provision for use in a Bus Controller configuration. It has two extra control lines on the encoder's parity and sync generation circuitry. The type of sync field desired can be externally set. It also permits external setting of the transmit/receive TX/RX bit (T10) of the command word. For more information on bus controller applications consult the factory.

FIFO

The MT32003 is a 16 bit wide by 32 word long first-in-first-out (FIFO) memory LSI chip. This device is an integral accessory to the protocol sequencer. The memory is controlled by six control lines: Data Input Ready (DIR), Data Output Ready (DOR), Shift-In (SI), Shift-Out (SO), RESET and ENABLE. (Please refer to Figure 2 timing chart). These control lines are provided by the MT32004 protocol sequencer to move data in and out of the FIFO.

NOTE: If blocks of 32 data words are continuously received at the same RT, then the transfer of data to the subsystems (via DATA STRB) at the max rate allowable (by the protocol sequencer) of .5 MHz is too slow to complete the full transfer in under a 12 microsecond response time. (Please refer to Figure 2 timing chart). Through the addition of a simple FIFO buffer circuit the subsystem may take control of the data transfer as shown in Figure 6, which will enable the transfer rate to be increased to 2 MHz.

The VAL CMD WD REC signal will reset or clear the FIFO for the next cycle. The only exception to this is when the WRAP ENABLE (pin 49) is made valid by the subsystem after receipt of a valid subaddress code of 11110. (Refer to Figure 3 timing chart). When enabled, no DATA STRB (pin 60) will be provided. Data will be held in the FIFO until the next RX command word requests this data. The controller can then compare the received data with the data originally sent out, thus providing a dynamic RT test.

PROTOCOL SEQUENCER

The MT32004 Protocol Sequencer chip interfaces directly with the MT32008 Encoder/Decoders, MT32003 FIFO and the subsystem through control lines and the 16 bit parallel three-state highway. Functionally, the Sequencer contains a FIFO status circuit, command register, last command register, built-in-test (BIT) register and status register, all of which can be accessed on the highway. It contains all the the mode code control logic, receive control logic, transmit control logic as well as its own time-out counter for 8, 17, 21 and 34 microsecond interval checking. The MT32004 also contains a word counter and receive count register which are compared automatically. A similar comparison is made when the command address register is compared to the status address. Finally, the Sequencer has

incorporated a power on reset feature for initializing all the internal counters and registers on power up.

In the receive mode the Protocol Sequencer monitors all the decoder control lines in preparation of a new valid command word. When a valid command word is received, processing will commence.

NOTE: WHEN ANOTHER VALID COMMAND WORD IS RECEIVED, THE SEQUENCE WILL BE TERMINATED AND IT WILL START SEQUENCING THE NEW COMMAND WORD.

The MT32004 will only consider a command word valid if the following conditions are met:

a) CMD SYNC, VALID WORD, THIS RT or BC DETECT becomes active at the same time.

b) The command word does not follow contiguously a valid data on the same bus.

Once a valid command word is established and the RT address is correct, the THIS RT ADDR IP pins are set by the sequencer so that the MT32008 is enabled for further data receiving or transmitting. At the same time VAL CMD WD REC becomes active for 500 ns. The decoded command word is available on the T0-T15 highway during this period.

The Protocol Sequencer then enables the input buffer (EN IP BUFFER) so that the data can be loaded into the command register. Bits T5 to T9 are examined to detect either a mode code or wrap around command. On all commands, except the wrap around transmit command, the FIFO is cleared. If a mode code is not detected then the least significant 5 bits contain the number of data words to be received or transmitted. The five bits are loaded into a word counter, the contents of the command register are loaded into the last command register, and the status register is cleared. Bit ten of the command register is then examined for transmit (TX) or receive (RX) mode.

TRANSFER FORMATS

RT TO BUS CONTROL TRANSFER

A broadcast address received with a valid command word in the transmit (TX) mode is not valid. If it occurs, the message error bit and broadcast command received bit in the status register will be set (bits T10 and T4) and the sequence terminated.

If the command is a valid TX then the status register is enabled onto the T0-T15 highway and the sequence halts for approximately 8 μs to see if another valid word has been detected (which is a fault condition). If another valid word is detected (ANOTHER WORD) then the message error bit in the status register is set and the sequence is terminated. If ANOTHER WORD is not detected, the contents of the status registers are loaded into the output buffer of MT32008 via load buffer for 125 ns and simultaneously the SEND DATA signal is valid for 250 ns. (Refer to Figure 3 timing chart). At the end of the SEND DATA pulse the transmit sequence will begin sending out the status word.

The response time measured from the middle of the last received bit of the TX command to middle of the first bit of the status word sync is approximately 10.8 μs.

While the status word transmission is taking place the terminal flag (TF) latch is cleared, and the contents of the command register are transferred to the subsystem interface unit (SSIU). The contents of the command register are enabled onto the highway during the 8.5 μs command strobes (CMD STRB) period.

If the SUBSYSTEM BUSY signal (pin 17) is activated by the subsystem, the busy bit of the status register will be set. After the CMD STRB period the sequence will terminate so no data will be transmitted.

When the CMD STRB period ends the sequencer will halt until the subsystem enables the first data word onto the 16 bit highway by activating the SSIU STRB (pin 28). This data is loaded into the output buffer and the word counter is decremented by one. The SSIU continues transferring its 16 bit parallel words to the MT32004 by enabling the data onto the highway and sending an SSIU STRB at a transfer rate between 100 KHz (10 μs) and 1 MHz (1 μs). (Refer to Figure 3 timing chart).

The first data word is loaded directly into the output buffer ready to be transmitted. While the first word is being transmitted the BUFFER FULL signal will become not valid, allowing the second data word to be shifted out of the FIFO and loaded into the output buffer ready for transmission. This occurs when the SSIU STRB is not valid so that the sequencer can take control of the 16 bit highway to transfer the data from the FIFO. The subsystem (SSIU) must only enable its three-state interface during the SSIU STRB valid time. This data shifting sequence is repeated as the word counter is decremented by one for every SSIU STRB until the word counter equals zero. When the word counter equals zero the shift in signals to the FIFO are disabled and the sequence is terminated.

If another SSIU STRB occurs within 17 μs after the word counter equals zero, Bit 1 of the built-in-test (BIT) register is set and the sequence is terminated.

BUS CONTROLLER TO RT TRANSFER

If a valid RX command word is received, bit T10 of the command register is set to "0" and the Protocol Sequencer is ready to receive data. Data being received must be continuous with no interword gaps. The first word received immediately after the command word is checked for no interword gap and that it is a valid data word. If it turns out to be another command word, then an RT to RT command has been issued (Refer to RT to RT transfer).

If an intermessage gap is detected on the incoming data words, the message error bit in the status register is set and the sequence will terminate.

If there are fewer or more valid data words (detected by counting ANOTHER WORD received than were indicated in the command word, the message error bit in the status register is set and the sequence is terminated.

When the complete message is contained in the FIFO and a broadcast command has not been detected, the contents of the status register are enabled onto the highway and the (status word) transmit sequence is initiated. The terminal flag (TF) is cleared during transmission of the status word.

If the command was a broadcast then the transmit status sequence is bypassed and the broadcast received bit in the status register is set. The CMD STRB output (pin 29) is activated for 8.5 μs so that SSIU transfer may take place. When the CMD STRB transfer ends, the FIFO is enabled so that its contents can be transferred onto the highway by the DATA STRB (pin 60). The SSIU may stop the normal .5 MHz max data transfer by holding DATA STRB low. (Please refer to Figure 6 and description of an external 2 MHz DATA STRB circuit). When the DATA STRB is released by the SSIU the next word is shifted to the front of the FIFO. This transfer cycle is repeated until the FIFO is emptied.

RT TO RT TRANSFER

The bus controller initiates an RT to RT transfer by sending a receive command word to RTU #1 followed by a transmit command to RTU #2. The RTU #2 will reply with a status word followed by the requested contiguous data words. RTU #2 will initiate the receive sequence on receipt of a valid receive command word with its own RT address and will monitor the RTU #2 TX command for validity and no interword gap. If it meets these two requirements, then the contents of RTU #1 input buffer (the transmit command word for RTU #2) will be enabled onto the 16 bit highway. If a valid TX Command Word is not received contiguously then the message error bit in the status register will be set and the sequence terminated.

When valid, the most significant 5 bits (the RTU #2 address) are loaded into the 5 bit command address register and the sequence on RTU #1 will halt for 20.5 μs. If during this time a valid data word or command word for another RT occurs, this would be a fault condition and the message error (ME) bit in the status register will be set and the sequence terminated. A valid command word received with RTU #1 address will override the complete sequence and reset the sequencer. The sequencer will wait 14 μs and if RTU #2 has not transmitted its status word by this time (whose contents are now in RTU #1's input buffer) the ME bit in the status register will be set and the sequence will terminate.

If there is no fault condition, the RTU #2 address on the highway is compared with the contents of the command address register. If they are not the same, then this is a fault condition which sets the ME bit and the sequence is terminated. If they do match, the sequence will continue.

WRAP AROUND

The wrap around test is initiated by receipt of a valid RX command word containing the code 11110 in the subsystem address (bits T5 thru T9). The contents of the word counter are loaded into the receive count register. The WRAP ENABLE input (pin 49) must be set high for the Protocol Sequencer to perform this function. (Refer to Figure 3 timing chart).

The wrap around test will perform like a standard Bus Control to RT transfer, except the sequence terminates after the status word and no DATA STRB's are provided since no transfers to SSIU will be made. The received data will remain stored in the FIFO.

The bus controller will send a TX command word and the sequencer will perform as a RT to Bus Controller, but the FIFO is not cleared by this TX command word. While the status word is being transmitted the contents of the receive count register are compared to the contents of the word counter. If the contents are not equal the ME bit in the status register is set and the sequence will terminate. If they are the same the FIFO is enabled and the contents are transmitted one word at a time.

MODE CODE IMPLEMENTATION

When a valid command word containing a mode code is received, the FIFO is cleared and the mode code sequence is initiated. In all mode codes, except transmit last command, the contents of the command register are loaded into the last command register.

DYNAMIC BUS CONTROL (CODE 00000) T/R =1

This mode code can be generated from an external CPU which is capable of performing bus control. When VAL CMD WD REC is present the SSIU can set DYNAMIC BUS ACCEPTANCE (input pin 18) which will set bit T1 of the status word, thereby accepting the bus control function.

SYNCHRONIZE WITHOUT DATA WORD (CODE 00001) T/R =1

The T/R bit of the RX command word must be set to a one for this mode code. If it is set to a zero then the ME bit in the status register is set and the sequence terminated. This same fault condition will result if it is set to a zero and a broadcast command is detected.

At the end of status word transmission all zeros are enabled onto the highway and a 250 ns active low pulse is applied to the synchronize output (pin 50). (The TF latch and status register are cleared upon receipt of a valid command).

TRANSMIT STATUS WORD (CODE 00010) T/R = 1

If a VAL CMD WD REC is received, the status register is enabled onto the highway (but is not cleared) and transmitted. The TF latch is cleared after the transmit sequence and then the sequence is terminated.

INITIATE SELF TEST (CODE 00011) T/R = 1

This mode code has an error checking and status word transmission sequence the same as the "synchronize without data word" previously described.

At the same time as SEND DATA a 500 ns BITE OUT pulse is sent to the external time-out circuits. The correct time-out circuit is enabled by the active MT32008 SEL EN signal. After a period of 672 μs to 800 μs the signal BITE

$\overline{IN}$ should time-out and return high. If this occurs too early or too late the least significant bit of the built-in-test register is set to a "1". The sequence then terminates. (Please refer to Figure 5 timing chart "initiate self test").

TRANSMITTER SHUTDOWN (CODE 00100) T/R = 1

This command may be used with a DDC BUS-65400 dual redundant configuration.

At the end of the error checking and status word transmission sequence THIS RT ADDR IP on the bi-directional address highway are examined. If it was set to 00 then it is reset to 01. If it was set to 01 then it is reset to 00. This disables the transmitter of the addressed encoder by generating a SEL TX DIS signal. Gating the correct encoder is handled by the SEL EN signal, which is generated by comparing this RT ADDR to THIS RT ADDR IP after it has been reset.

OVERRIDE TRANSMITTER SHUTDOWN (CODE 00101) T/R = 1

This command performs the same sequence as in transmitter shutdown, but the pulse is applied to signal SEL TX EN. This will re-enable the redundant bus. The sequence will then terminate.

INHIBIT TERMINAL FLAG BIT (CODE 00110) T/R = 1

The TF bit is used to detect any power resets or interruptions to the VDD power (+5 Volts). Once latched, the Protocol Sequencer must generate "CLEAR TF" (internal to chip). The TF bit is not reset until "CLEAR STATUS" (internal to chip) occurs. If the "CLEAR STATUS" occurs while the latch is still set then the status bit will return back to the set condition when "CLEAR STATUS" is removed. With a valid inhibit TF bit command word, the standard error checking and status word transmission will take place and the sequence will then terminate. As the terminal flag (TF) bit of the status register is used to detect power on, it is not inhibited (it has an embedded latch).

OVERRIDE INHIBIT TERMINAL FLAG BIT (CODE 00111) T/R = 1

The error checking and status word transmission sequence is initiated and the sequence is then terminated. Override inhibit TF is not performed due to "INHIBIT TF" (internal to chip) not operating.

RESET REMOTE TERMINAL (CODE 01000) T/R = 1

The standard error checking and status word transmission sequence starts. After receipt of $\overline{\text{VAL CMD WD REC}}$ a reset signal will clear the FIFO, and reset the MT32008 Encoder/Decoder and MT32004 Protocol Sequencer.

RESERVED MODE CODES (CODES 01001 TO 01111) T/R = 1

A valid reserved mode code will enable, but not clear, the status register and set the ME bit. The status word is transmitted, the TF latch is cleared and the sequence then terminates. If it was a broadcast command, then the broadcast received bit of the status register is set and the sequence terminates without transmitting the status.

TRANSMIT VECTOR WORD (CODE 10000) T/R = 1

(Refer to Figure 4 timing chart).
The T/R bit must be a one in order to clear the status register. A zero T/R bit will set the ME bit in the status register and the sequence will terminate. If a broadcast command is received, the ME bit and the broadcast received bit of the status register are set and the sequence is terminated.

The vector word transmit sequence is initiated by $\overline{\text{SEND DATA}}$ and $\overline{\text{LOAD BUFFER}}$. The TF latch is then cleared and the sequence will wait until the status register is being transmitted via signal $\overline{\text{BUFFER FULL}}$.

The $\overline{\text{EN VECTOR WORD}}$ output (pin 30) signal becomes valid for 250 ns in which time the SSIU vector word must be enabled onto the highway. The sequence then terminates. $\overline{\text{EN VECTOR WORD}}$ signal returns high until the next command word is received.

SYNCHRONIZE WITH DATA WORD (CODE 10001) T/R = 0

(Refer to Figure 4 timing chart).
If T/R bit is set to a one, the ME bit in the status register is set and the sequence will terminate. If the T/R bit is set to zero the status register is cleared. If a broadcast command is received, the broadcast received bit of the status register is set.

The RX command word is checked to insure a contiguous data word follows. If it doesn't, the ME bit of the status register is set and the sequence terminates. When a valid data word is received it is stored in the FIFO and a further check is made to ensure that only one data word is received via signal $\overline{\text{ANOTHER WORD}}$. If another word is detected, the ME bit is set and the sequence is terminated.

The "synchronize with data word" enables the status register onto the highway for transmission. The TF latch is then cleared, the contents of the FIFO are enabled onto the highway and a 250 ns pulse is simultaneously applied to the $\overline{\text{SYNCHRONIZE}}$ output (pin 50).

TRANSMIT LAST COMMAND (CODE 10010) T/R = 1

The mode code error checking sequence is the same as "Transmit Vector Word". It differs by enabling the contents of the last command registers onto the 16 bit highway to be transmitted. Also, the status register is not cleared before transmission, and the TF latch is cleared after the status word transmission.

TRANSMIT BIT WORD (CODE 10011) T/R = 1

This mode code is error checked and sequenced in the same way as "Transmit Vector Word", but the contents of the built-in-test register are enabled onto the highway for transmission. The BIT word register is then cleared and the sequence terminated.

SELECTED TRANSMITTER SHUTDOWN (CODE 10100) T/R = 0

(U.S. Air Force has cancelled the use of this code).
This mode code is error checked and sequenced in the same manner as "Synchronize with Data Word".

If a valid data word is received, it is stored in the FIFO. The least significant 2 bits (T0 & T1) of the data word are compared to THIS RT ADDRESS of the receiving MT-32008. If they are the same this is a fault condition and the ME bit is set. The status register is then transmitted.

If the bits are not the same, then the two least significant bits of the FIFO contains THIS RT ADDRESS of the MT32008 to be shut down.

The sequencer will then change the THIS RT ADDR IP signals to the contents of T0 and T1 (i.e., SEL EN becomes valid for the MT32008 to be shut down), while a pulse on signal SEL TX DIS terminates the sequence.

OVERRIDE SELECTED TRANSMITTER SHUTDOWN (CODE 10101) T/R = 0

Same as above except that a pulse is applied to signal SEL TX EN.

RESERVED MODE CODES (CODES 10110 TO 11111)

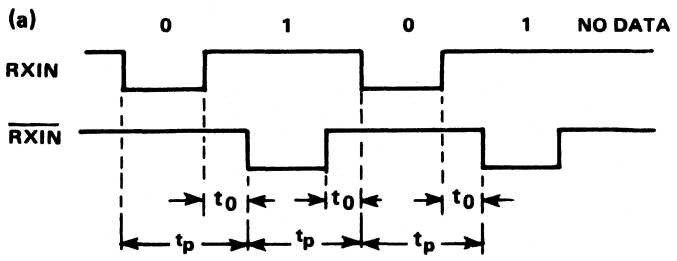
If a valid reserved mode code is received then the ME bit of the status register is set. The status register is then enabled, but not cleared, and then transmitted. The TF latch is cleared and the sequence terminates. If it is a broadcast command, then the broadcast received bit of the status register is set and the sequence terminates without transmitting the status.

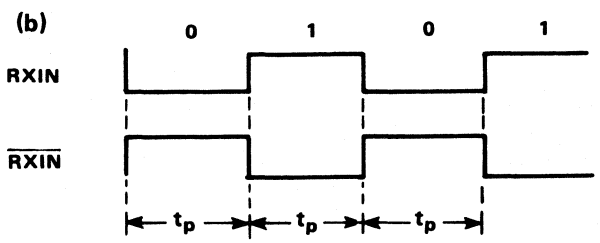
DETAILED TIMING

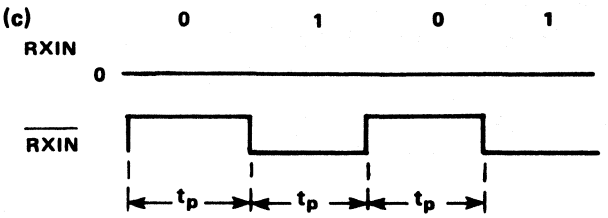
RECEIVE MODE

RXIX Waveform Requirements

There are three variations of waveform requirements required at the RXIN and $\overline{\text{RXIN}}$ inputs.







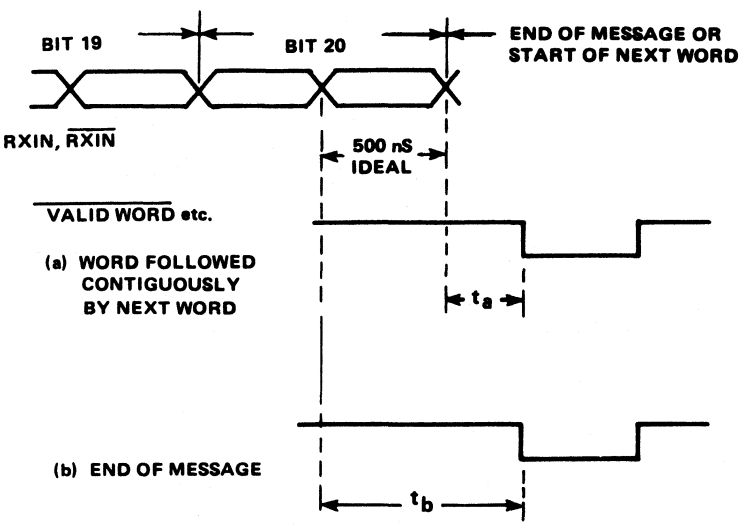
(to) 10 ns min to 400 ns max.

(tp) ±150 ns (i.e., 2.0 ±.15 μs, 1.5 ±.15 μs, 1.0 ±.15 μs, .5 ±15 μs)

Waveform (a) is the ideal. With waveform (b) applied, the device is less immune to noise on these inputs than waveform (a). With waveform (c) applied, the device is less immune to noise on these inputs than waveform (b).

PROPAGATION DELAYS

Propagation Delays over free air temperature range VDD = 5 volts. Propagation delays do not include rise and fall time of outputs. Propagation delay time or RXIN to VALID WORD, CMD SYNC, THIS RT, BC DETECT.



ta 300 ns min – 480 ns max.

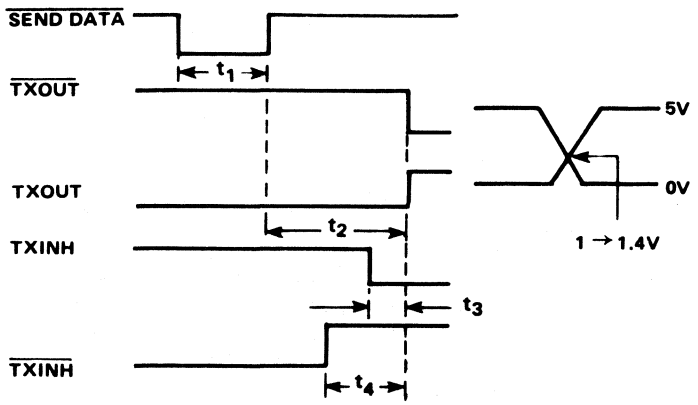
tb 800 ns min – 980 max.

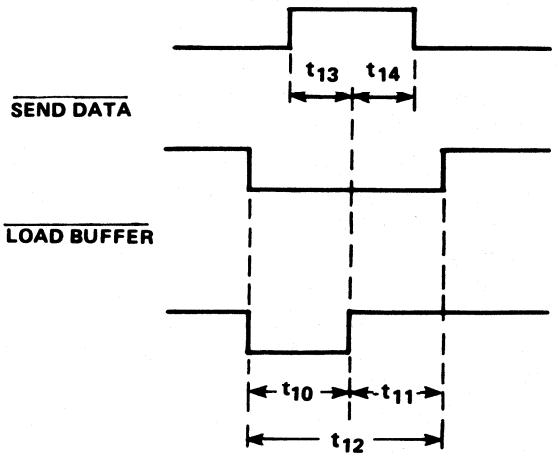
Propagation delay time:

	MIN	MAX	
$\overline{\text{CMD SYNC}}$ to T0-T15	20	40	ns
CMD SYNC to THIS RT ADDR IP (remains enabled for half bit period, 500ns ideal)	50	100	ns
$\overline{\text{CMD SYNC}}$ to SEL EN	150	250	ns
$\overline{\text{EN IP BUFFER}}$ to T0-T15	75	125	ns

TRANSMIT MODE

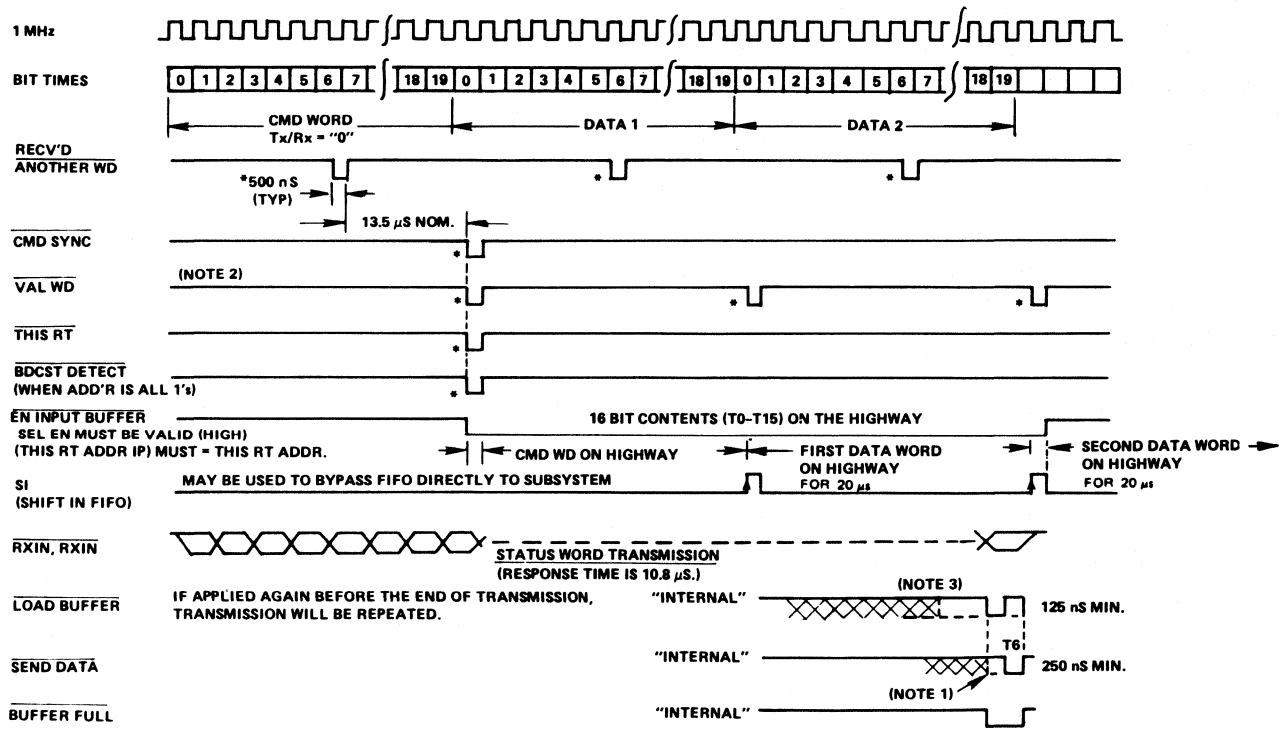
Propagation delay time SEND DATA to TXOUT, TX INH.





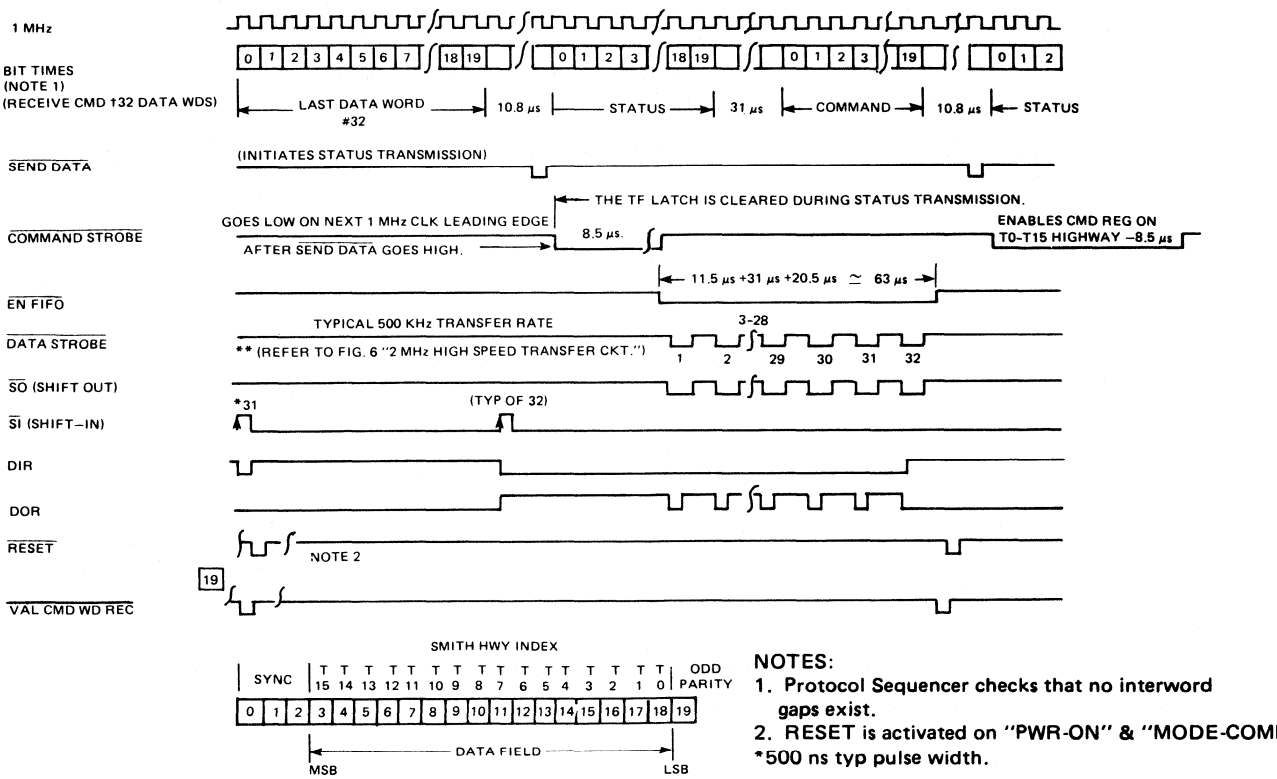
If the device is required to internally load its own RT address to be transmitted with status, then the send data and load buffer signals must be as shown.

	MIN	MAX	
t_1	250		ns
t_2	320	500	ns
t_3	70	110	ns
t_4	90	150	ns
t_{10}	125		ns
t_{11}	125		ns
t_{12}	250		ns
t_{13}	75		ns
t_{14}	75		ns



NOTE 1. SEND DATA MUST BE APPLIED SAME TIME AS LOAD BUFFER IF HARDWIRED RT ADDRESS IS TO BE INTERNALLY ENABLED ON T11-T15 HIGHWAY.
2. DATA WAS SHIFTED INTO THE INPUT BUFFER REGISTER PRIOR TO VAL WD.
3. LOAD BUFFER ACTIVATION WILL OVERWRITE CONTENTS OF OUTPUT BUFFER REGISTER.
*500 NS TYP PULSE WIDTH

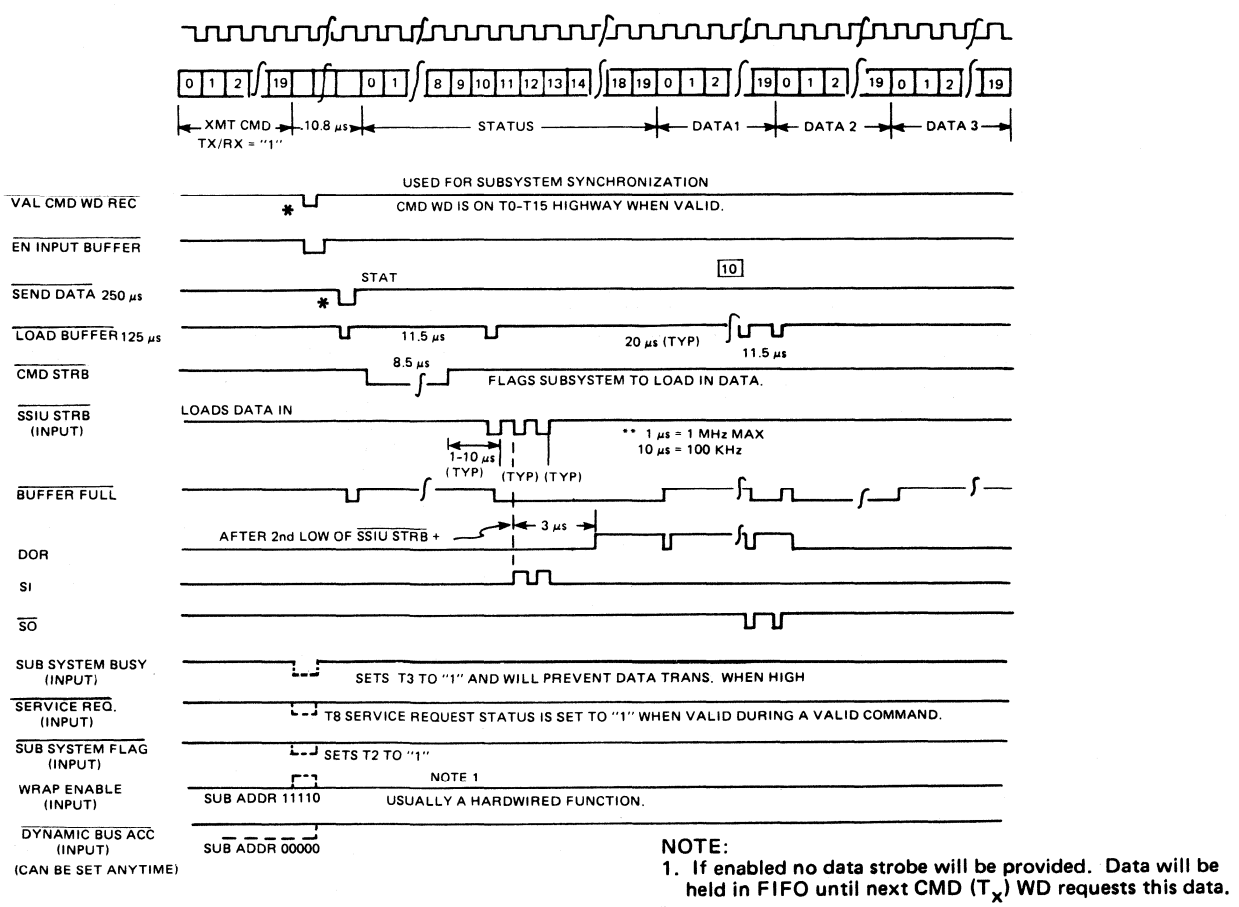
FIGURE 1. RECEIVER MODE TIMING, MT32008



NOTES:
1. Protocol Sequencer checks that no interword gaps exist.
2. RESET is activated on "PWR-ON" & "MODE-COMMAND".

*500 ns typ pulse width.

FIGURE 2. RECEIVER MODE TIMING, MT32004 & MT32003



NOTE:
1. If enabled no data strobe will be provided. Data will be held in FIFO until next CMD (T_X) WD requests this data.

*500 ns type pulse width

FIGURE 3. TRANSMITTER MODE TIMING MT32004

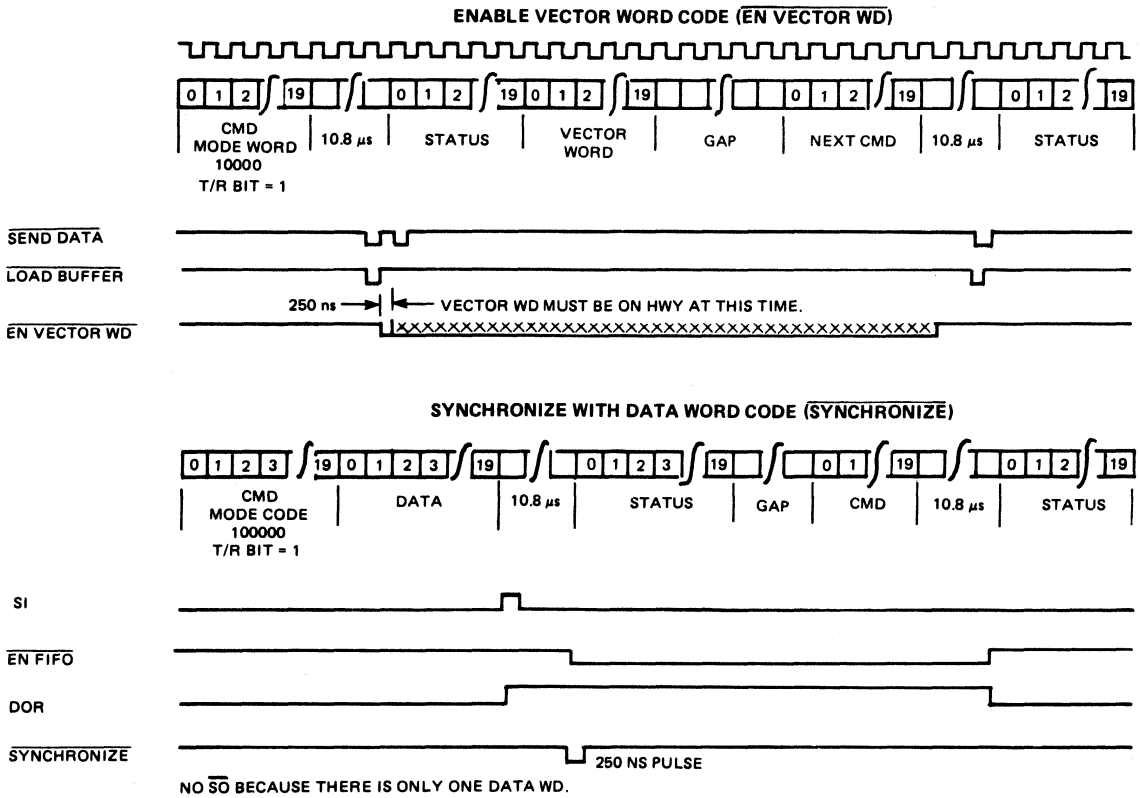


FIGURE 4. MODE CODING TIMING, EN VECTOR WD AND SYNCHRONIZE WITH DATA WORD

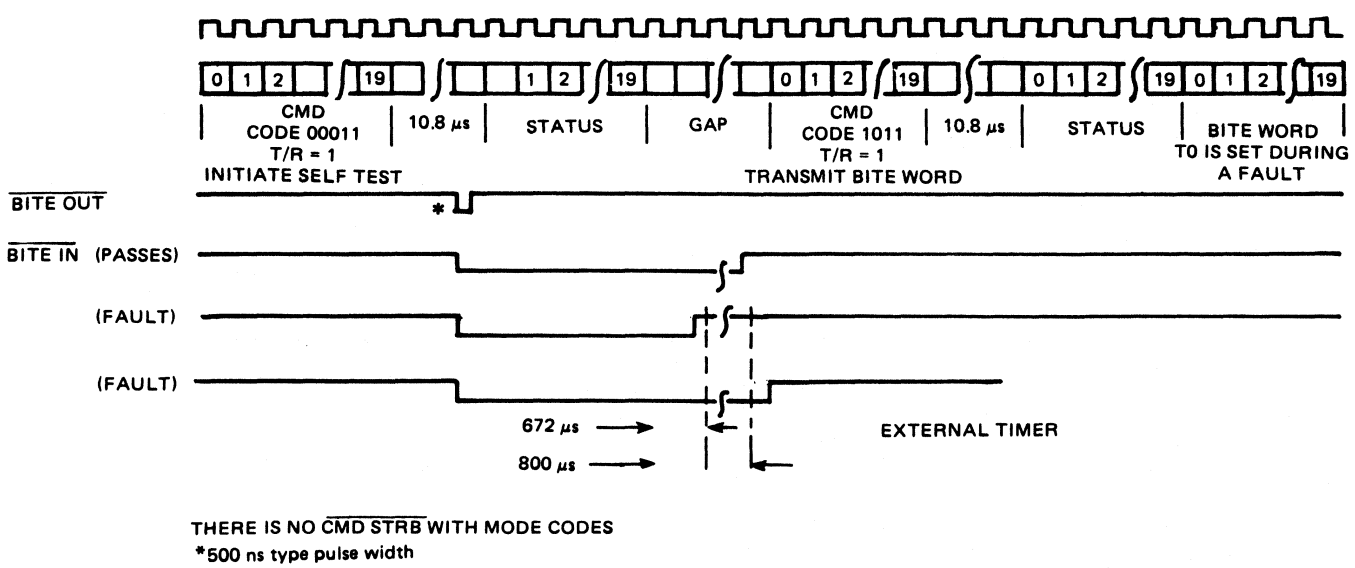


FIGURE 5. MODE CODE TIMING, INITIATE SELF-TEST

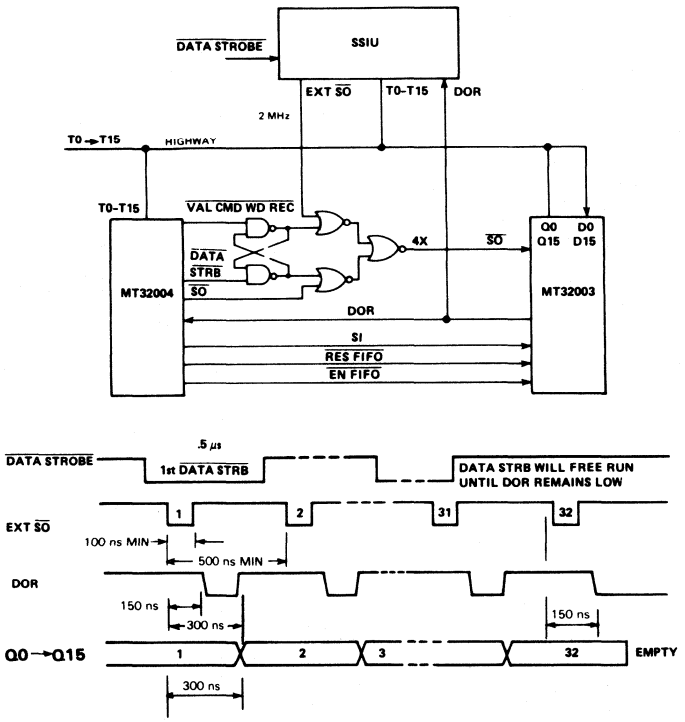


FIGURE 6. HIGH SPEED TRANSFER CIRCUIT

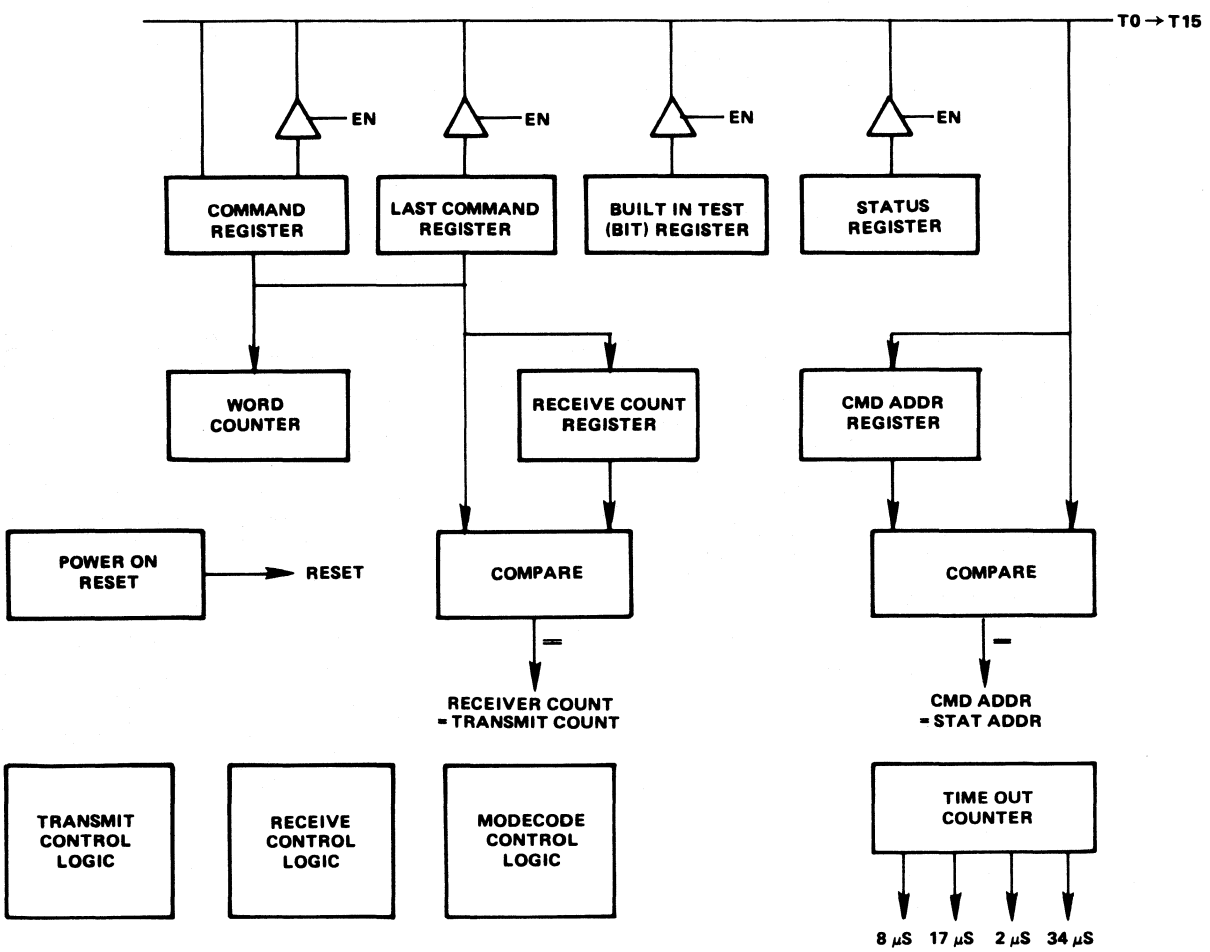
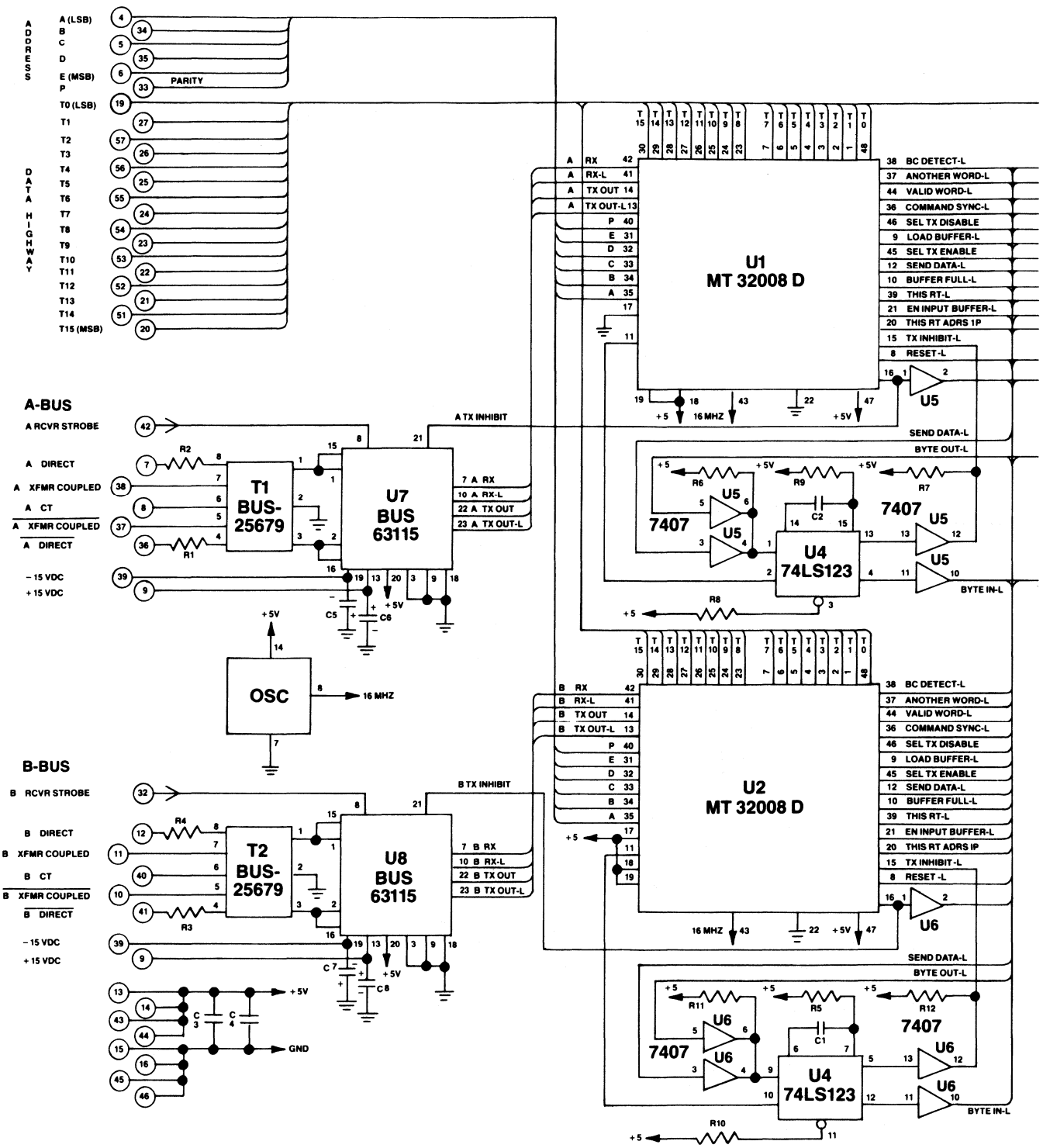


FIGURE 7. SIMPLIFIED BLOCK DIAGRAM (MT32004)


ADDRESS
A (LSB)
B
C
D
E (MSB)
P
PARITY
DATA HIGHWAY
T0 (LSB)
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15 (MSB)
U1
MT 32008 D
U2
MT 32008 D
A RX
A RX-L
A TX OUT
A TX OUT-L
B RX
B RX-L
B TX OUT
B TX OUT-L
BC DETECT-L
ANOTHER WORD-L
VALID WORD-L
COMMAND SYNC-L
SEL TX DISABLE
LOAD BUFFER-L
SEL TX ENABLE
SEND DATA-L
BUFFER FULL-L
THIS RT-L
EN INPUT BUFFER-L
THIS RT ADRS 1P
THIS RT ADRS IP
TX INHIBIT-L
RESET -L
A-BUS
A RCVR STROBE
A DIRECT
A XFMR COUPLED
A CT
A XFMR COUPLED
A DIRECT
-15 VDC
+15 VDC
T1
BUS-
25679
U7
BUS
63115
A TX INHIBIT
7 A RX
10 A RX-L
22 A TX OUT
23 A TX OUT-L
B-BUS
B RCVR STROBE
B DIRECT
B XFMR COUPLED
B CT
B XFMR COUPLED
B DIRECT
-15 VDC
+15 VDC
T2
BUS-
25679
U8
BUS
63115
B TX INHIBIT
7 B RX
10 B RX-L
22 B TX OUT
23 B TX OUT-L
OSC
16 MHZ
+5V
GND
U5
U6
7407
U4
74LS123
SEND DATA-L
BYTE OUT-L
BYTE IN-L
16 MHZ

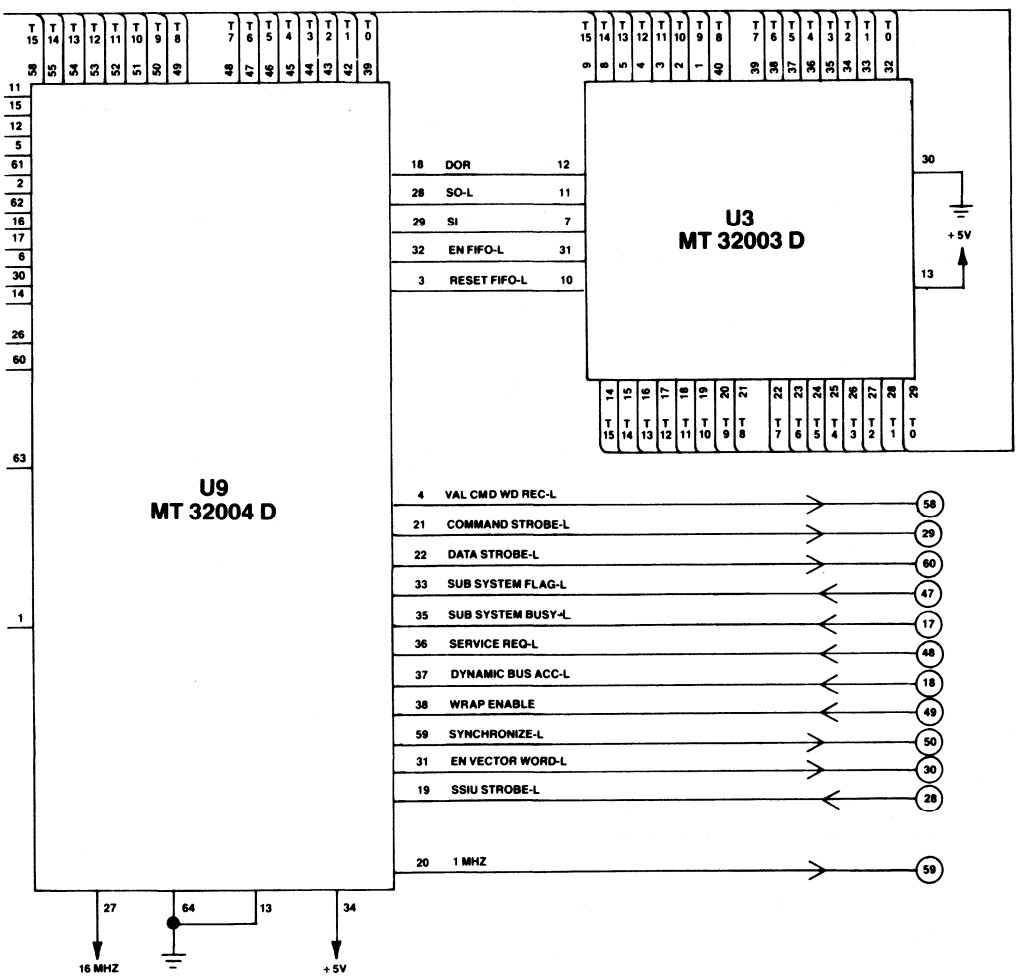
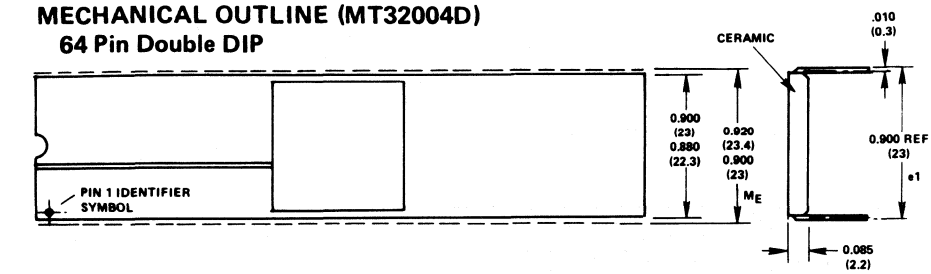
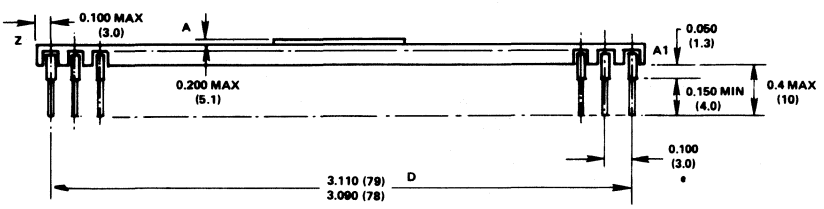


TABLE
EN = ENABLE
-L = LOW OR DATA BAR
T = TRI-STATE I/O

FIGURE 8.
DDC DUAL REDUNDANT RTU
EVALUATION BOARD
(BUS-65400)

MECHANICAL OUTLINE (MT32004D)
64 Pin Double DIP



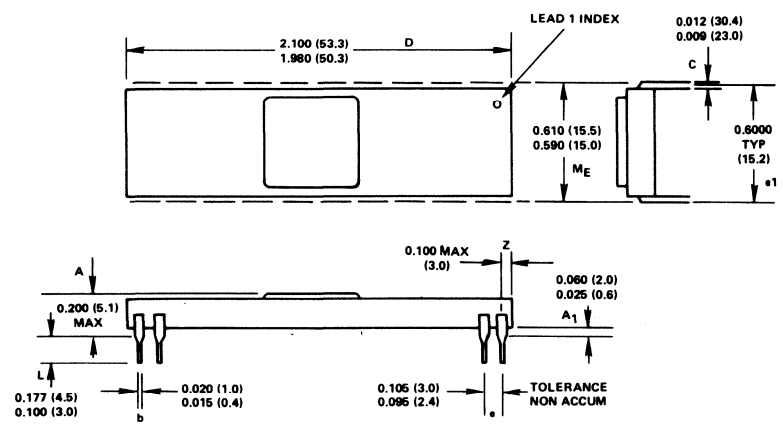


NOTES:
1. Dimensions in inches (millimeters).
2. Refer to BUS-65400 Mechanical Outline for orientation on P.C. Card.

PIN FUNCTION TABLE (MT32004D)

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{BIT IN}}$	33	$\overline{\text{SUB SYSTEM FLAG}}$
2	$\overline{\text{LOAD BUFFER}}$	34	$\overline{\text{VDD}}$
3	$\overline{\text{RESET FIFO}}$	35	$\overline{\text{SUBSYSTEM BUSY}}$
4	$\overline{\text{VAL CMD WD REC}}$	36	$\overline{\text{SERVICE REQUEST}}$
5	$\overline{\text{CMD SYNC}}$	37	$\overline{\text{DYNAMIC BUS ACCEPTANCE}}$
6	$\overline{\text{THIS RT}}$		
7	NC	38	WRAP AROUND
8	NC	39	T0
9	NC	40	NC
10	$\overline{\text{NC}}$	41	NC
11	$\overline{\text{BC DETECT}}$	42	T1
12	$\overline{\text{VALID WORD}}$	43	T2
13	THIS RT ADDR IP MS	44	T3
14	$\overline{\text{THIS RT ADDR IP LS}}$	45	T4
15	$\overline{\text{ANOTHER WORD}}$	46	T5
16	$\overline{\text{SEND DATA}}$	47	T6
17	$\overline{\text{BUFFER FULL}}$	48	T7
18	$\overline{\text{DOR}}$	49	T8
19	$\overline{\text{SSIUSTRB}}$	50	T9
20	$\overline{\text{1 MHz}}$	51	T10
21	$\overline{\text{CMD STRB}}$	52	T11
22	$\overline{\text{DATA STRB}}$	53	T12
23	NC	54	T13
24	NC	55	T14
25	$\overline{\text{NC}}$	56	NC
26	$\overline{\text{RESET}}$	57	NC
27	$\overline{\text{16 MHz}}$	58	$\overline{\text{T15}}$
28	$\overline{\text{SO}}$	59	$\overline{\text{SYNCHRONIZE}}$
29	$\overline{\text{SI}}$	60	TX INHIBIT
30	$\overline{\text{EN IP BUFFER}}$	61	SEL TX DIS
31	$\overline{\text{EN VECTOR WORD}}$	62	$\overline{\text{SEL TX EN}}$
32	$\overline{\text{ENFIFO}}$	63	$\overline{\text{BITE OUT}}$
		64	VSS

MECHANICAL OUTLINE (MT32003D)
40 PIN DOUBLE DIP

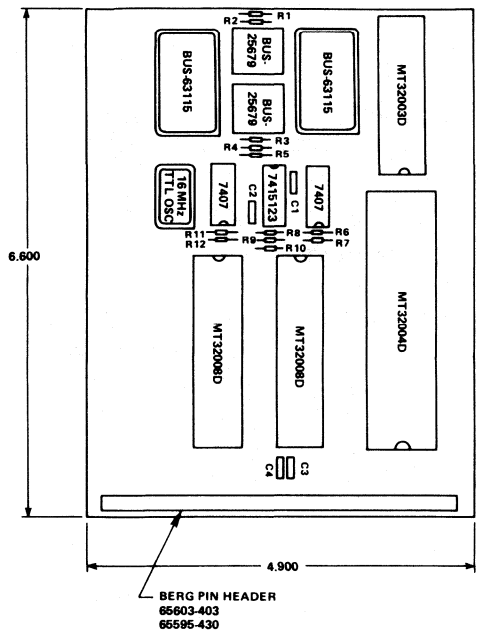


NOTES:
1. Dimensions in inches (millimeters).
2. Refer to BUS-65400 Mechanical Outline for orientation on P.C. Card.

PIN FUNCTION TABLE (MT32003)

PIN	FUNCTION	PIN	FUNCTION
1	D9	21	Q8
2	D10	22	Q7
3	D11	23	Q6
4	D12	24	Q5
5	D13	25	Q4
6	DIR	26	Q3
7	SI	27	Q2
8	D14	28	Q1
9	D15	29	Q0
10	$\overline{\text{RESET}}$	30	$\overline{\text{VSS}}$
11	$\overline{\text{SO}}$	31	ENABLE
12	DOR	32	D0
13	VDD	33	D1
14	Q15	34	D2
15	Q14	35	D3
16	Q13	36	D4
17	Q12	37	D5
18	Q11	38	D6
19	Q10	39	D7
20	Q9	40	D8

MECHANICAL OUTLINE (BUS-65400)

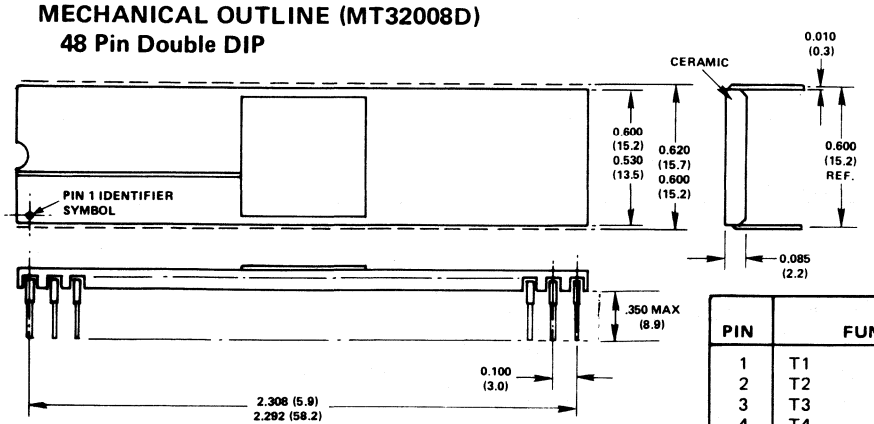


PIN FUNCTION TABLE (BUS-65400)

PIN	FUNCTION	LOADING TTL	PIN	FUNCTION	LOADING TTL
1			31		
2			32	B RCVR	1
3			33	P	1
4	A LSB	1	34	B	1
5	C	1	35	D	1
6	E (MSB)	1	36	A DIRECT	
7	A DIRECT		37	A XFMR COUPLED	
8	A CT		38	A XFMR COUPLED	
9	+15 VDC		39	−15 VDC	
10	B XFMR COUPLED		40	B CT	
11	B XFMR COUPLED		41	B DIRECT	
12	B DIRECT		42	A RCVR STROBE	1
13	+5V		43	+5V	
14	+5V		44	+5V	
15	GND		45	GND	
16	GND		46	GND	
17	SUBSYSTEM BUSY	1	47	SUBSYSTEM FLAG	1
18	DYNAMIC BUS ACC	1	48	SERVICE REQ	1
19	T0 LSB	1-2	49	WRAP ENABLE	1
20	T15 MSB	1-2	50	SYNCHRONIZE	2
21	T13	1-2	51	T14	1-2
22	T11	1-2	52	T12	1-2
23	T9	1-2	53	T10	1-2
24	T7	1-2	54	T8	1-2
25	T5	1-2	55	T6	1-2
26	T3	1-2	56	T4	1-2
27	T1	1-2	57	T2	1-2
28	SSIU STROBE	1	58	VAL CMND WD REC	2
29	COMMAND STROBE	2	59	1 MHz	2
30	EN VECTOR WORD	2	60	DATA STROBE	2

NOTES:
1. Dimensions in inches.
2. Refer to BUS-65400 Mechanical Outline for orientation on P.C. Card.
3. Mating connector supplied, P/N Berg 65057-002 PV Double row of 30.

MECHANICAL OUTLINE (MT32008D)
48 Pin Double DIP



NOTES:
1. Dimensions in inches (millimeters)
2. Refer to BUS-65400 mechanical outline for orientation on P.C. Card.

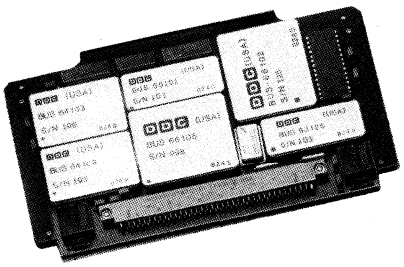
PIN FUNCTION TABLE (MT32008)

PIN	FUNCTION	TYPE I/O	PIN	FUNCTION	TYPE I/O
1	T1	E	25	T10	E
2	T2	E	26	T11	E
3	T3	E	27	T12	E
4	T4	E	28	T13	E
5	T5	E	29	T14	E
6	T6	E	30	T15	E
7	T7	E	31	TERM ADDR E	B
8	RESET	A	32	TERM ADDR D	B
9	LOAD BUFFER	A	33	TERM ADDR C	B
10	BUFFER FULL	D	34	TERM ADDR B	B
11	SEL EN	C	35	TERM ADDR A	B
12	SEND DATA	A	36	CMD/STAT SYNC	D
13	TX OUT	C	37	ANOTHER WORD	D
14	TX OUT	D	38	BC DETECT	D
15	TX INHIBIT	D	39	THIS RT	D
16	TX INHIBIT	C	40	ADDR PARITY	B
17	THIS RT ADDR LS	A	41	RXIN	A
18	RX/TX	B	42	RXIN	A
19	DATA SYNC IN	B	43	16 MHz	A
20	THIS RT ADDR IP LS	E	44	VALID WORD	D
21	EN IP BUFFER	A	45	SEL TX EN	A
22	VSS		46	SEL TX DIS	A
23	T8	E	47	VDD	
24	T9	E	48	T0	E

ORDERING INFORMATION
ORDER: BUS-65400

ILC DATA DEVICE CORPORATION

MIL-STD-1553 DUAL REDUNDANT REMOTE TERMINAL UNIT (RTU)



DESCRIPTION

The BUS-65401 is a complete dual redundant MIL-STD-1553 Remote Terminal Unit (RTU), including protocol and dual port memory subsystem interface. Consisting of a set of hybrids packaged on a small 4" x 7" printed circuit card, the BUS-65401 serves as a complete intelligent interface between a 1553 serial MUX data bus and a subsystem tri-state data highway. It is flexible and easy to use since it appears to the subsystem as a 256 word memory mapped I/O. Furthermore, the internal memory is dual redundant and double buffered, so the subsystem is assured immediate access to the RTU with the certainty that transferred data blocks are all from the same message.

The BUS-65401 is implemented with DDC standard product hybrids. The set includes: a BUS-63125 dual transceiver hybrid; two BUS-64103 encoder/decoder hybrids; a BUS-66101 and BUS-66102 RTU protocol hybrid; and a BUS-66105 dual port memory hybrid. These hybrids, along with two BUS-25679 transformers, a crystal oscillator, and three ROMs, complete the BUS-65401. All RTU protocol, as well as memory management and built-in test, are performed without subsystem intervention. Consequently, the BUS-65401 needs only a minimum of subsystem overhead to manage its RTU function. The BUS-65401 is available screened to MIL-STD-883B and it operates over the full −55°C to +125°C temperature range.

FEATURES

- *COMPLETE MIL-STD-1553 INTELLIGENT REMOTE TERMINAL*
- *1 K x 8 BIT DUAL PORT MEMORY I/O*
- *COMPLETE RTU PROTOCOL:*
  ADDRESS RECOGNITION
  MANCHESTER VALIDATION
  BIT COUNT AND PARITY
  WORD COUNT
  MODE CODE RESPONSE
- *WRAPAROUND BUILT-IN TEST*
- *SMALL SIZE: 4" x 7" PC CARD*
- *−55°C TO +125°C OPERATING TEMPERATURE RANGE*

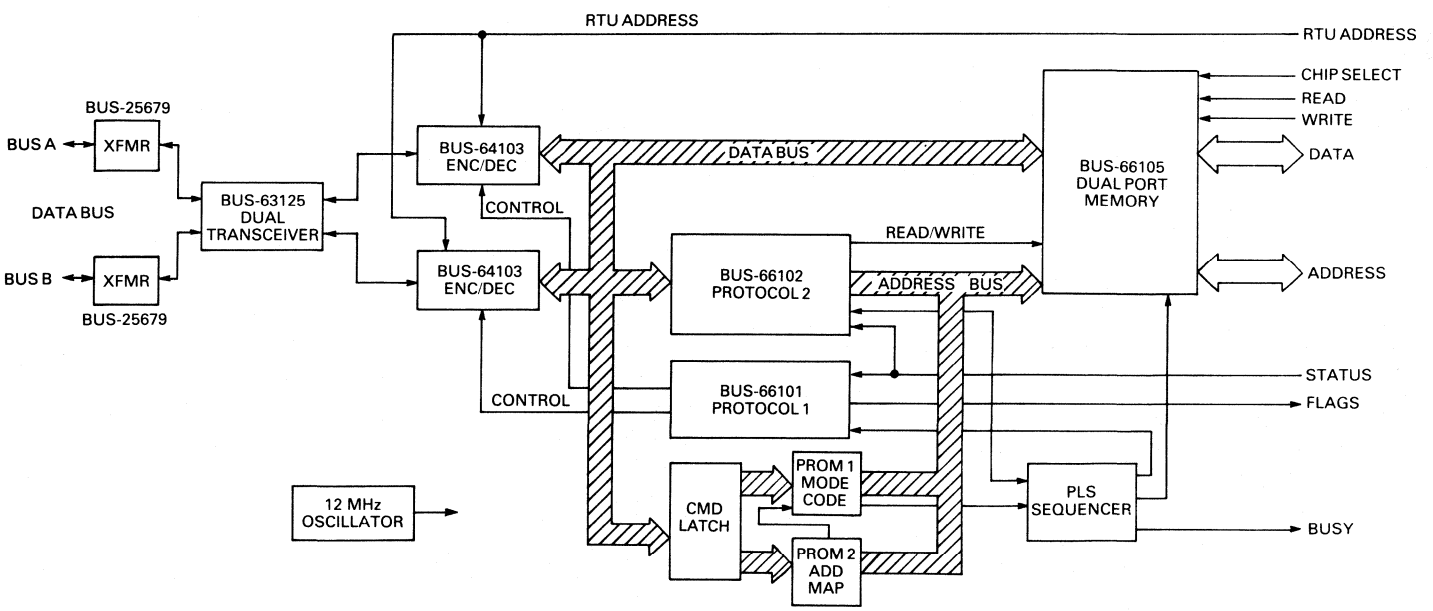


FIGURE 1. BUS-65401 BLOCK DIAGRAM

SPECIFICATIONS – Values at nominal power supply voltages.		
PARAMETER	**UNITS**	**VALUE**
LOGIC		
I_{IH}, I_{IL}, I_{OH}, I_{OL}		See pin function & loading table.
V_{OH}	V	2.5 min
V_{OL}	V	0.4 max
V_{IH}	V	2.5 min
V_{IL}	V	0.4 max
POWER SUPPLIES		
+5V Supply		
Voltage Tolerance	%	10
Current Drain	mA	1500 max
+15V Supply		
Voltage Tolerance	%	5
Current Drain	mA	100 max
−15V Supply		
Voltage Tolerance	%	5
Current Drain		
Idle	mA	100 max
25% Transmit	mA	140 max
100% Transmit	mA	270 max
TEMPERATURE RANGE (Case)		
Operating	°C	−55 to +125
Storage	°C	−65 to +150
PHYSICAL		
Size	in.	3.96 x 7.01 x0.35 max
	cm	10.06 x 17.81 x.89 max
Weight	oz (gm)	10 (283.29)

GENERAL

The BUS-65401 is a MIL-STD-1553B Dual Redundant Remote Terminal Unit (RTU) Printed Circuit Board (PCB) Assembly. It is manufactured from standard off-the-shelf DDC Hybrids and Pulse Transformers, specifically: BUS-25679 Transformers; BUS-64103 Manchester II Converters; BUS-66101 Protocol 1; BUS-66102 Protocol 2 (includes State Sequencer and PROMS); and the BUS-66105 Dual Access Memory Hybrid. The supplied 12 MHz Hybrid Crystal Clock Oscillator offers a 0.01% frequency stability over the full MIL-temperature range.

Figure 1 is the BUS-65401 block diagram. It is recommended that you refer to the separate hybrid data sheets for detailed information on each, especially the BUS-66101 and BUS-66102 Protocol Hybrids. These two devices, along with the State Sequencer and External Latch and PROMs, provide the BUS-65401 RTU with a number of special features resulting in a great deal of system flexibility. These features, such as Mode Code Selection, Subaddress Field Memory Mapping, Built-In Test and Wraparound operation, will be described below.

The BUS-65401 RTU complies fully with MIL-STD-1553B, supporting the following four transfer formats:

(1) Controller to RT Transfer
(2) RT to Controller Transfer
(3) RT to RT Transfer
(4) Mode Command without Data Word

TABLE 1. COMMANDS (HEXADECIMAL)

BLOCK	TYPE	ADDRESS	T/R	SUB-ADDRESS	WORD COUNTS (REF ONLY)
2	TX CMD	RTU	T	10001	1 through 32
3	RCV CMD	RTU	R	10010	1 through 32
7	TX WRAPARND	RTU	T	11110	1 through 32
1	TX CMD	RTU	T	10000	1 through 32

TABLE 2. MODE COMMANDS

MSC ID	ADDRESS	T/R	SUB-ADDRESS	MODE
TX STS WD	RTU	T	11111 or 00000	00010
TX SHUT DWN	RTU	T	11111 or 00000	00100
OVRID TX SHUT DWN	RTU	T	11111 or 00000	00101
RESET REMT TERML	RTU	T	11111 or 00000	01000
INITIATE SELF TEST	RTU	T	11111 or 00000	00011
SYNCHRONIZE*	RTU	T	11111 or 00000	00001
*Optional				

In addition, the RTU has the capacity to validate all Mode Commands used as well as those commands with an associated Data Word. The RTU will verify the presence, validity and continuity of the message.

The BUS-65401 will respond to receive or transmit commands with subaddress, and T/R bit combinations, as specified in Table 1. All other combinations, apart from those specified in Table 1, are considered illegal.

The P1 and P2 PROMs determine the illegality of a command received by the RTU. They also can be programmed to illegalize or add other Mode Commands. (See Table 2.)

Table 1 shows how the RTU protocol partitions memory into receive and transmit blocks. The only unique item is the wraparound buffer which is reserved for the Subaddress (11110) for either a Transmit or Receive (T/R) Bit. The Bus Controller and RTU host CPU can access this buffer for dynamic system testing.

MODE CODES

The BUS-65401 RTU will respond to the Mode Commands from the Bus Controller, as listed in Table 2. Detailed explanations of each command follow:

Transmit Status Word. On receipt of this Mode Command, the RTU will not reset the bits in the Status Word but will transmit a Status Word with bits set as they apply to the most recent message other than a Transmit Status Word Mode Command.

Transmitter Shutdown. On receipt of this Mode Command, the RTU will disable the output of the transmitter associated with the redundant data bus. Thus, if the command arrives on Bus A, the Bus B transmitter will be disabled; or, if the command arrives on Bus B, the Bus A transmitter will be disabled.

Reset Remote Terminal. This Mode Command causes the terminal to be placed in its power-up state, enabling both transmitters.

Override Transmitter Shutdown. On receipt of this Mode Command, the RTU enables the output of the transmitter associated with the redundant data bus. Thus, if the command arrives on Bus A, the Bus B transmitter will be enabled; or, if the command arrives on Bus B, the Bus A transmitter will be enabled.

Initiate Self Test. Receipt of an Initiate Self Test Mode Command will result in no RTU action other than the transmission of the Status Word per MIL-STD-1553B.

Illegal Commands. Illegal Commands include those valid commands with Illegal Subaddress and T/R combinations, and those requesting unimplemented Mode Action. The response of the RTU to an Illegal Command, followed by the correct number of contiguous valid Data Words is to set the Message Error Bit in the Status Word and transmit the Status Word. The Message Error Bit will remain set until reset by conditions described in the Message Error Bit Section.

Invalid Commands. Invalid Commands include those with invalid sync pattern, parity or Manchester waveform. The RTU takes no action on receipt of an invalid command.

Partially Updated Data. Through a double buffer feature, the RTU ensures that partially updated data blocks are not transmitted.

STATUS WORD IMPLEMENTATION

The RTU stores internally the Status Word described in MIL-STD-1553. The individual bits are implemented as specified in Table 3.

The Message Error Bit will be set to 1 in the following cases:

(1) When one or more Data Words following a Valid Receive Command are found Invalid; the wrong number of data words is present; or, the Data Words and Command Word are not contiguous.

(2) When one or more Data Words follow a Transmit Command.

(3) When one or more Data Words following the Status Word transmitted by the Transmitting Terminal in a Terminal-To-Terminal transfer are Invalid, or when the number of Data Words is incorrect.

(4) When a Data Word following a Mode Command is Invalid or when the wrong number of Data Words is present.

TABLE 3. RTU STATUS REGISTER

BIT	USE	IMPLEMENTATION
1-3	Sync	Hardware generated by the RTU.
4-8	Remote Terminal Address	Hardware loaded from discrete bit inputs.
9	Message Error	Hardware sets to 1.
10	Instrumentation Bit	Always set by hardware to 0.
11	Service Request	
12-15	Reserved	
16	Busy	
17	Subsystem Flag	Loaded from the subsystem Fail Input line.
18	Dynamic Bus Control	Always set by hardware to 0.
19	Terminal Flag	Loaded by hardware according to result of built-in test.
20	Parity	Hardware generated.

Refer to the BUS-66102 hybrid data sheet for more detail.

(5) When an Illegal but valid command is received.

(6) When an RT-to-RT time-out occurs.

The BUS-65401 RTU will transmit a Status Word in 10μs following each valid message received. Transmission of the Status Word will be suppressed in cases 1-6, above.

REMOTE TERMINAL-TO-REMOTE TERMINAL TIMEOUT

If the Remote Terminal gets a valid Receive Command, and the first Data Word has not been received within a fixed time, T (between 54 and 60 μs), the Remote Terminal will reset itself, set the Message Error Bit in the Status Word, and suppress its status response. The time is measured from the mid-bit zero crossing of the first expected Data Words, as shown in Figure 8 of MIL-STD-1553B.

BUILT-IN TEST FUNCTION

The BUS-65401 carries out a wraparound built-in test (BIT) in that it receives the last word of each of its transmitted messages. This test actually occurs in the active BUS-64103 Manchester II Converter. When the data comparison doesn't match, a Fault Flag is generated and latched in the BUS-66102 Fault Register. Once set, the RTU FAIL line will be taken HIGH, and will remain there until the subsystem provides a LOW on the RT FL RST line.

The Condition Latch and the RTU FAIL line will be inhibited due to a BIT failure on a bus on which the transmitter has been shut down by Mode action. In this case, BIT functions normally on the bus which has not been shut down.

SUBSYSTEM INTERFACE

The BUS-65401 Subsystem Interface consists of a 1024 x 8 bit dual access memory RAM internal to the BUS-66105 hybrid. This interface supports the Multibus 8086 Intel Microcomputer (CPU), using 8 bit byte transfers. (Refer to the BUS-66105 detailed data sheet.)

The data sheet describes fully how the blocks in RAM are allocated, and how the CPU selects the current and noncurrent data areas via the Switch Register. (See Table 4.) In this case, the A10 address line goes HIGH selecting the Buffer Switch Register. The CPU then designates Message Block areas A or B for each Command Word's subaddress. Once selected, areas A or B are automatically maintained by the RTU for Receive or Transmit Commands and associated data. The CPU reads the Buffer Selected Register at all times and changes this register by reloading with the A10 line enable. The newly defined Block Areas will not be updated until the RTU transfers have been completed. This shift is enabled by the $\overline{\text{IDLE}}$ signal from the 1553 RTU.

TABLE 4. MEMORY MAP IN HEXADECIMAL

BUFFER ADDRESS	CPU ADDRESS	USAGE
000 to 03F	000-07F	Receive control word, Area A
200 to 23F	000-07F	Receive control word, Area B
040 to 07F	080-0FF	Block 1 TX Message, Area A
240 to 27F	080-0FF	Block 1 TX Message, Area B
080 to 0BF	100-17F	Block 2 TX Message, Area A
280 to 2BF	100-17F	Block 2 TX Message, Area B
0C0 to 0FF	180-1FF	Block 3 RX Message, Area A
200 to 2FF	180-1FF	Block 3 RX Message, Area B
100 to 13F	200-27F	Block 4 Spare Buffer 1A
300 to 33F	200-27F	Block 4 Spare Buffer 1B
140 to 17F	280-2FF	Block 5 Spare Buffer 2A
340 to 37F	280-2FF	Block 5 Spare Buffer 2B
180 to 1BF	300-37F	Block 6 Spare Buffer 3A
380 to 3BF	300-37F	Block 6 Spare Buffer 3B
1C0 to 1FF	380-3FF	Block 7 Wraparound A
3C0 to 3FF	380-3FF	Block 7 Wraparound B

The bits in the Buffer Selected Register relate to the blocks within the buffer RAM, as follows:

DB0 (LSB)	Bit 0	Receive control word area
DB1	Bit 1	Block 1
DB2	Bit 2	Block 2
DB3	Bit 3	Block 3
DB4	Bit 4	Block 4
DB5	Bit 5	Block 5
DB6	Bit 6	Block 6
DB7 (MSB)	Bit 7	Block 7 (Wraparound)

Note: A Logic 0 selects buffer Area A.
A Logic 1 selects buffer Area B.

The Receive Command Word Buffer areas A and B are reserved for RAM locations 000 through 03F, and 200 through 23F, respectively. Each area is divided into 32 word sections with each section dedicated to a subaddress. (Refer to DDC BUS-66101 and BUS-66102 combined data sheet for PROM detail.) The assigned locations within the Receive Command Word Buffer correspond to the buffer RAM data areas, as follows:

	RAM ADDRESS IN HEXADECIMAL	
DATA AREA	BUFFER A (8 Bit MSB) (8Bit LSB)	BUFFER B MSB LSB
Block 1	002 and 003	202 and 203
Block 2	004 and 005	204 and 205
Block 3	006 and 007	206 and 207
Block 4	008 and 009	208 and 209
Block 5	00A and 00B	20A and 20B
Block 6	00C and 00D	20C and 20D
Block 7	00E and 00F	20E and 20F

When a valid Command Word is received, it is loaded into the Receive Command Word Buffer, Area A or B, as determined by the Buffer Selected Register contents. Since it is not mandatory that the RTU Address Field be loaded into RAM, the BUS-66105 uses this area for special Status flags.

The Message Transferred and the Message Error Flags are set to a logic "0" when a valid Command Word is placed into RAM. The Message Error Flag is reset to logic "0" if the message transfer is completed without errors. The $\overline{\text{END}}$ signal generated by the 1553 RTU denotes the completion of the 1553 message transfer. The Message Error Flag prevents the CPU from accessing a data block, which may contain errors or simply be in the process of being updated. If there was a Message Format Error or Data Word Error, this bit will remain HIGH.

The CPU clears the Message Transferred Flag, allowing the CPU to keep tabs on current Message Block Transfers.

The Receive Command Word Area, Buffer A or B, is organized as follows:

Odd Byte		Even Byte	
Bit 7	Message Transferred Flag	Bit 7	Subaddress Bit 2
Bit 6	Message Error Flag	Bit 6	Subaddress Bit 1
Bit 5		Bit 5	Subaddress Bit 0
Bit 4	Spare	Bit 4	Word Count Bit 4
Bit 3		Bit 3	Word Count Bit 3
Bit 2	T/R Bit	Bit 2	Word Count Bit 2
Bit 1	Subaddress Bit 4	Bit 1	Word Count Bit 1
Bit 0	Subaddress Bit 3	Bit 0	Word Count Bit 0

Bits 0 through 7 of the Even Byte, and bits 0 through 2 of the Odd Byte, contain the subaddress, T/R bit and word count of the valid Command Word received.

Although the 8086 CPU always has read and write access to the whole noncurrent area of the buffer RAM, a contention conflict will occur if the CPU attempts to access the RAM when the 1553 RTU is transferring data in or out. This problem is resolved, as follows:

When the CPU writes into RAM, the address and data are loaded into the Address Register and Input Register, respectively. The internal control logic transfers the data to the correct location in RAM, always within 1.8μs from the end of the CPU write cycle ($\overline{\text{MWTC}}$); or read cycle ($\overline{\text{MRDC}}$) trailing edge.

When the CPU reads from RAM, it actually receives the data held in the Output Register. Since the Output Register data is always associated with the previous read operation, the effect of this is that reading a block of words from RAM requires one additional read operation.

The CPU write cycle begins when the $\overline{\text{CS3M}}$ (chip select) line followed by the $\overline{\text{MWTC}}$ (write) line becomes active (LOW). The D0-D7 parallel data and A1-A10 address highway must be valid at the trailing edge of $\overline{\text{MWTC}}$ and held valid for 40ns, min. The $\overline{\text{RTU ACCESS}}$ input signal should never be activated when $\overline{\text{CPU ACCESS}}$ output is LOW. (See Figure 2.) This sequence must be repeated in 1.8 μs min. to write in the LSB byte. The 1.8 μs interval ensures that the RTU has the necessary RAM access time. Figure 2 also shows that data loaded into the Input Register by the CPU is transferred to RAM upon completion of $\overline{\text{RTU ACCESS}}$.

The CPU read cycle is similar to the write cycle except $\overline{\text{MRDC}}$ (read) input signal must be valid. Note that data shifted out on the D0-D7 highway lags each $\overline{\text{MRDC}}$ (read) cycle by 1.

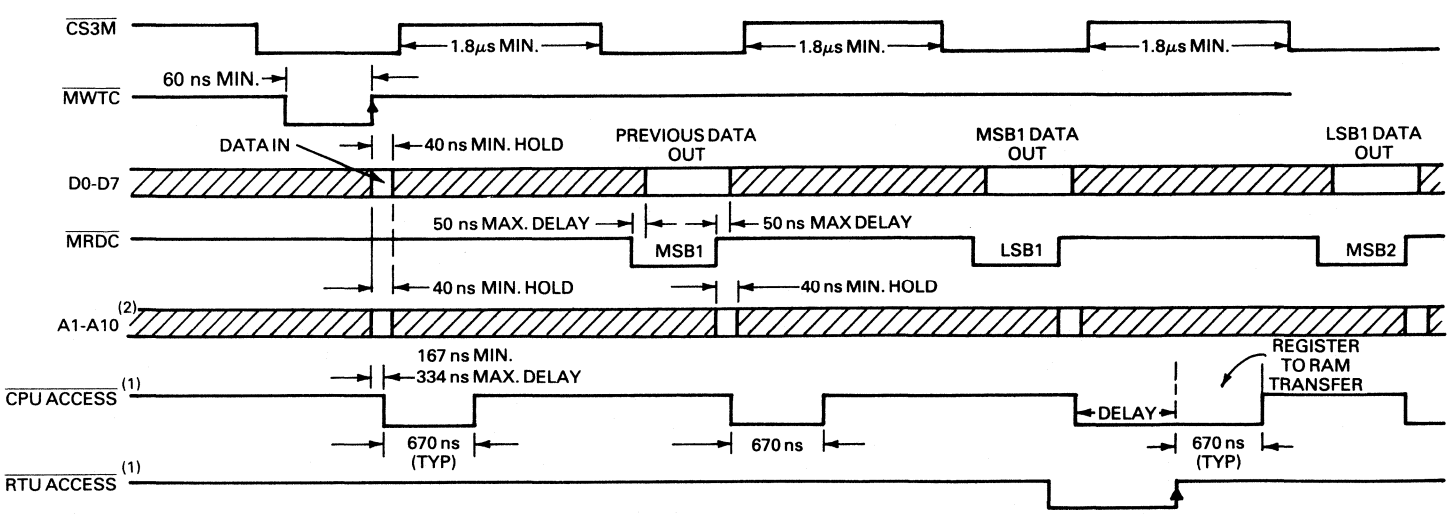
Address Lines. From the CPU, 10 address lines (A1 through A10) provide inputs to the BUS-65401. A1 is the least significant.

Data Lines. There are eight bidirectional parallel data lines (D0 through D7). D0 is the least significant.

Control Lines.

$\overline{\text{ACS3M}}$	Active LOW to indicate selection of the card for a read or write operation. The edges of this signal shall not be used for timing purposes.
$\overline{\text{MRDC}}$	Active LOW to indicate a read operation is to be performed.
$\overline{\text{MWTC}}$	Active LOW to indicate a write operation is to be performed.

All connections to the 1553 Interface and Buffer Board are handled through a 70 pin connector, MIL Part No. 55302/57-A70Y. (See Pin Function and Loading Table.)



Notes: (1) $\overline{\text{CPU ACCESS}}$ and $\overline{\text{RTU ACCESS}}$ signals represent data moving "in" or "out" of the RAM. $\overline{\text{RTU ACCESS}}$ should never be activated when $\overline{\text{CPU ACCESS}}$ output is active
(2) A10 selects the Buffer Switch Register when HIGH. When LOW, the input and output registers for accessing RAM are selected.

FIGURE 2. BUS-65401 TIMING

BUS-65401 PIN FUNCTION AND LOADING TABLE

PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
1	GND					Ground.
2	+5V					+5V D.C. power supply input.
3	NC					No connection.
4	$\overline{\text{TBUSY}}$			−0.4	4.0	A LOW on this output indicates that the RTU is transmitting.
5	A1	20	−0.4			(LSB) 10 bit address bus.
6	A3	20	−0.4			10 bit address bus.
7	A5	20	−0.4			10 bit address bus.
8	A7	20	−0.4			10 bit address bus.
9	A9	40	−0.8			10 bit address bus.
10	NC					No connection.
11	CTAP A					1553 Bus A BUS-25679 transformer (Pin 6) center tap.
12	TRANS POS B					1553 Bus B BUS-25679 transformer (Pin 7) positive tap.
13	TRANS NEG B					1553 Bus B BUS-25679 transformer (Pin 5) negative tap.
14	DIR POS B					1553 Bus B BUS-25679 & 55Ω positive direct coupled tap.
15	$\overline{\text{MWTC}}$	40	−0.8			An active LOW indicates the CPU is to perform a write operation.
16	DIR NEG B					1553 Bus B BUS-25679 & 55Ω negative direct coupled tap.
17	$\overline{\text{CS3M}}$	40	−0.8			An active LOW input indicates the CPU is performing a read or write operation. This signal should not be used for timing purposes.
18	RTU ADDR 1	40	−0.8			RTU Address bit (hard wired).
19	RTU ADDR 3	40	−0.8			RTU Address bit (hard wired).
20	NC					No connection.
21	NC					No connection.
22	GND					RTU System ground.
23	CPU READY	40	−0.8			Transceiver receiver strobe signal; an active HIGH enables Channels A & B receiver.
24	DATA REC			−0.4	4.0	A HIGH on this output indicates that the DATA REC register has been set by $\overline{\text{EOM}}$ input.
25	$\overline{\text{RT PRESENT}}$					Grounded J1 pin, used to indicate presence of RTU.
26	NC					No connection.
27	NC					No connection.
28	NC					No connection.
29	NC					No connection.
30	D7	40	−0.8	−13	24	(MSB) Tri-state 8 bit parallel data I/O.
31	D5	40	−0.8	−13	24	Tri-state 8 bit parallel data I/O.
32	D3	40	−0.8	−13	24	Tri-state 8 bit parallel data I/O.
33	D1	40	−0.8	−13	24	Tri-state 8 bit parallel data I/O.
34	+5V					+5V D.C. power supply input.
35	GND					System ground.
36	GND					System ground.

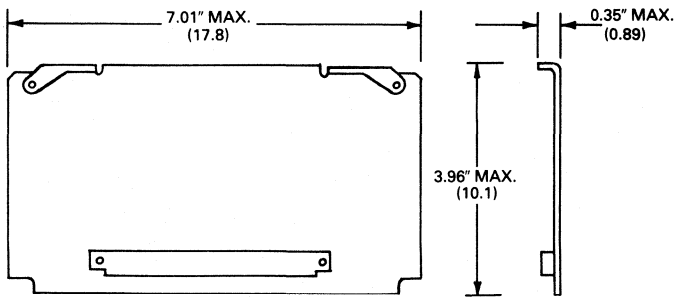
BUS-65401 PIN FUNCTION AND LOADING TABLE (CONTINUED)

PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
37	+5V					+5V DC power supply input.
38	NC					No connection.
39	NC					No connection.
40	A2	20	−0.4			10 bit address bus.
41	A4	20	−0.4			10 bit address bus.
42	A6	20	−0.4			10 bit address bus.
43	A8	20	−0.4			10 bit address bus.
44	A10	40	−0.8			10 bit address bus. This input, A10 bit, selects data transfer from the dual access memory hybrid's (BUS-66105) buffer switch and buffer select registers when HIGH. If A10 is LOW, data is being transferred to memory.
45	TRANS POS A					1553 Bus A BUS-25679 (Pin 7) positive tap.
46	TRANS NEG A					1553 Bus A BUS-25679 (Pin 5) negative tap.
47	C TAP B					1553 Bus B BUS-25679 (Pin 6) center tap.
48	RTU FAIL			−0.4	4.0	A HIGH level on this output indicates a fault condition occurred during the last RTU transmission while in the normal wraparound mode.
49	$\overline{\text{MRDC}}$	40	−0.8			An active LOW input indicates the CPU is to perform a read operation.
50	DIR POS A					1553 Bus A, BUS-25679 & 55Ω, direct positive coupled tap.
51	DIR NEG A					1553 Bus A, BUS-25679 & 55Ω, direct negative coupled tap.
52	RTU ADDR 0	60	−1.2			(LSB) RTU Address bit (hard wired).
53	RTU ADDR 2	40	−0.8			RTU Address bit (hard wired).
54	RTU ADDR 4	40	−0.8			(MSB) RTU Address bit (hard wired).
55	$\overline{\text{RT FL RST}}$	20	−0.4			A LOW level input (0.1 μs min.) resets the RTU fail logic register.
56	+15V					+15V DC power supply input.
57	−15V					−15V DC power supply input.
58	$\overline{\text{SS FAIL}}$	20	−0.4			$\overline{\text{SUBSYSTEM FLAG}}$, a HIGH level external input sets bit 17 in the status word register.
59	$\overline{\text{RT RC RST}}$	20	−0.4			A LOW level input (0.1 μs min.) resets the data rec logic register in BUS-66101.
60	$\overline{\text{RESET}}$	120	−1.6			A LOW level input (0.1 μs min.) resets the RTU for power-up or fault detection situations.
61	NC					No connection.
62	NC					No connection.
63	NC					No connection.
64	NC					No connection.
65	D6	40	−0.8	−13	24	Tri-state 8 bit parallel data highway.
66	D4	40	−0.8	−13	24	Tri-state 8 bit parallel data highway.
67	D2	40	−0.8	−13	24	Tri-state 8 bit parallel data highway.
68	D0	40	−0.8	−13	24	(LSB) Tri-state 8 bit parallel data highway.
69	+5V					+5V DC power supply input.
70	GND					Ground

NOTES: In the above table, the symbols are defined as follows:
I_{IH}=maximum input HIGH current with V_{in}=2.5 volts.
I_{IL}=maximum input LOW current with V_{in}=0.4 volts.
I_{OH}=maximum output HIGH current with V_{out}=2.5 volts minimum.
I_{OL}=maximum output LOW current with V_{out}=0.4 volts maximum.

MECHANICAL OUTLINE
BUS-65401

Dimensions shown in inches (centimeters)

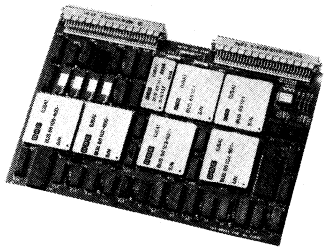


Mating Connector: M55302/58-A70Y

ORDERING INFORMATION

BUS-65401-883B

MIL-STD-883 Processing:
883B = Conforms to MIL-STD-883 DDC Procedures
Blank = Same, except burn-in is omitted



MIL-STD-1553 BUS CONTROLLER AND REMOTE TERMINAL UNIT

DESCRIPTION

The BUS-65500 is a dual redundant MIL-STD-1553 Bus Controller (BC) and Remote Terminal Unit (RTU) with a VME interface. It is packaged on a small 6.3 x 9.2 inch double Eurocard, and provides complete intelligent BC/RTU interface between a 1553 serial MUX data bus and a parallel VME bus. It is fully compliant with MIL-STD-1553, supports all message formats, implements 11 mode codes and provides a complete wraparound built-in test capability.

The BUS-65500 is flexible and easy to use, and appears to the subsystem VME bus as programmed I/O. Its 4K x 16 bit Dual Port RAM and four types of subsystem interrupts minimize the amount of user overhead required to support BC or RTU operation. BUS-65500 contains six VME command registers which allow the subsystem to configure its operation under software control. As a Bus Controller, it can store and process up to 62 messages of 64 words without subsystem intervention. As an RTU, it can store and respond to 119 messages of 32 words with no subsystem intervention.

MIL-STD-1553 related functions, such as address recognition, Manchester coding validation, bit count, parity, word count, and mode code response are all provided by BUS-65500 transparent to the user subsystem. It operates over the full −55°C to +125°C temperature range and is available screened to MIL-STD-883B.

FEATURES

- *COMPLETE DUAL REDUNDANT INTELLIGENT BC/RTU WITH VME INTERFACE*
- *SUPPORTS ALL MIL-STD-1553 MESSAGE FORMATS AND 11 MODE CODES*
- *4K x 16 DUAL PORT RAM STORES:*
  62 BC MESSAGES PLUS ADDRESS STACK AND POINTER
  119 RTU MESSAGES PLUS COMMAND STACK AND POINTER
- *6.3 " x 9.2 " VME EUROCARD*
- *SIX VME COMMAND REGISTERS*
- *FOUR TYPES OF SUBSYSTEM INTERRUPT*
- *WRAPAROUND BUILT-IN TEST*

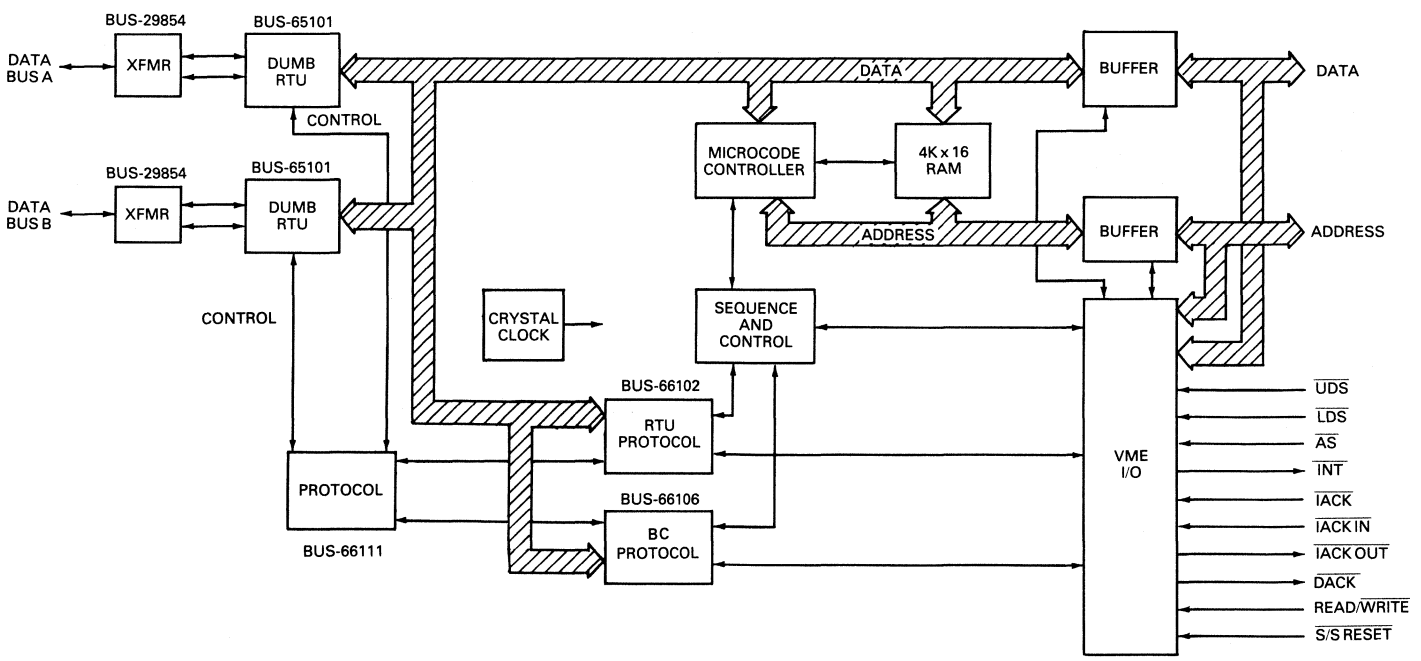


FIGURE 1. BUS-65500 BLOCK DIAGRAM

SPECIFICATIONS–Values at nominal power supply voltages.		
PARAMETER	**UNITS**	**VALUE**
LOGIC		
I_{IH}, I_{IL}, I_{OH}, I_{OL}		See Pin Function & Loading Table.
V_{OH}	V	2.5 min
V_{OL}	V	0.4 max
V_{IH}	V	2.4 min
V_{IL}	V	0.8 max
POWER SUPPLIES		
+5V Supply		
Voltage Tolerance	%	10
Current Drain	A	3.0 max
+15V Supply		
Voltage Tolerance	%	5
Current Drain	mA	300 max
−15V Supply		
Voltage Tolerance	%	5
Current Drain	mA	300 max
TEMPERATURE RANGE (Case)		
Operating	°C	−55 to +125
Storage	°C	−65 to +150
SIZE	in. (mm)	6.3 x 9.2 x 0.44 160 x 234 x 11

GENERAL

The BUS-65500 appears to the subsystem VME bus as programmed I/O. Once its VME Command Registers are loaded, the BUS-65500 functions with a minimum of subsystem intervention. Management and control of the onboard 4K x 16 bit Dual Port RAM is accomplished transparent to the subsystem. Memory address partitioning is flexible, since eight bits of the available 23 address bits are switch programmable. As a Bus Controller, the memory map contains data blocks, a data block address stack, and a data block address pointer. As a Remote Terminal Unit, the memory map contains data blocks, dual command word stacks, command word stack pointers and data block subaddress look-up tables.

The six VME Command Registers contained in the BUS-65500 allow software control of configuration, modes and functions. Subsystem VME Commands used to program the BUS-65500 include: interrupt vector base address, interrupt enable/disable, BC/RTU mode, external status bits, message lengths, and start or stop commands.

MEMORY MAPPING

All the transfers between the subsystem and the VME interface on the BIU are accomplished by treating the BIU as a memory location. Two modes of address are used to achieve this transfer of data between the BIU and the subsystem: Standard Address and Short Address.

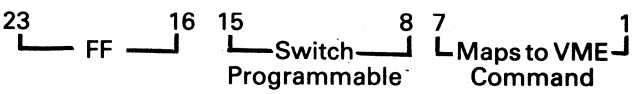
The Standard Address Mode is used to address the 4096 word x 16 bit RAM in the BIU. The Short Address Mode is reserved for the transfer of the VME Command to the BIU.

Two eight bit jumper programmable Address Decoders are provided on the BIU to decode the VME Address Lines. One decoder is used for the Standard Address and the other for the Short Address Mode.

The positions of the bits are as follows:

Standard Address

Short Address



Address Modifiers

The Address Modifiers are programmed in a 256 x 4 PROM. The BIU is supplied with one PROM which accepts Address Modifiers 3D or 39 (when 23 bits of address are used), and Address Modifiers 2D or 29 (when 16 bits of address are used).

NOTE, re: $\overline{\text{DTACK}}$

Normally, $\overline{\text{DTACK}}$ is a 0.5μs MAX pulse unless a valid Command Word received is being processed in the memory, in which case this pulse will be 2.5μs MAX.

VME COMMANDS

The Short Address Mode is used to transfer the VME Commands to the BIU

A Data Word transferred with these addresses contains the specific actions involved with each category of command. These commands, plus their associated addresses are:

Address	Command
FFXX00	NOT USED
FFXX02	INTERRUPT VECTOR ADDRESS
FFXX04	BIU EXTERNAL STATUS LOAD
FFXX04	BIU EXTERNAL STATUS READ
FFXX06	CONTROLLER START
FFXX08	RESET
FFXX0A	NOT USED
FFXX0C	INTERRUPT ENABLE/DISABLE
FFXX0C	INTERRUPT REGISTER READ
FFXX0E	CONTROLLER CONTINUE/STOP

The "XX" in the address field represents user defined jumper selectable address bits.

BIU External Status Load Command (FFXX04)

The External Status Load Command is used to load the operational mode of the BIU together with the four External Status Word bits used when the BIU is operating as an RT. The Data Word associated with this command has the following format:

Bit	
15-8	NOT USED
7	LOGIC "0" – BCIU MODE LOGIC "1" – RT MODE
6	LOGIC "0" – BIU CONTROLLED DOUBLE BUFFERING LOGIC "1" – CPU CONTROLLED DOUBLE BUFFERING

5	LOGIC "0" – CONTROL AREA A TO BE CURRENT TO BIU LOGIC "1" – CONTROL AREA B TO BE CURRENT TO BIU
4	NOT USED
3	DB ACCEPTANCE
2	BUSY
1	SERVICE REQUEST
0	SUBSYSTEM FLAG

Note

A "POWER ON" or "CPU RESET" command resets Bits 0 to 7 in the Data Word above to the logic "0" condition.

BIU External Status Read Command (FFXX04)

The External Status Read Command is used to read the control area previously selected as well as the RT Address Parity Errors for Channels A and B of the 1553 Multiplex Bus. The Data Word associated with this command has the following format:

Bit	
15-8	NOT USED
7	NOT USED
6	NOT USED
5	LOGIC "0" – CONTROL AREA A TO BE CURRENT TO BIU LOGIC "1" – CONTROL AREA B TO BE CURRENT TO BIU
4	NOT USED
3	NOT USED
2	NOT USED
1	B CHANNEL ODD PARITY
0	A CHANNEL ODD PARITY

Interrupt Enable/Disable Command (FFXX0C)

The above Interrupts are enabled/disabled by the Interrupt Enable/Disable command. The Data Word associated with this command enables the interrupt type. The Data Word format is:

Bit	
0	END OF MESSAGE
1	COMMAND RECEIVED
2	STATUS WORD SET OR ADDRESS MISMATCH
3	NOT USED (LOGIC "0")
4	LOOP TEST FAIL
5	TIME OUT
6	1553 FORMAT ERROR
7	NOT USED (LOGIC "0")
8-15	NOT USED

To enable the required interrupt, the corresponding Data Word bit must be a logic "1". To disable the required interrupt, the corresponding Data Word must be a Logic "0".

Interrupt Register Read Command (FFXX0C)

The subsystem issues this command to see what activated the interrupt. The Data Word format associated with this command is:

Bit	
0	END OF MESSAGE
1	COMMAND RECEIVED
2	STATUS WORD SET OR ADDRESS MISMATCH
3	NOT USED (LOGIC "1")
4	LOOP TEST FAIL
5	TIME OUT
6	1553 FORMAT ERROR
7	NOT USED (LOGIC "1")
8-15	NOT USED

Any bit set to logic "1" indicates its associated interrupt was activated.

Whenever an interrupt is acknowledged by the subsystem, further interrupts are inhibited. A Read Error Interrupt Register command clears pending interrupts and reenables the generation of further interrupts. The Read Error Interrupt Register reflects all the interrupt activity regardless of whether the interrupt type is enabled or disabled.

Interrupt Vector Address Command (FFXX02)

This Subsystem command is issued to transfer an 8 bit Interrupt Vector to the BIU. This vector is enabled on D0 to D7 by the BIU in response to an interrupt acknowledge from the Subsystem.

Controller Start Command (FFXX06)

The Subsystem issues this command in the BCIU Mode whenever a 1553 Data Block is available for transmission.

The data word associated with this command contains the number of data blocks ready for transmission:

Bit	
7-0	Message Count: 00000000=1 Message 11111111=256 Messages
15-8	NOT USED

Controller Continue/Stop Command (FFXX0E)

The subsystem issues this command to the BCIU when it wishes the BCIU to resume processing a halted Start Command or to stop the BCIU's predetermined mode of operation at the end of the current Data Block. The format of the Data Word associated with this command is:

Bit	
0	Logic "1" – Continue Logic "0" – Stop
1-15	NOT USED

INTERRUPTS The BIU Interrupt Request Priority is jumper programmable to level 5, 6 or level 7 is the highest priority.

Command Received.

This interrupt is generated when the BIU is operating as a Remote Terminal and when a Command Word is received.

End of Message (EOM) Interrupt. When operating as a BCIU, the BIU is instructed to process a number of 1553 data blocks that have been formatted and placed in the Bus Controller Data Buffer. The BIU generates an EOM Interrupt after all these data blocks have been processed and transmitted over the 1553 Data Bus. When operating

as an RT, the BIU generates an EOM Interrupt at the completion of every 1553 message transfer.

Status Word Set Interrupt. This interrupt is generated when the BIU is operating in the BCIU Mode and whenever the status response from a Remote Terminal contains a bit set to logic "1" in any of the eight bits, or when a wrong RT Address is present.

Error Interrupt. The BIU stops operating at the end of the present data block whenever an error is detected. The Error Interrupt can be caused by a Loop Test Fail, a Time-Out, or by a 1553 Format Error. After this Interrupt is generated, the BCIU starts to process succeeding data blocks upon reception of the Controller Continue command.

Loop Test Fail Interrupt. This Interrupt is generated in the BCIU or RT Mode whenever the last word transmitted over the 1553 Bus did not loop back correctly into the corresponding 1553 Receiver, thus indicating a BIU failure.

Time-Out Interrupt. This interrupt is generated in the BCIU Mode whenever a Timeout occurred as per MIL-STD-1553B.

1553 Format Error Interrupt. This Interrupt is generated in the BIU whenever a fault in word/message format occurs as per MIL-STD-1553B.

BUS CONTROLLER OPERATION

On power up, the BIU assumes the function of a Bus Controller. Another way to revert to this Mode is to use the BIU External Status Load command with Bit 7 set to a logic "0".

BC Memory Allocation

For proper operation, the 4K x 16 Memory must be initialized and loaded by the Subsystem with the proper command and/or data to be transmitted.

The Memory is divided into three areas:

- Data Block Address Stack
- Pointer Area
- Data Blocks

The corresponding addresses to these areas are:

Address	Area
0000 to 007E	Data Block Address Stack
0080 to 00FE	Data Block 60
0100 to 017E	Data Block 61
0180 to 01FE	Data Block 62
0200	BCIU Data Block Addr. Pointer
0201 to 027E	Spares
0280 to 02FE	Data Block 1
0300 to 037E	Data Block 2
0380 to 03FE	Data Block 3
0400 to 047E	Data Block 4
•	•
•	•
•	•
1F80 to 1FFE	Data Block 59

The Data Block Address Stack is a first-in, first-out implementation of a 64 word stack. Each entry in the stack consists of the 12 least significant address bits of a data block ready for processing by the BCIU. Entries in the stack are in sequential address locations.

The location 0200 is used by the BCIU for storing the BCIU Data Block Address Stack Pointer. This pointer, initialized by the CPU at Stack Location 2, is used by the BCIU for storing the next Address Stack location to be read out. It is incremented by the BIU every time a data block is to be processed. When an Error Interrupt occurs, this location contains the stack address, which points to the data block where the error was detected. The data block area consists of data block sections 64 words long. A maximum of 62 data blocks can be handled by the BCIU.

BC Controller Start

The CPU issues this command in the BCIU Mode whenever a 1553 Data Block is available for transmission.

The data word associated with this command contains the number of Data Blocks ready for transmission:

Bit 7-0	Message Count: 00000000 = 1 Message 11111111 = 256 Messages
Bit 15-8	NOT USED

Upon receipt of the Controller Start Command, the BCIU takes the following actions:

1. Reads and increments the content of the BCIU Data Block's Address Stack Pointer
2. Addresses the data block stack using the data obtained from the data block's Address Stack Pointer
3. Addresses the data block using the data obtained from the data block's stack.
4. Transfers the 1553 message over the 1553 Data Bus.
5. At the end of the transfer it decrements by one, the number of data blocks to be processed.
6. Generates an EOM Interrupt if all the data blocks have been transmitted. Otherwise, steps 1 through 5, above, are repeated.

If an error occurs, the BCIU continues transmission until the end of the message, after which the BCIU generates an Error Interrupt, decreases by one the number of data blocks to be processed, and then stops. The error can be caused by one of three conditions:

- 1553 Format
- Timeout
- Loop Test

The Controller hardware also checks for a bit set in the Status Word. However, it does not stop the Controller in this case.

BC Controller Continue/Stop

The CPU issues this command to the BCIU when it wishes the BCIU to resume processing a halted Start Command or to stop the BCIU's predetermined mode of operation at the end of the current data block. The format of the data word associated with this command is:

Bit 0	Logic "1" – Continue Logic "0" – Stop
Bit 1-15	NOT USED

BCIU Timeout

Receive and RT-to-RT Transfer Modes. The BCIU will provide a Timeout function to protect the BIU from locking up if the receiving RT does not transmit the Status Word (in the receive mode) or if either the transmitting or receiving RT do not transmit their Status Word (in the RT-to-RT mode). The BIU in this case will reset itself to the initialized state and prepare to receive a new command from the CPU, after having issued an Error Interrupt to the CPU. The minimum no-response Timeout is 14μs.

Transmit Transfer Mode. The BIU will provide a Timeout function to protect itself from locking up if the transmitting RT does not respond with a Status Word. The BIU in this case will reset itself after the no-response Timeout period and prepare to receive another command from the CPU after having issued an Error Interrupt to the CPU.

BC Data Block Configuration

Each Data Block is loaded by the CPU sequentially into the BIU Data Buffer with a Control Word followed by the 1553 Command and Data Words to be transmitted over the Mux Bus. The last word transmitted over the 1553 Data Bus by the BIU is added to the next addressable location in the Loop Test. The Status or Data Words received on the 1553 Data Bus are added sequentially to the Data Block.

The Control Word format is:

Bits 15-8	Not used
7	Channel A/$\overline{B}$ Bus operation
6	Spare
5	Spare
4	Spare
3	Spare
2	Mode Code
1	Broadcast
0	RT-to-RT

Data is stored in the Data Buffer in the same format as it appears on the 1553 Multiplex Bus, preceded by the Control Word. The formats that apply to the different types of messages received are shown in Table 1.

REMOTE TERMINAL OPERATIONS

The BIU assumes the role of a remote terminal after having received the External Status Load command from the Subsystem with bit 7 set to a logic "1".

RTU Memory Allocation

The 4K x 16 memory is used as a data buffer when the BIU is operating in the RT Mode. The memory has three sections:

- Table Look-up
- Command Stack
- Data

The address allocation is as follows:

Address	Area
0000 to 007E	Look-Up Table A
0080 to 00FE	Command Stack A
0100 to 017E	Look-Up Table B
0180 to 01FE	Command Stack B
0200	Pointer A
0202	Pointer B
0204 to 023E	Spare
0240 to 027E	Data Block 1
0280 to 02BE	Data Block 2
0200 to 02FE	Data Block 3
0300 to 033E	Data Block 4
•	•
•	•
•	•
1FC0 to 1FFE	Data Block 119

Each one of the look-up table sections is 64 words long. Each section is addressed by the combination of the T/$\overline{R}$ bit together with the 5 bit subaddress field contained in the valid Command Word received. Thus, for each T/$\overline{R}$ bit plus 5 bit subaddress combination, a particular location is addressed in the look-up table area. This look-up area is initialized with the addresses of the data blocks upon power-up by the subsystem software. The remote terminal uses the look-up address to read the base address of the data block. The 1553 Data Words are subsequently transferred to/from that data block.

The Command Stack is organized as a 64 word long first-in, first-out stack. Every valid Command Word received is added to the stack in successive locations. A pointer is used in association with the Command Stack to identify the last location used. At power-up, this pointer will be initialized by the Subsystem to the top of the Command Stack. The data section is divided into 119 Data Word Blocks, each 32 Data Words long.

TABLE 1. DATA BLOCK FORMATS

Receive Data Block	Transmit Data Block	RT-to-RT Data Block	Mode Code With Data-Receive Data Block	Mode Code With Data-Transmit Data Block	Mode Code No Data, Data Block
Control Word	Control Word	Control Word	Control Word	Control Word	Control Word
Receive Command	Transmit Command	Receive Command	Mode Command	Mode Command	Mode Command
Data Word 1	Transmit Command (looped back by BIU)	Transmit Command (looped back by BIU)	Data Word (looped back by BIU)	Mode Command (looped back by BIU)	Mode Command (looped back by BIU)
Data Word 2	Status Received	Status 1 Received (from transmitter)	Status Received (if any)	Status Received	Status Received
•	Data Word 1 Rcvd	Data Word 1 Rcvd	Data Word Rcvd	Data Word Rcvd	
•	Data Word 2 Rcvd	Data Word 2 Rcvd			
•	•	•			
Last Data Word	•	•			
Last Data Word (looped back by BIU)	•	•			
Status Received (if any)	Last Data Word Rcvd	Last Data Word Rcvd			
		Status 2 Received (from receiver)			

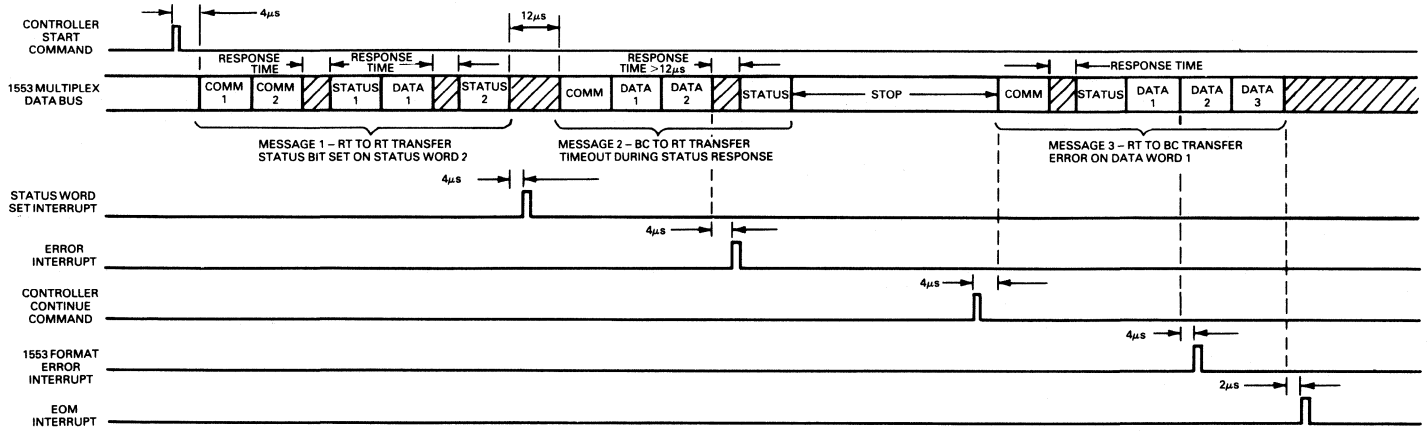


FIGURE 2. BUS CONTROLLER INTERRUPT TIMING

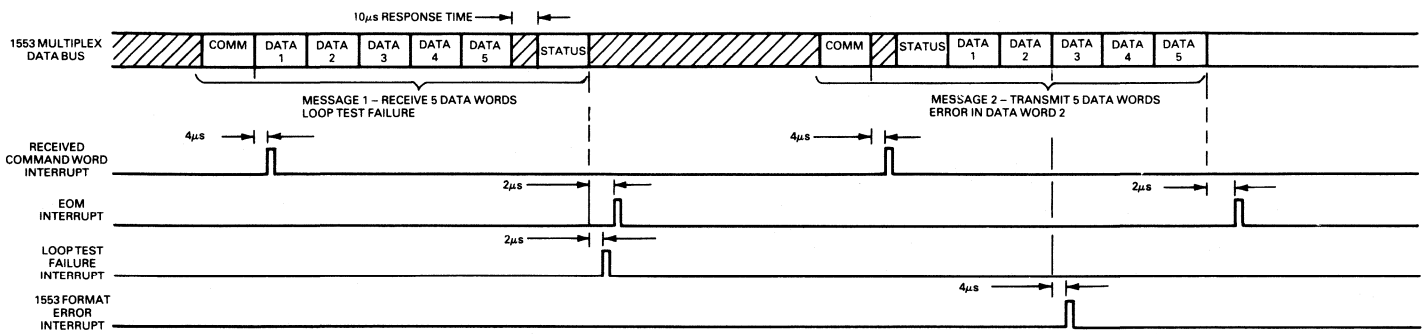


FIGURE 3. REMOTE TERMINAL UNIT INTERRUPT TIMING

RTU Sequence

Upon receipt of a valid Command Word over the 1553 Multiplex Bus, the BIU – acting as an RT – takes the following actions:

1. Generates a Look-Up Address by extracting the T/$\overline{R}$ and subaddress bits from the Command Word.
2. Reads and increments the RT Stack Pointer.
3. Uses the contents of the Stack Pointer to address a location in the Command Stack.
4. Stores a Command Word at that location.
5. Uses the Look-Up Address to read a data block Base Address from the Look-Up Table. A Busy Flag is also placed in bit 15 of the Look-Up Table entry being addressed to indicate that a transfer operation is in progress.
6. Generates a Command Received Interrupt if this Interrupt Mode is enabled.

The 1553 Data Words associated with a valid command are transferred to/from a Data Block using the block address obtained in (5), above. The Data Words within the Data Block are addressed sequentially using a BIU Internal Word Counter.

When the end of a Data Block is detected, the BIU removes the Busy Flag from the Look-Up Table Entry. If BIU Controlled Double Buffering is selected, then Bit 6 of the Look-Up Table Entry is toggled. The BIU also generates an EOM Interrupt at the end of a Data Block.

RTU Double Buffering

The double buffering can be used to prevent partially updated Data Blocks from being either read by the Subsystem or transmitted by the 1553 bus. The dual access memory can be organized to accomplish double buffering by designating two control areas: A and B. Each control area consists of a Command Stack, a Look-Up Area and a Pointer Area.

At any given time, one control area is designated as current and is used by the BIU to transfer data to/from the 1553 data bus while the other area is used by the Subsystem to read received data or prepare data for transmission. The selection of which area is current is determined by the External Status Load Command.

If Bit 6 of the Data Word corresponding to this command is set to a logic "0", then Control Area A is current to the BIU. If this bit is a logic "1", then Control Area B is current to the BIU.

The actual switching of control areas is accomplished while the BIU is not receiving or transmitting over the 1553 Bus. The Subsystem can issue an External Status Read command to see which control area is current.

The double buffering can also be controlled by the BIU as opposed to the Subsystem. The type of double buffering required is controlled by bit 6 of the Data Word associated with the External Status Load command. If this

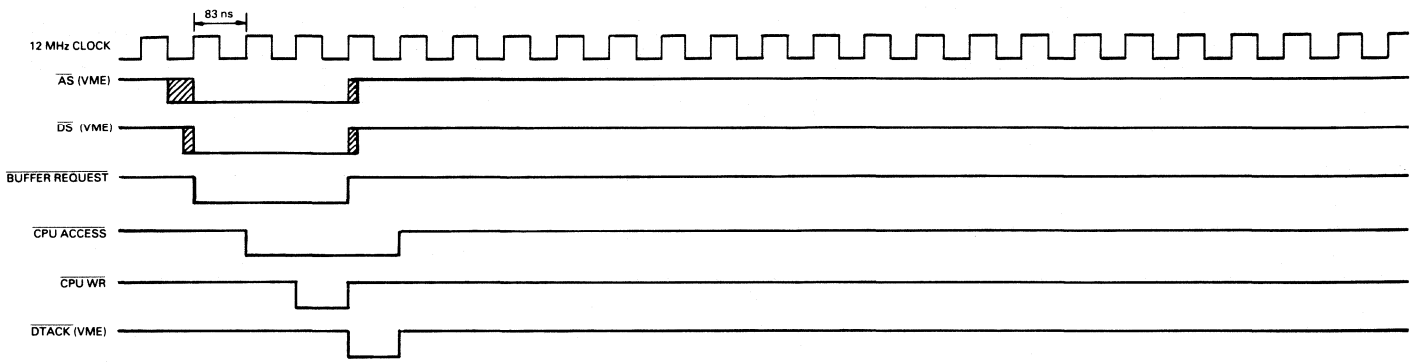


FIGURE 4. BUS-65500 TIMING

bit is a logic "1", then the Subsystem controls the double buffering. If it is a logic "0", then the BIU has control.

When the double buffering is controlled by the BIU, Bit A6 in the Look-Up Area is toggled at the end of a good data message. This allows 59 pairs of adjacent data blocks to be used (2 and 3, 4 and 5,...118 and 119).

RTU Mode Codes

When operating as a remote terminal, the BIU will implement the following Mode Codes:

T/$\overline{R}$ BIT	MODE CODE	FUNCTION	DATA WORD
1	00000	Dynamic Bus Control	NO
1	00001	Synchronize	NO
1	00010	Transmit Status Word	NO
1	00100	Transmitter Shutdown	NO
1	00101	Override Xmtr Shutdown	NO
1	01000	Reset Remote Terminal	NO
1	10000	Transmit Vector Word	YES
0	10001	Synchronize	YES
1	10010	Transmit Last Command	YES
1	00110	Inhibit T/F BIT	NO
1	00111	Override Inhibit T/F BIT	NO

In the case of the Dynamic Bus Control Mode Code, the RT, if enabled to accept this Mode Code, will set the Dynamic Bus Control Acceptance Bit to a logic "1" in the Status Word Response.

When the RT receives a Synchronize Mode Command without data, it transfers the Mode Code Command Word to the RT Data Buffer as a Standard Transmit Command Word.

The Reset Remote Terminal Mode Code will cause the RT to reset itself to the initialized state and to transmit the Status Word. Any Transmit Inhibit condition involving either Bus is also cleared by this Mode Code.

In the case of the Transmit Vector Word Mode Code, the RT will recognize this mode as an equivalent one word transmit message transferred from the VME to the 1553B Bus via the RT.

If an illegal mode code is received by the RT, the RT responds by setting the Message Error Bit in the Status Register and transmitting no more than the Status Word.

RTU Status Response Word Format

The format of the Status Word Response is:

Bits 15-11	Terminal Address
10	Message Error
9	Logic "0"
8	Service Request
7-5	Logic "0"
4	Broadcast Received
3	Busy
2	Subsystem Flag
1	Dynamic Bus Control Acceptance
0	Terminal Flag

The four external condition flags, i.e., Service Request, Busy, Subsystem Flag and Dynamic Bus Control Acceptance, are set up with the External Status Load Command.

LOOP TESTS

Long Loop Test

Function and circuitry are provided in the BIU to facilitate full loop testing of the VME/BIU/1553 Bus combination. The BIU will receive the last word transmitted by the BIU and pass it on to the Buffer Memory for each message. The VME, with the support of its processor, will process the Data Word to check the operational status of both the transmit and receive paths of the BIU.

Short Loop Test

The BIU implements a Short Loop Test wherein the last word transmitted in a message is looped back into the Encoder/Decoder where it is checked against the word transmitted. Detection of an error initiates an Interrupt to the VME and sets the Terminal Flag when operating as an RT.

BUS-65500 PIN FUNCTION AND LOADING TABLE

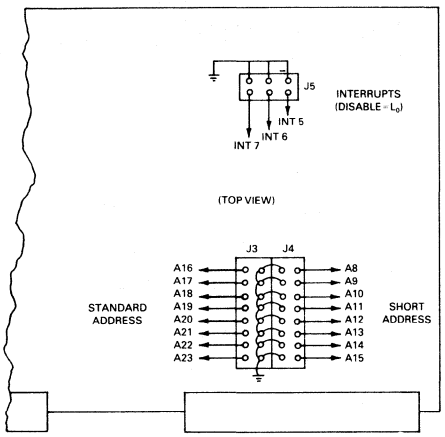
PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
A1	D0	20	−0.4	−3.0	48.0	LSB of VME 16 bit Tri-State Data I/O.
A2	D1	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
A3	D2	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
A4	D3	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
A5	D4	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
A6	D5	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
A7	D6	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
A8	D7	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
C1	D8	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
C2	D9	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
C3	D10	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
C4	D11	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
C5	D12	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
C6	D13	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
C7	D14	20	−0.4	−3.0	48.0	Part of VME 16 bit Tri-State Data I/O.
C8	D15	20	−0.4	−3.0	48.0	MSB of VME 16 bit Tri-State Data I/O.
A30	A1	20	−0.4			LSB of VME 23 bit Address Bus.
A29	A2	20	−0.4			Part of VME 23 bit Address Bus.
A28	A3	20	−0.4			Part of VME 23 bit Address Bus.
A27	A4	20	−0.4			Part of VME 23 bit Address Bus.
A26	A5	20	−0.4			Part of VME 23 bit Address Bus.
A25	A6	20	−0.4			Part of VME 23 bit Address Bus.
A24	A7	20	−0.4			Part of VME 23 bit Address Bus.
C30	A8	20	−0.4			Part of VME 23 bit Address Bus.
C29	A9	20	−0.4			Part of VME 23 bit Address Bus.
C28	A10	20	−0.4			Part of VME 23 bit Address Bus.
C27	A11	20	−0.4			Part of VME 23 bit Address Bus.
C26	A12	20	−0.4			Part of VME 23 bit Address Bus.
C25	A13	20	−0.2			Part of VME 23 bit Address Bus.
C24	A14	20	−0.2			Part of VME 23 bit Address Bus.
C23	A15	20	−0.2			Part of VME 23 bit Address Bus.
C22	A16	20	−0.2			Part of VME 23 bit Address Bus.
C21	A17	20	−0.2			Part of VME 23 bit Address Bus.
C20	A18	20	−0.2			Part of VME 23 bit Address Bus.
C19	A19	20	−0.2			Part of VME 23 bit Address Bus.
C18	A20	20	−0.2			Part of VME 23 bit Address Bus.
C17	A21	20	−0.2			Part of VME 23 bit Address Bus.
C16	A22	20	−0.2			Part of VME 23 bit Address Bus.
C15	A23	20	−0.2			MSB of VME 23 bit Address Bus.
B16	AM0	40	−0.1			LSB of Address Modifier's 6 bit input.
B17	AM1	40	−0.1			Part of Address Modifier's 6 bit input.
B18	AM2	40	−0.1			Part of Address Modifier's 6 bit input.
B19	AM3	40	−0.1			Part of Address Modifier's 6 bit input.
A23	AM4	40	−0.1			Part of Address Modifier's 6 bit input.
C14	AM5	40	−0.1			MSB of Address Modifier's 6 bit input.
A16	$\overline{\text{DTACK}}$			−0.25	48.0	Data Transfer Acknowledge output indicates that the data transfer is completed. When the processor recognizes $\overline{\text{DTACK}}$ during a Read Cycle, data is latched and the cycle terminated. On a Read Cycle, the output goes LOW to indicate that the data has been read from memory and has been placed on the Data Bus.

BUS-65500 PIN FUNCTION AND LOADING TABLE

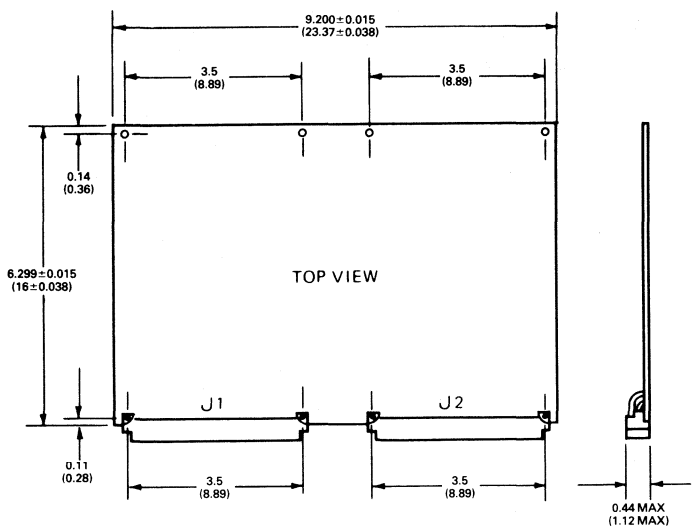
PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
A21	$\overline{\text{IACKIN}}$	20	−0.4			Interrupt acknowledge In is a Totem-Pole driven input which, when active LOW, indicates to the BIU that an acknowledge cycle is in progress. This signal forms a daisy-chained acknowledge.
A22	$\overline{\text{IACKOUT}}$			−1.0	20.0	Interrupt Acknowledge Out output indicates to the next board that an acknowledge cycle is in progress. This signal forms a daisy-chained acknowledge.
A12	$\overline{\text{UDS}}$	20	−0.4			Upper Data Strobe input controls the data on the VME Data Bus. When this input is LOW, the valid Data Bits are D8-D15.
A13	$\overline{\text{LDS}}$	20	−0.4			Lower Data Strobe input controls the data on the VME Data Bus. When this input is LOW, the valid Data Bits are D0-D7.
A18	$\overline{\text{AS}}$	20	−0.4	0.02		Address Strobe. A LOW on this input indicates a Valid Address on the Address Bus.
B26	$\overline{\text{INT 5}}$			−1.25	60.0	Interrupt Request: an open collector output to signal an interrupt request on Level 5, the lowest priority driven by the BCIU.
B25	$\overline{\text{INT 6}}$			−0.25	60.0	Interrupt Request: an open collector O/P used for the 2nd highest prior interrupt request.
B24	$\overline{\text{INT 7}}$			−0.25	60.0	Interrupt Request: an open collector O/P used for the highest priority interrupt request.
C12	$\overline{\text{SYS RESET}}$	20	−0.4			A LOW on this input line resets the BIU to the power-on condition.
A32	+5V					+5V Power supply input.
B32	+5V					+5V Power supply input.
C32	+5V					+5V Power supply input.
A14	READ/$\overline{\text{WRITE}}$	20	−0.4			This input defines the processor data transfer as a read or write cycle. A HIGH indicates a read operation; a LOW indicates a write operation. This signal works in conjunction with the upper and lower data strobes.
A20	$\overline{\text{IACK}}$	20	−0.4			Interrupt Acknowledge. A LOW on this input indicates that the processor has granted the interrupt.
A9	GND					Logic and power return.
A11	GND					Logic and power return.
A15	GND					Logic and power return.
A17	GND					Logic and power return.
A19	GND					Logic and power return.
B20	GND					Logic and power return.
C31	+15V					+15 Volt power supply input.
A31	−15V					−15 Volt power supply input.
C15	RTA0	60	−1.0			LSB of 5 bit RTU Address input.
C13	RTA1	60	−1.0			Part of 5 bit RTU Address input.
C16	RTA2	60	−1.0			Part of 5 bit RTU Address input.
C14	RTA3	60	−1.0			Part of 5 bit RTU Address input.
C17	RTA4	60	−1.0			MSB of 5 bit RTU Address input.
C12	RTPAR	40	−0.8			Parity input for 5 bit RTU Address input (Odd Parity).
C19	BUS A DIRECT COUPLED					Direct coupled MIL-STD-1553B BUS A DATA connection.
C24	BUS A XFMR COUPLED					Transformer coupled MIL-STD-1553B BUS A DATA connection.
C25	BUS A CTR TAP					Center tap connection for BUS A Isolation Transformer.
C20	BUS A XFMR COUPLED					Transformer coupled MIL-STD-1553B BUS A $\overline{\text{DATA}}$ connection.
C21	BUS A DIRECT COUPLED					Direct coupled MIL-STD-1553B BUS A $\overline{\text{DATA}}$ connection.
C11	BUS A $\overline{\text{REC INH}}$	20	−0.4			A LOW on this input disables BUS A receiver.
C6	BUS B DIRECT COUPLED					Direct coupled MIL-STD-1553B BUS B DATA connection.
C4	BUS B XFMR COUPLED					Transformer coupled MIL-STD-1553B BUS B DATA connection.
C5	BUS B CTR TAP					Center tap connection for BUS B Isolation Transformer.
C8	BUS B $\overline{\text{XFMR COUPLED}}$					Transformer coupled MIL-STD-1553B BUS B $\overline{\text{DATA}}$ connection.
C7	BUS B $\overline{\text{DIRECT COUPLED}}$					Direct coupled MIL-STD-1553B BUS B $\overline{\text{DATA}}$ connection.
C10	BUS B $\overline{\text{REC INH}}$	20	−0.4			A LOW on this input disables BUS B receiver.
C18	GND					Power and logic return.
C9	GND					Power and logic return.

NOTES: In the above table, the symbols are defined as follows:
I_{IH}=maximum input HIGH current with V_{in}=2.4V min.
I_{IL}=maximum input LOW current with V_{in}=0.8V max.
I_{OH}=maximum output HIGH current with V_{out}=4.5V min.
I_{OL}=maximum output LOW current with V_{out}=0.4V max.

JUMPER CONNECTIONS



MECHANICAL OUTLINE BUS-65500



ORDERING INFORMATION

BUS-65500-883B

Power Supply Option:
0=±15VDC supplies
1=±12VDC supplies

DDC
ILC DATA DEVICE CORPORATION

MIL-STD-1553 HYBRID DUAL REDUNDANT BUS CONTROLLER AND REMOTE TERMINAL

DESCRIPTION

The BUS-65600 is a dual redundant MIL-STD-1553 Bus Controller (BC) and Remote Terminal Unit (RTU) packaged in a 1.9" x 2.1" hermetic hybrid. It provides all the functions required to interface between a MIL-STD-1553 dual redundant MUX data bus transceiver, such as DDC's BUS-63125, and a subsystem parallel 3-state data highway. Utilizing several DDC custom monolithic ICs, the BUS-65600 provides selectable operation as either a Bus Controller or a Remote Terminal Unit. It is a flexible and easy to use component, and includes dual encoder/decoders, dual bit processors, RTU protocol, BC protocol, and a simple DMA subsystem interface.

The BUS-65600 is compatible with most microprocessors. It provides a 16-bit 3-state parallel data bus, and DMA handshaking for subsystem message transfers. All message transfer timing, as well as DMA address and

(con't. on page 419)

FEATURES

- *SELECTABLE BC OR RTU OPERATION.*
- *SMALL 1.9" x 2.1" HYBRID PACKAGE.*
- *16 BIT MICROPROCESSOR COMPATIBILITY. DMA SUBSYSTEM MESSAGE TRANSFERS. COMPLETE TIMING AND CONTROL PROVIDED INTERNALLY; WITH COMMON SIGNALS FOR BC AND RTU.*
- *BC CHECKS STATUS WORD FOR VALID ADDRESS AND PRESENCE OF BIT FLAGS.*
- *RTU HAS ALL MODE CODES AVAILABLE; WITH ILLEGAL MODE CODES EXTERNALLY SELECTABLE.*
- *BC AND RTU ERROR DETECTION FOR RESPONSE TIME, TIMING GAPS, SYNC, PARITY, MANCHESTER, WORD COUNT, AND BIT COUNT.*
- *CONTINUOUS ON-LINE BUILT-IN TEST.*

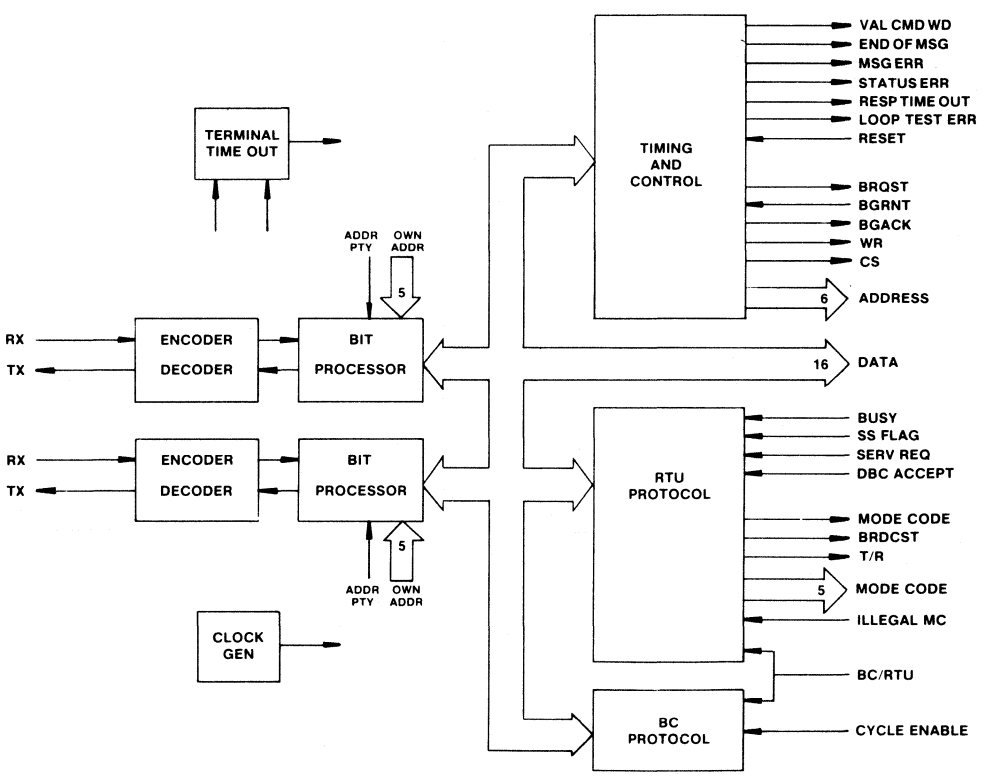


FIGURE 1. BUS-65600 BLOCK DIAGRAM

DESCRIPTION *(con't. from page 418)*

control lines, are provided internally. Subsystem overhead associated with message transfers is therefore minimized. Interface control lines are common for both BC and RTU operation.

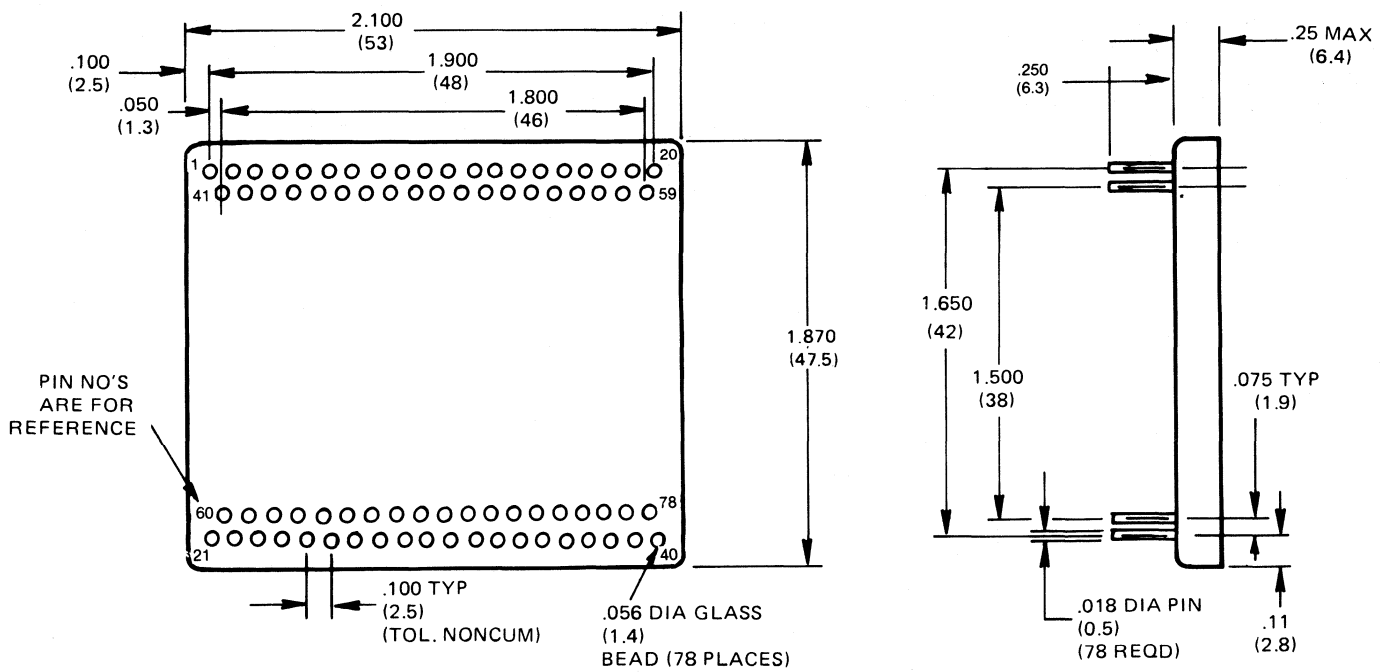
The BUS-65600 features the capability for implementing any or all of the MIL-STD-1553 mode codes. Any mode code may be defined as illegal by an externally selected ROM code. Complete error detection capability is provided by the BUS-65600, for both BC and RTU modes, including response time, timing gaps, sync, parity, Manchester, word count, and bit count. Additionally, in the BC mode, the status word is checked for proper address and the setting of bit flags.

The BUS-65600 carries out a continuous on-line self-test. All transmitted messages are wrapped around through the receiver channel, and compared to the desired message. An off-line loop test, under subsystem control, can also be implemented. Numerous error flags are provided to the subsystem including message error, status error, response timeout and loop test error.

The BUS-65600 complies with all of the requirements of MIL-STD-1553. The hybrid is screened in accordance with the requirements of MIL-STD-883B and operates over the full military temperature range of -55° C to +125° C.

MECHANICAL OUTLINE

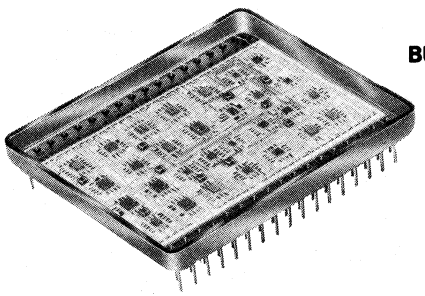
Dimensions in inches (millimeters)



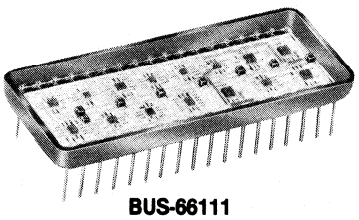
ORDERING INFORMATION
BUS-65600-883B

DDC
ILC DATA DEVICE CORPORATION

MIL-STD-1553 BUS CONTROLLER PROTOCOL HYBRIDS



BUS-66106



BUS-66111

DESCRIPTION

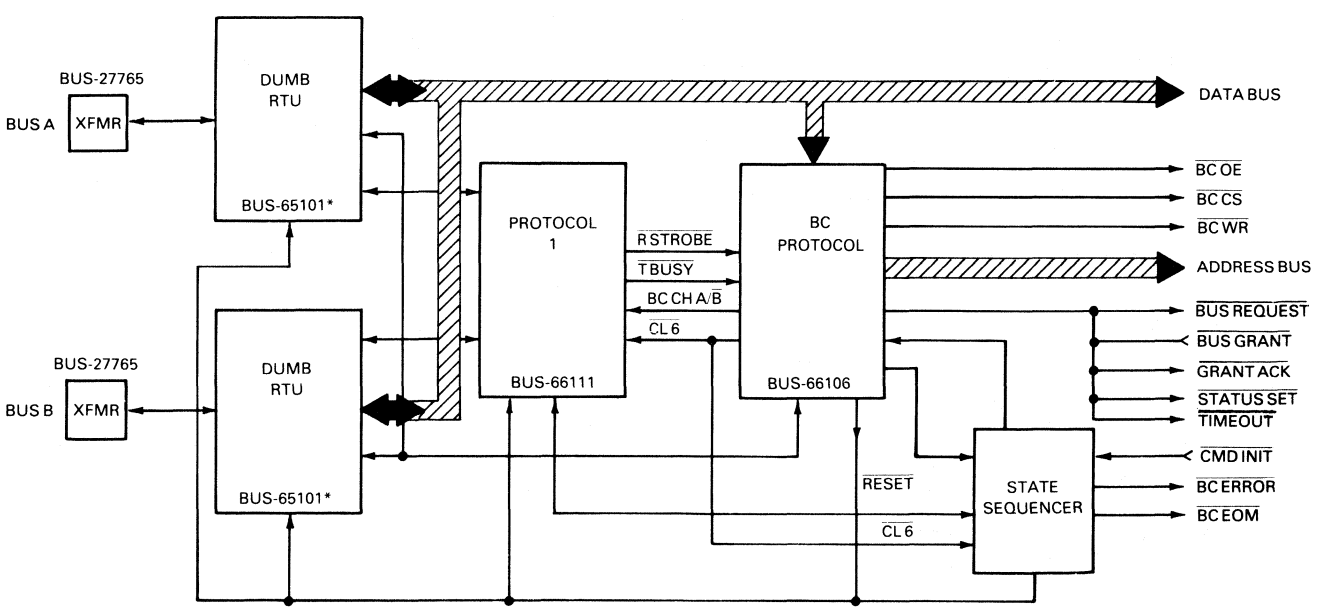
BUS-66106 and BUS-66111 comprise a pair of hybrids which generate the complete protocol, timing and control function required by a Bus Controller (BC) in full compliance with MIL-STD-1553 or MacAir A5690. When used with a Dumb RTU and State Sequencer, as shown in Figure 1, these BC Protocol hybrids provide a complete Bus Controller function which supports all message formats. A significant feature is that the RTU status word response is validated by the BC Protocol hybrids with no subsystem intervention.

BUS-66106 and BUS-66111 BC Protocol hybrids provide a simple and flexible interface to the subsystem. Message transfers are accomplished by means of a DMA type handshaking. Output flags are provided to the subsystem at the end of each message, when a BC error has occurred, a status word bit has been set, and a Terminal Fail-Safe Timeout has occurred. The BC Protocol hybrids provide control lines for implementation of online wraparound built-in test of the Bus Controller.

The BUS-66106 is packaged in a 68 pin 1.6 x 1.9 inch hybrid, and the BUS-66111 is packaged in a 36 pin DDIP 0.8 x 1.9 inch hybrid. A complete dual redundant Bus Controller and Remote Terminal Unit, using these hybrids, is available from DDC on a 6.3 x 9.2 inch VME Eurocard as part number BUS-65500.

FEATURES

- *GENERATES PROTOCOL, TIMING AND CONTROL FOR MIL-STD-1553 OR MACAIR A5690 BUS CONTROLLER*
- *SUPPORTS ALL MESSAGE FORMATS*
- *VALIDATES RTU STATUS RESPONSE AND DATA WORDS*
- *TRANSFERS MESSAGES WITH DMA TYPE HANDSHAKING*
- *PROVIDES FLAGS FOR:*
  END OF MESSAGE
  ERROR
  STATUS BIT SET
  TIMEOUT
- *IMPLEMENTS WRAPAROUND BUILT-IN TEST*



*FOR MACAIR A5690, USE BUS-65201

FIGURE 1. BLOCK DIAGRAM – BUS CONTROLLER HYBRID SET

SPECIFICATIONS – BUS-66106 Values at nominal supply voltage.		
PARAMETER	**UNITS**	**VALUE**
Logic		
I_{IH}, I_{IL}, I_{OH}, I_{OL}		See Pin Function and Loading Table.
V_{OL}	V	0.4 max.
V_{OH}	V	2.5 min.
V_{IL}	V	0.7 max.
V_{IH}	V	2.0 min.
Power Supplies		
Voltage	V	5.0±10%
Current Drain	mA	800 max.
Temperature Range (Case)		
Operating	°C	−55 to +125
Storage	°C	−65 to +150
Physical Characteristics		
Size	in.	1.85 x 1.59 x 0.21
	(mm)	(46.9 x 40.38 x 5.33)
Weight	oz.	2.0
	(gm)	(56)

SPECIFICATIONS – BUS-66111 Values at nominal supply voltage.		
PARAMETER	**UNITS**	**VALUE**
Logic		
I_{IH}, I_{IL}, I_{OH}, I_{OL}		See Pin Function and Loading Table.
V_{OL}	V	0.4 max.
V_{OH}	V	2.5 min.
V_{IL}	V	0.7 max.
V_{IH}	V	2.0 min.
Power Supplies		
Voltage	V	5.0±10%
Current Drain	mA	200 max.
Temperature Range (Case)		
Operating	°C	−55 to +125
Storage	°C	−65 to +150
Physical Characteristics		
Size	in.	1.895 x 0.775 x 0.21
	(mm)	(48.1 x 19.7 x 5.3)
Weight	oz.	1.0
	(gm)	(28)

GENERAL

BUS-66106 and BUS-66111 are Bus Controller Protocol hybrids designed for use in MIL-STD-1553 Bus Controllers. BUS-66111 functions as a multiplexer for the handshaking signals required by the Dumb RTUs interfacing to the dual serial MUX data bus. It generates control signals for the BUS-66106, as well as providing the fault processing function.

BUS-66106 provides the protocol timing and control for a MIL-STD-1553 Bus Controller. It supports all 1553 message formats while validating the RTU status word response without help from the subsystem. Its subsystem interface includes a 16 bit data highway, a 6 bit address bus and control lines for a DMA type handshake during message transfer.

A typical implementation of the Bus Controller function would include Dumb RTU BUS-65101, BC Protocol BUS-66106 and BUS-66111, a Programmable Logic Sequencer and possibly a dual port memory for interim message storage. DDC has packaged a complete dual redundant Bus Controller and Remote Terminal Unit on a 6.3 x 9.2 inch VME Eurocard, which is supplied as part number BUS-65500.

BUS-66106 OPERATION

The BUS-66106 contains three registers, a 16 bit Data Buffer, a Status Word Comparator, two counters and Timing Logic. (See Block Diagram, Figure 3.)

The 16 bit Tri-State Data Bus is buffered to prevent loading of the bus. The incoming data can be stored in one of the three registers, depending on the four mode signals originating in the State Sequencer. The three registers are:

- Command 1 Register
- Command 2 Register
- Control Word Register

BUS CONTROL ACTIVE FLAG

Upon receipt of the $\overline{\text{CMND INIT}}$ pulse (500ns minimum width) the Bus Controller activates the Bus Control Active output and starts the transmit cycle. The Bus Controller remains active until one of the following occurs, making the Bus Control Active Flag go high within one microsecond:

(1) Bus cycle Enable Input is taken low.

(2) Transmission by the Bus Controller is complete (Broadcast Mode).

(3) Transmission by the Bus controller is complete, a no response-time has occurred and an interrupt has been generated.

(4) During an RT to RT Transfer, the transmission by the Bus Controller is complete, the transmission by the first RT is complete, a no-response time-out has occurred and an interrupt has been generated.

(5) The complete transmit-receive cycle is complete and any required interrupts have been generated.

(6) A Bus Controller failure has been detected and the Bus Controller Error Flag has been set.

Upon receipt of the $\overline{\text{START}}$ signal from the sequencer, with BUS CYCLE ENABLE input HIGH, a Data Transfer from the Subsystem is requested by a $\overline{\text{BUS REQUEST}}$ output. When the $\overline{\text{B GRANT}}$ signal is received from the Subsystem, the first Data Word is read out of the Subsystem's memory and stored in the Control Word Register. The Control Word Register outputs are analyzed to detect what type of transfer is required, and then another $\overline{\text{START}}$ signal is received from the Sequencer. This causes the next location of the Subsystem's memory, which contains the Command Word, to be read. The Command Word is then latched in both Command 1 Register and in the external Encoder Register. Subsequently, the encoder is enabled and the Command Word is transmitted via the data bus. After each word transfer is completed, a COMPLETE output is generated to the Sequencer.

CONTROL WORD FORMAT

The format of the Control Word initiated by the Subsystem must be as follows:

BITS	FUNCTION
0	RT to RT Transfer
1	Broadcast Transfer
2	Mode Code Transfer
3-6	Not Used
7	Data Bus Channel Selection CHA/B
8-15	Not Used

To select one of the above transfers, the appropriate bit should be set to a high level. In the case of Bit 7, the Channel Selection, a high level will select BUS A and a low level will select BUS B.

If an RT to RT transfer is required, then the second Command Word is read out of the memory, after the first Command Word, and latched in the Command 2 Register as well as in the external Encoder's Register, prior to transmission.

Depending on the Command Word involved, data words are either read out of memory and latched by the external Encoder Register ready for transmission, or enabled by the external Decoder Register and written into memory after reception.

SUB-SYSTEM BUFFER CONTENTS

The Command Words and Data Words should be stored in the Sub-System Data Buffer in the same format as they are to appear on the Multiplex Data Bus.

The following data format for the Subsystem data buffer is implemented by the BUS-66106.

ADDRESS	DATA BUFFER CONTENTS	CONTROL CODE (3 LSB's)
(1)	Receive Command	000
000000	Control Word	
000001	Receive Command	
000010	Data Word 1	
000011	Data Word 2	
.	.	
.	.	
.	.	
.	Data Last Word	
.	Data Last Word (Wrapped)	
.	Status Received (If Any)	
(2)	Transmit Command	000
000000	Control Word	
000001	Transmit Command	
000010	Transmit Command (Wrapped)	
000011	Status Received	
000100	Data Word 1 Received	
000101	Data Word 2 Received	
.	.	
.	.	
.	.	
.	.	
.	Data Last Word Received	
(3)	RT To RT Command	000
000000	Control Word	
000001	Receive Command	
000010	Transmit Command	
000011	Transmit Command (Wrapped)	
000100	Status Word 1 (From Trans.) Received	
000101	Data Word 1 Received	
000110	Data Word 2 Received	
.	.	
.	.	
.	.	
.	Data Last Word Received	
.	Status 2 (From Rec.) Received	
(4)	Mode Code With Data (Rec.) Command	100
000000	Control Word	
000001	Mode Command	
000010	Data Word	
000011	Data Word (Wrapped)	
000100	Status Received (If Any)	
(5)	Mode Code With Data (Trans.) Command	100
000000	Control Word	
000001	Mode Command	
000010	Mode Command (Wrapped)	
000011	Status Received	
000100	Data Word Received	
(6)	Mode Code With No Data	100
000000	Control Word	
000001	Mode Command	
000010	Mode Command (Wrapped)	
000011	Status Received	
(7)	Broadcast Mode	010
000000	Control Word	
000001	Receive Command	
000010	Data Word 1	
000011	Data Word 2	
.	.	
.	.	
.	.	
.	Data Last Word	
.	Data Last Word (Wrapped)	

When a reply is expected from the Remote Terminal, the Timeout Counter is enabled and if no reply is received within 15μs, the BC TIMEOUT flag is set.

The first word received from the Remote Terminal is always a Status Word. When this word is received within 15μs, its address field is compared with the address field in the respective Command Word Register. It is also checked for any bits set HIGH. A STAT SET flag is set LOW if any bit was set in the Status Word or if the RT address field did not match.

INTERRUPT FLAGS

The BUS-66106 Hybrid, in conjunction with the Protocol Sequencer, provides the following flags:

(1) BC TIME OUT
This Flag will be set low if no response was obtained from a Remote Terminal within 15 microseconds (this interrupt does not occur in the case of a Broadcast Message) or an Invalid Status or Data Word was received, or if there was a word count error.

(2) STATUS SET
This Flag will be set low if the Status Word received had a wrong address or if one of the Subsystem Flags is set.

(3) BC ERROR
This Flag will be set low if there was an error during the BC operation.
Additionally, the BUS-66111 generates a BCU Fail Flag, which will be set high if an error occurred during the operation of the Dumb RTU Hybrid.

(4) BC EOM
This Flag will be set low when the message has been processed by the BUS-66106.

The 6 Bit Address Counter is incremented for every word read out or stored into the subsystem's memory. This counter also checks for the correct number of words transmitted. The BCL WORD flag is set when the number of words transmitted or received is the same as that indicated by the Word Count field in the Command Word Register.

All the DMA handshake signals are generated by the general timing logic. The timing for the subsystem's DMA handshake signals is shown on Figures 6 and 7.

SELF-TESTING CAPABILITY

The BUS-66106 implements a Long Loop Test wherein the last word transmitted by the Bus Controller of every message is received back (wrapped) and stored in the Data Buffer in the next location following the last word transmitted.

The Subsystem can compare the wrapped word with the last transmitted word to check the operational status of the receive and transmit circuitry.

BUS-66111 OPERATION

A $\overline{\text{R STROBE}}$ output is generated 1μs after the reception of a RCVR BUSY signal by the BUS-66111 from one of the Dumb RTUs interfacing with the two data buses. This pulse is only generated if the FAIL-SAFE FLAG inputs are active LOW.

The $\overline{\text{R STROBE}}$ pulse is used to sample the error condition, initiate the data transfer and simultaneously step the protocol sequencer device. $\overline{\text{R STROBE}}$ is generated for every RCVR BUSY input.

After the internal multiplexer is selected by the BC CH $\overline{\text{A}}$/B input, the following signals from one of the Dumb RTUs are selected:

- $\overline{\text{VALID WORD}}$
- FAIL-SAFE FLAG
- REC SYNC TYPE
- XMIT BUSY
- FAULT

The RCVR BUSY signal is sampled periodically to generate a NO DT (IDLE/$\overline{\text{ACTIVE}}$) signal. The XMIT $\overline{\text{BUSY}}$ signal is used internally to inhibit the generation of $\overline{\text{R STROBE}}$. In addition, 4$\mu$s after the falling edge of the last XMIT BUSY signal, a $\overline{\text{R INH}}$ internal signal is generated which samples the fault signal resulting from the Wraparound Test. This $\overline{\text{R INH}}$ signal is also used to sample the FAULT signal resulting from the operation of the system as a whole. If a fault is detected, then the BCU FAIL signal will be activated. This output can be used as an interrupt to flag a system error, in which case $\overline{\text{RESET}}$ can be used as an interrupt acknowledge.

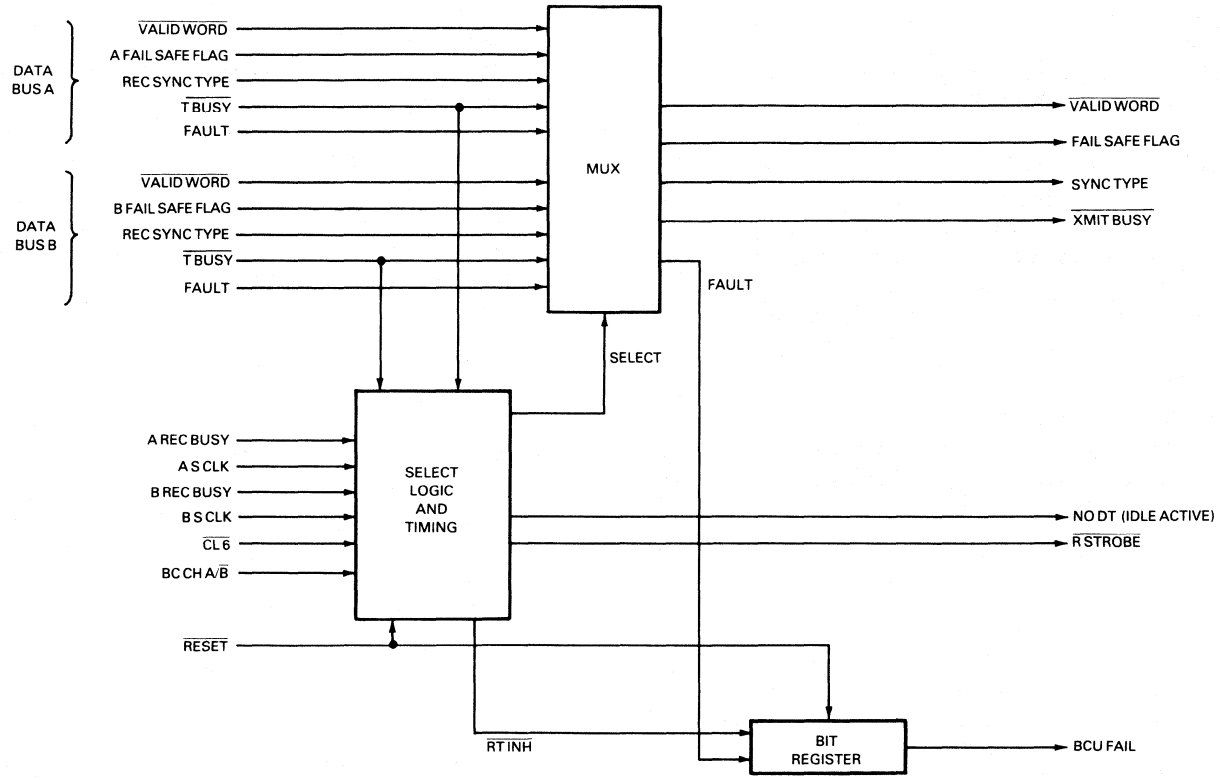


FIGURE 2. BUS-66111 PROTOCOL HYBRID BLOCK DIAGRAM

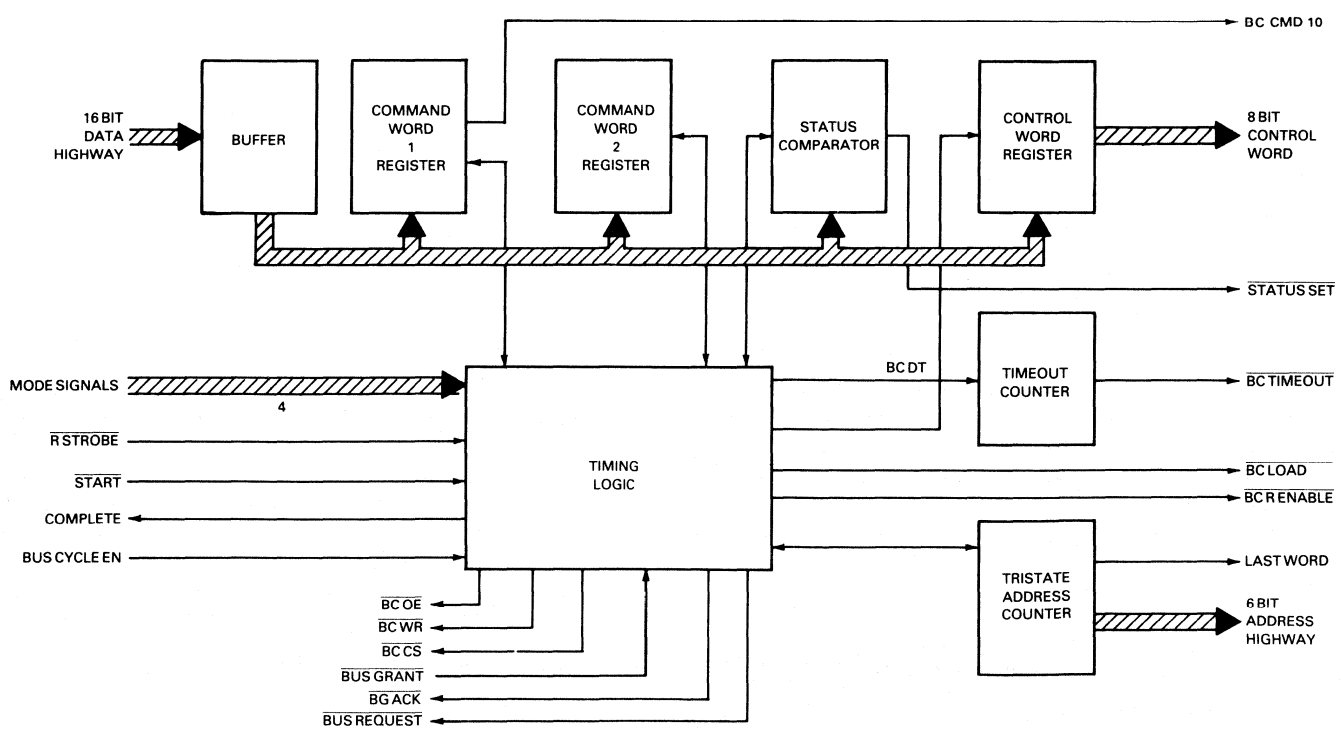


FIGURE 3. BUS-66106 BC PROTOCOL BLOCK DIAGRAM

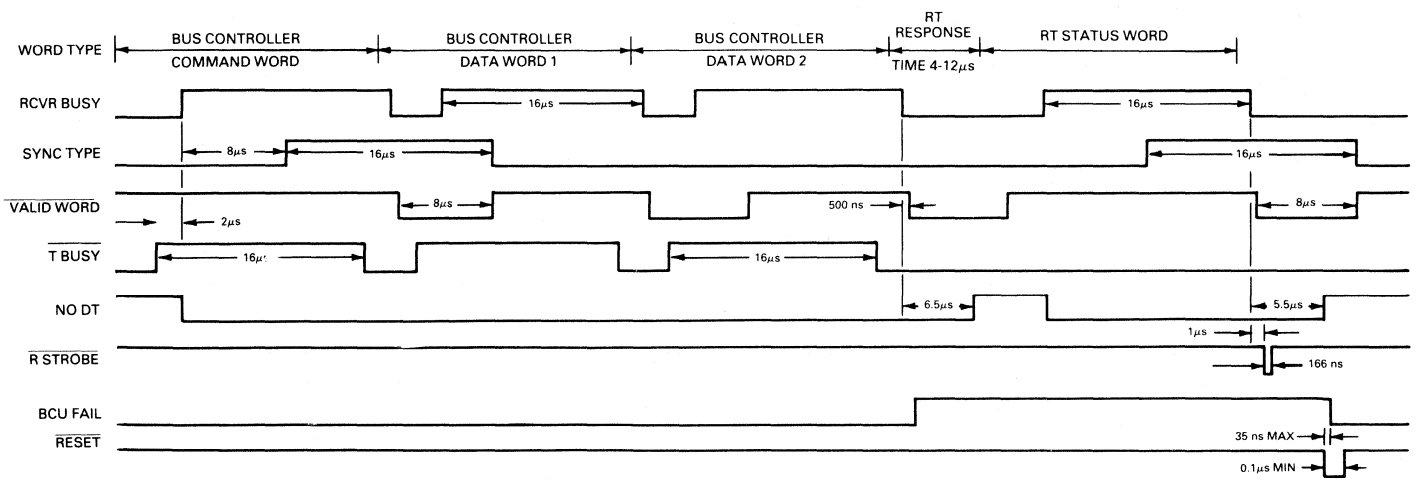


FIGURE 4. BUS-66111 TRANSMITTER MODE TIMING (2 DATA WORDS)

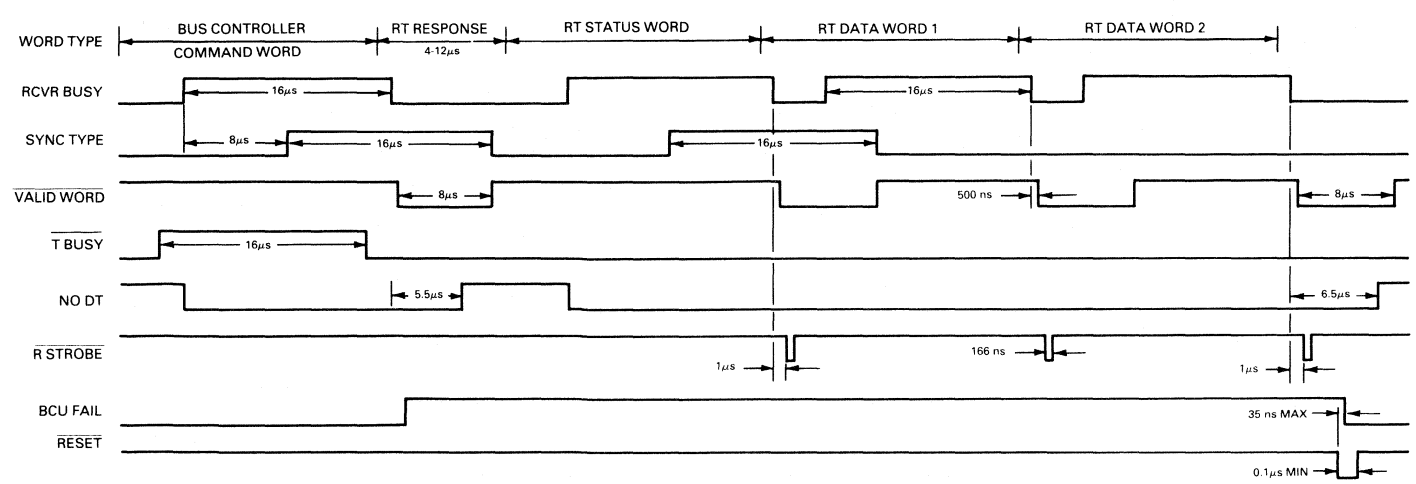


FIGURE 5. BUS-66111 RECEIVER MODE TIMING (2 DATA WORDS)

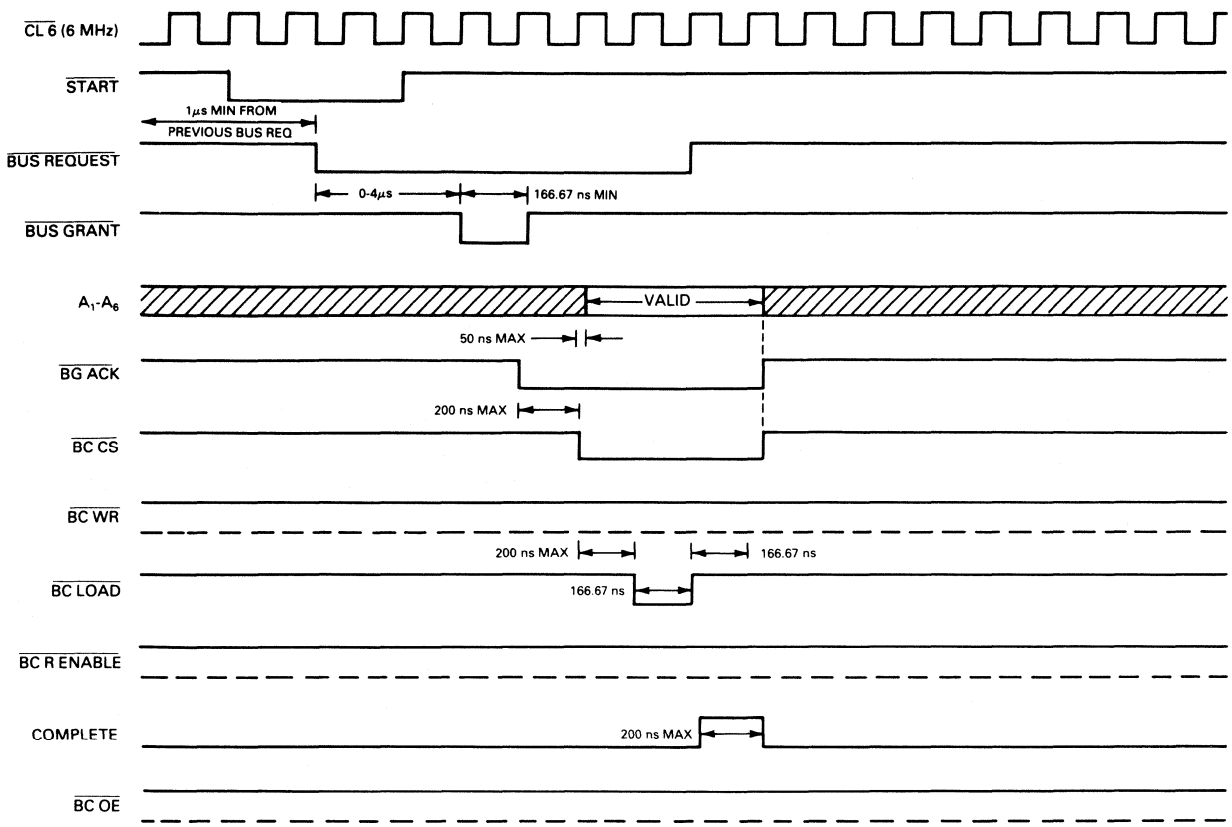


FIGURE 6. SUBSYSTEM MEMORY READING CYCLE

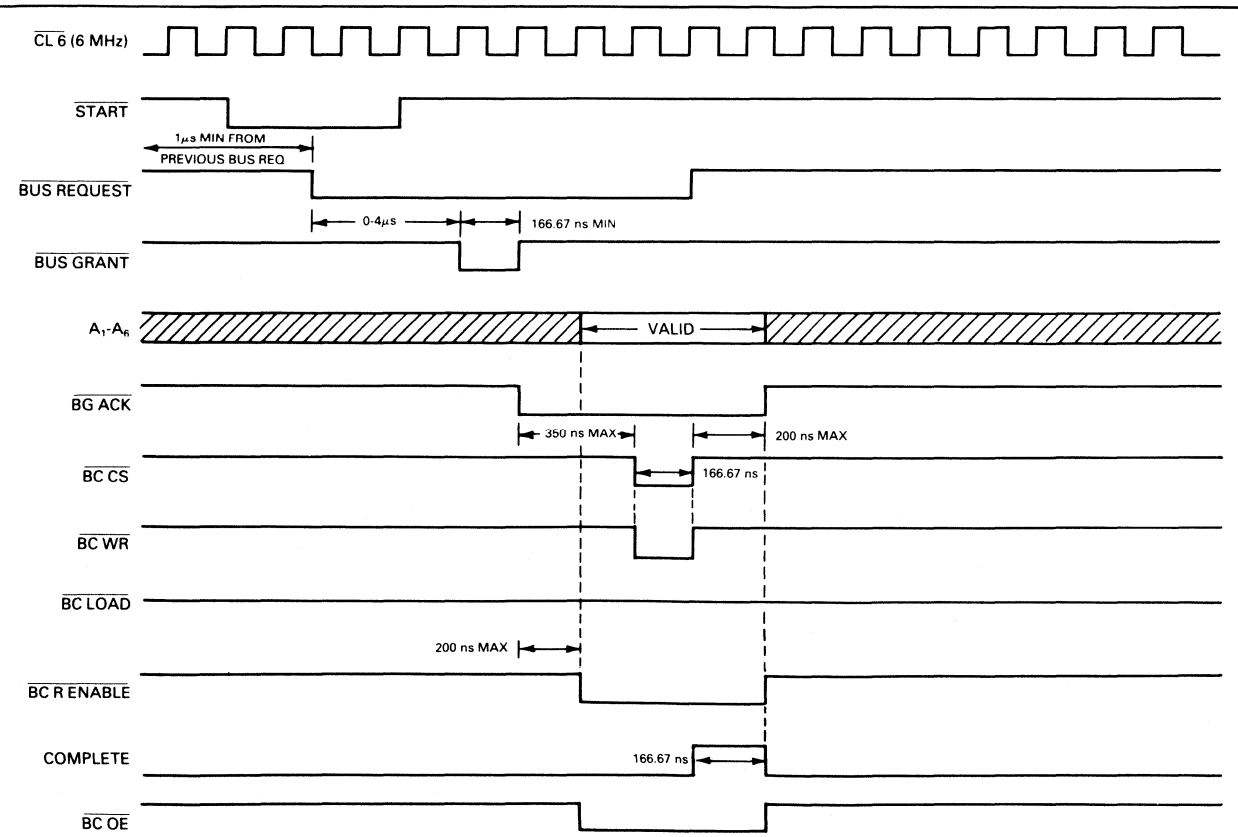


FIGURE 7. SUBSYSTEM MEMORY WRITING CYCLE

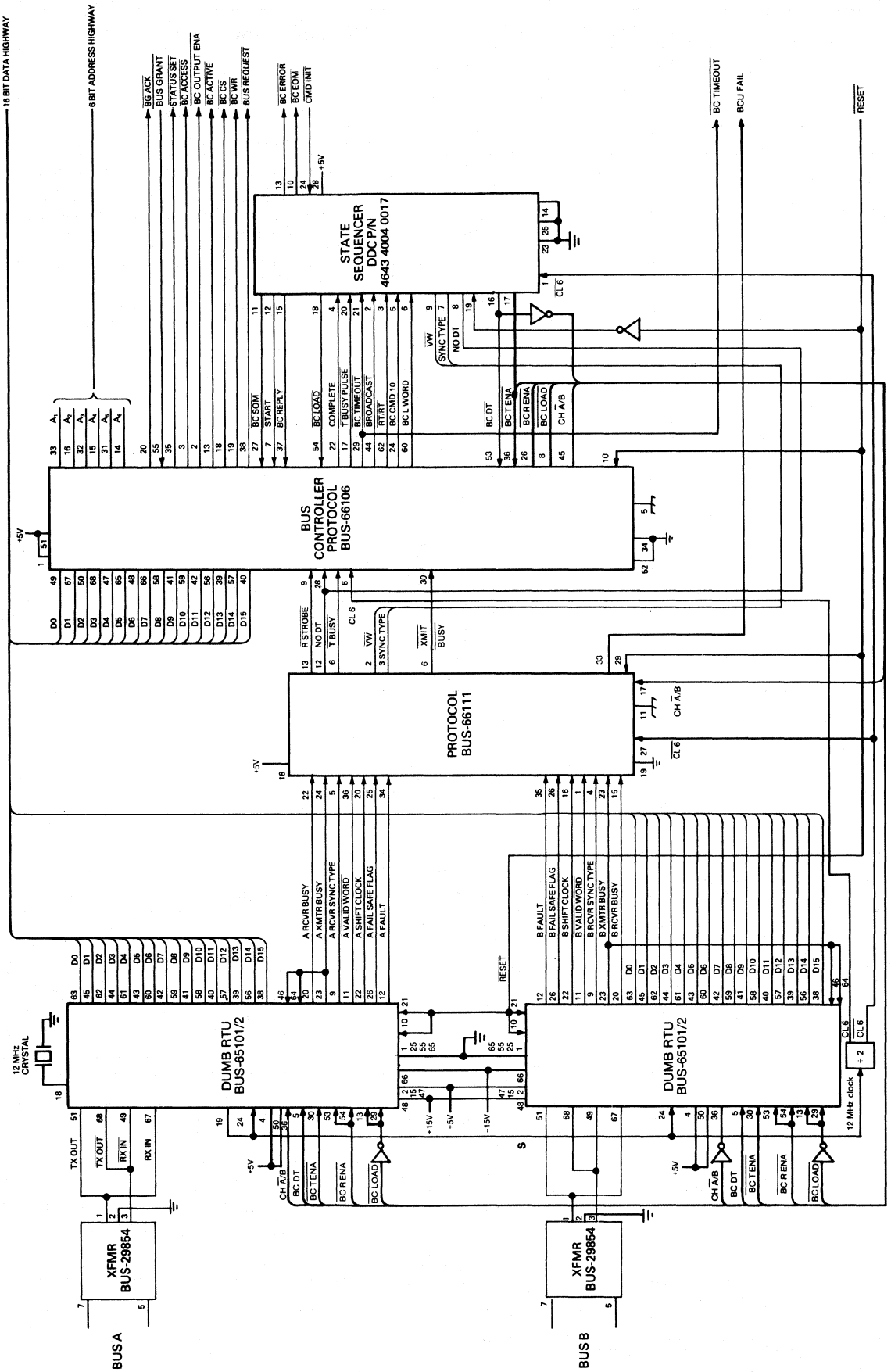


FIGURE 8. BUS CONTROLLER INTERCONNECT DIAGRAM

BUS-66111 PIN FUNCTION AND LOADING TABLE

PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
1	$\overline{\text{B VALID WORD}}$	20	−0.4			A LOW on this input indicates receipt of a valid word on Bus B.
2	$\overline{\text{VALID WORD}}$			−0.4	4.0	A LOW on this output indicates receipt of a valid word by the BCU.
3	SYNC TYPE			−0.4	4.0	A HIGH on this output indicates receipt of a Command or Status Word. A LOW indicates receipt of a Data Word.
4	B RCVR SYNC TYPE	20	−0.4			A HIGH on this input indicates receipt of a Command or Status word on Bus B. A LOW indicates receipt of a Data Word on Bus B.
5	A RCVR SYNC TYPE	20	−0.4			A HIGH on this input indicates receipt of a Command or Status Word on Bus A. A LOW indicates receipt of a Data Word on Bus A.
6	$\overline{\text{XMIT BUSY}}$			−0.4	4.0	A LOW on this output indicates that the BCU is transmitting.
7	NC					No connection.
8	NC					No connection.
9	NC					No connection.
10	NC					No connection.
11	CASE					Case connection.
12	NO DT			−0.4	4.0	A LOW on this IDLE/$\overline{\text{ACTIVE}}$ output indicates that the BCU is busy handling a message transfer.
13	$\overline{\text{R STROBE}}$			−0.4	4.0	This output goes LOW every time a valid Command or Data Word is received and is available for processing.
14	FAIL SAFE FLAG			−0.4	4.0	A HIGH on this output indicates that a 680μs fail-safe timeout occurred in one of the transmitters interfacing with the data bus.
15	B RCVR BUSY	60	−1.2			This input goes HIGH for nominally 16μs for each word being decoded on either Bus A or Bus B.
16	B SHIFT CLOCK	40	−0.8			Input for a TTL compatible 1 MHz decoder shift clock, which is synchronized with the Manchester coded data being received on Bus B.
17	BC CH$\overline{\text{A}}$/B	40	−0.8			A LOW on this input indicates selection of Channel A.
18	+5V DC					+5V power input.
19	GND					Logic and power return.
20	A SHIFT CLOCK	40	−0.8			Input for a TTL compatible 1 MHz decoder shift clock, which is synchronized with the Manchester coded data being received on Bus A.
21	NC					No connection.
22	A RCVR BUSY	60	−1.2			A HIGH on this input indicates that the BCU is receiving data on Bus A.
23	B XMIT BUSY	20	−0.4			A HIGH on this input indicates that the BCU is transmitting on Bus B.
24	A XMIT BUSY	20	−0.4			A HIGH on this input indicates that the BCU is transmitting on Bus A.
25	A FAIL-SAFE FLAG	40	−0.8			A HIGH on this input indicates that a 680μs timeout occurred on Bus A transmitter.
26	B FAIL-SAFE FLAG	40	−0.8			A HIGH on this input indicates that a 680μs timeout occurred on Bus B transmitter.
27	$\overline{\text{CL 6}}$	50	−2.0			Input for a TTL compatible 6 MHz system clock.
28	NC					No connection.
29	$\overline{\text{RESET}}$	20	−0.4			A LOW on this input (for 0.1μs min.) resets the fault detection and internal circuitry of the BUS-66111 Hybrid.
30	NC					No connection.
31	NC					No connection.
32	NC					No connection.
33	BCU FAIL			−0.4	4.0	A HIGH on this output indicates a fault condition occured during the normal BCU operation.
34	A FAULT	20	−0.4			A HIGH on this input indicates a fault during the loop back on Bus A. This signal sets the BCU Fail Register.
35	B FAULT	20	−0.4			A HIGH on this input indicates a fault during the loop back on Bus B. This signal sets the BCU Fail Register.
36	$\overline{\text{A VALID WORD}}$	20	−0.4			A LOW on this input indicates that the BCU received a valid word on Bus A.

NOTES: In the above table, the symbols are defined as follows:
I_{IH}=maximum input HIGH current with V_{in}=2.5 volts.
I_{IL}=maximum input LOW current with V_{in}=0.4 volts.
I_{OH}=maximum output HIGH current with V_{out}=2.5 volts minimum.
I_{OL}=maximum output LOW current with V_{out}=0.4 volts maximum.

BUS-66106 PIN FUNCTION AND LOADING TABLE

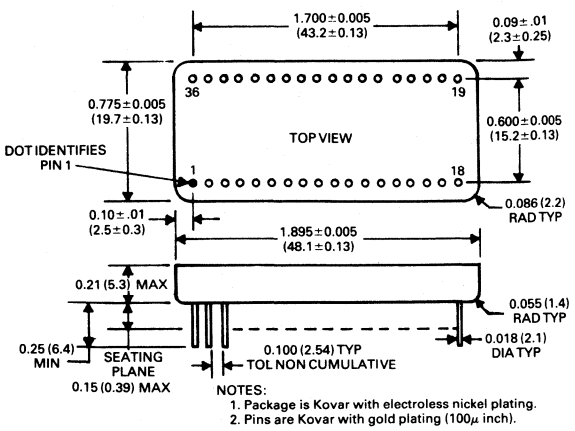
PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
1	+5V DC					+5V power input.
2	$\overline{\text{BC OUTPUT ENABLE}}$			−0.4	4.0	A LOW on this output indicates that the Bus Controller is transferring data into the subsystem
3	$\overline{\text{BC ACCESS}}$			−0.36	3.6	A LOW on this output indicates that the Bus Controller is using the Data and Address Tri-State buses.
4	NC					No connection.
5	CASE					Case connection.
6	$\overline{\text{CL 6}}$	20	−0.4			Input for a 6 MHz system clock, TTL compatible.
7	$\overline{\text{START}}$	20	−0.4			A LOW on this input initiates a word transfer by the hybrid.
8	$\overline{\text{BC LOAD}}$			−0.38	3.6	A LOW pulse on this output loads the data to be transmitted on the Encoder Registers.
9	$\overline{\text{R STROBE}}$	20	−0.4			A LOW pulse on this input starts a sequence to unload the data from the decoder register.
10	BUS CYCLE ENABLE	20	−0.4			A HIGH on this input from the subsystem will initiate a command/response sequence.
11	RECLOCKED CYCLE ENABLE			−0.38	3.6	This output is the Cycle Enable Signal synchronized with the 6 MHz clock.
12	BC NO DT			−0.4	0.4	This output is the NO DT input synchronized with the 6 MHz clock.
13	$\overline{\text{BC ACTIVE}}$			−0.4	4.0	A LOW on this output indicates that the device is processing a message.
14	A6			−1.2	12	MSB of 6 Bit Tri-State Address Bus.
15	A4			−1.2	12	Part of 6 Bit Tri-State Address Bus.
16	A2			−1.2	12	Part of 6 Bit Tri-State Address Bus.
17	$\overline{\text{T BUSY PULSE}}$			−0.4	4.0	A LOW level pulse that follows the trailing edge of $\overline{\text{T BUSY}}$.
18	$\overline{\text{BC CS}}$			−0.4	4.0	A LOW on this output selects a memory device.
19	$\overline{\text{BC WR}}$			−0.4	4.0	A LOW on this output transfers the data to the memory.
20	$\overline{\text{BG ACK}}$			−0.36	3.2	A LOW on this output handshake signal indicates that the device received the B GRANT signal.
21	NC					No connection.
22	COMPLETE			−0.4	4.0	A HIGH on this output indicates that the word transfer cycle is complete.
23	$\overline{\text{COMPLETE}}$			−0.36	3.2	This is the COMPLETE output inverted.
24	BC CMD 10			−0.36	3.2	This is the T/$\overline{\text{R}}$ bit of the Command Word transmitted.
25	NC					No connection.
26	$\overline{\text{BC R ENABLE}}$			−0.4	4.0	A LOW on this output enables the Decoder Register contents onto the internal 16 Bit Data Highway.
27	$\overline{\text{BC SOM}}$	20	−0.4			A LOW on this input resets the internal circuitry of the Hybrid.
28	NO DT	20	−0.4			A LOW on this IDLE/$\overline{\text{ACTIVE}}$ input indicates that the Data Bus Receiver is active.
29	$\overline{\text{BC TIMEOUT}}$			−0.4	4.0	A LOW on this output indicates that there was no reply from the RTU within 15μs.
30	$\overline{\text{T BUSY}}$	20	−0.4			Input to the negative edge triggered circuit which generates $\overline{\text{T BUSY PULSE}}$ output.
31	A5			−1.2	12	Part of 6 Bit Tri-State Address Bus.
32	A3			−1.2	12	Part of 6 Bit Tri-State Address Bus.
33	A1			−1.2	12	LSB of 6 Bit Tri-State Address Bus.
34	GND					Power and logic return.

BUS-66106 PIN FUNCTION AND LOADING TABLE (CONTINUED)

PIN NO.	NAME	I_{IH} (μA)	I_{IL} (mA)	I_{OH} (mA)	I_{OL} (mA)	DESCRIPTION
35	$\overline{\text{STAT SET}}$			−0.4	4.0	A LOW pulse on this output indicates a bit set or address mismatch in the Status Word received.
36	$\overline{\text{BC T ENABLE}}$	20	−0.4			This is one of a group of four Bus Controller mode code signals. A LOW on this input enables the transmit cycle.
37	$\overline{\text{BC REPLY}}$	−40	0.8			This is one of a group of four Bus Controller mode signals. A LOW on this input enables the reply cycle.
38	$\overline{\text{BUS REQUEST}}$			−0.38	3.6	A LOW on this handshake output signal indicates a request to access the Tri-State Data and Address Buses.
39	D 13	20	−0.2			Part of 16 Bit Tri-State Data input
40	D 15	20	−0.2			MSB of 16 Bit Tri-State Data input.
41	D 9	20	−0.2			Part of 16 Bit Tri-State Data input.
42	D 11	20	−0.2			Part of 16 Bit Tri-State Data input.
43	$\overline{\text{CTW3}}$			−0.4	4.0	Part of 8 Bit Control Word Register output.
44	$\overline{\text{CTW1}}$			−0.4	4.0	Part of 8 Bit Control Word Register. A LOW indicates a Broadcast Command.
45	$\overline{\text{CTW7}}$			−0.4	4.0	MSB of 8 Bit Control Word Register output. A LOW output selects MIL-STD-1553 Channel A.
46	$\overline{\text{CTW5}}$			−0.4	4.0	Part of 8 bit Control Word Register output.
47	D4	20	−0.2			Part of 16 bit Tri-State Data input.
48	D6	20	−0.2			Part of 16 bit Tri-State Data input.
49	D0	20	−0.2			LSB of 16 bit Tri-State Data input.
50	D2	20	−0.2			Part of 16 bit Tri-State Data input.
51	+5V					+5V Power supply.
52	GND					Power and logic return.
53	$\overline{\text{BC DT}}$	40	−0.8			This is one of a group of four Bus Controller mode signals. A LOW on this input indicates Data Word transfer on the Data Bus.
54	$\overline{\text{BC LOAD}}$	40	−0.8			This is one of a group of four Bus Controller mode signals. A LOW on this input indicates a Data Word to be loaded in the Encoder.
55	$\overline{\text{B GRANT}}$	20	−0.4			A LOW on this input indicates that the subsystem relinquished control of the Tri-State Buses.
56	D 12	20	−0.2			Part of 16 Bit Tri-State Data input.
57	D 14	20	−0.2			Part of 16 Bit Tri-State Data input.
58	D 8	20	−0.2			Part of 16 Bit Tri-State Data input.
59	D 10	20	−0.2			Part of 16 Bit Tri-State Data input.
60	BC L WORD			−0.4	4.0	A HIGH on this output indicates that the last Data Word has been transferred.
61	$\overline{\text{CTW2}}$			−0.4	4.0	Part of 8 Bit Control Word Register output. A LOW indicates a Mode Code Command.
62	$\overline{\text{CTW0}}$			−0.4	4.0	LSB of 8 Bit Control Word Register. A LOW indicates an RT to RT Command.
63	$\overline{\text{CTW6}}$			−0.4	4.0	Part of 8 Bit Control Word Register output.
64	$\overline{\text{CTW4}}$			−0.4	4.0	Part of 8 Bit Control Word Register output.
65	D 5	20	−0.2			Part of 16 Bit Tri-State Data input.
66	D 7	20	−0.2			Part of 16 Bit Tri-State Data input.
67	D 1	20	−0.2			Part of 16 Bit Tri-State Data input.
68	D 3	20	−0.2			Part of 16 Bit Tri-State Data input.

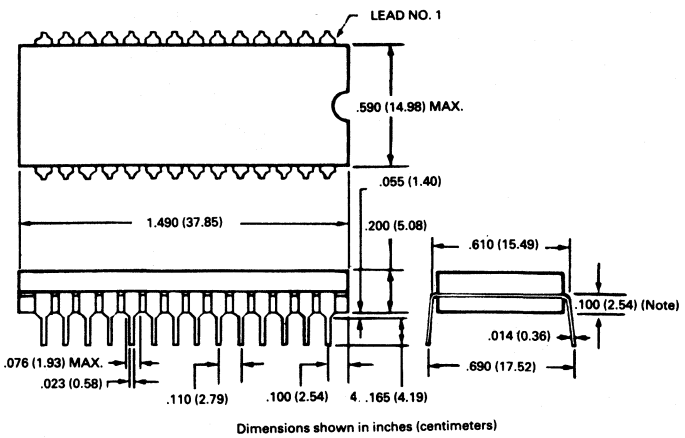
See notes following BUS-66111 Pin Function Table.

MECHANICAL OUTLINE BUS-66111



NOTES:
1. Package is Kovar with electroless nickel plating.
2. Pins are Kovar with gold plating (100μ inch).

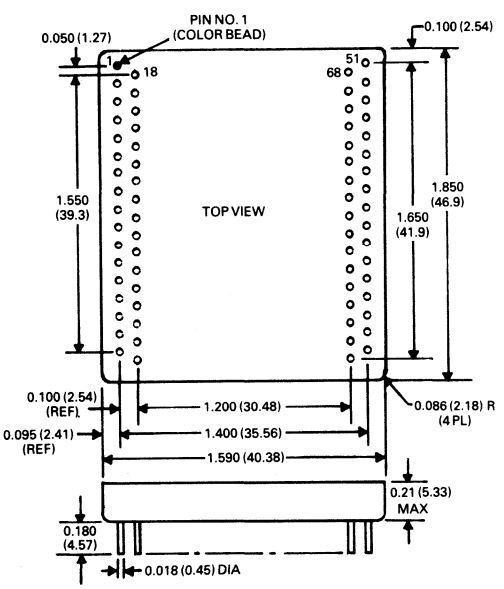
MECHANICAL OUTLINE #464340040017



Dimensions shown in inches (centimeters)

MECHANICAL OUTLINE BUS-66106

Dimensions are in inches (millimeters)



ORDERING INFORMATION

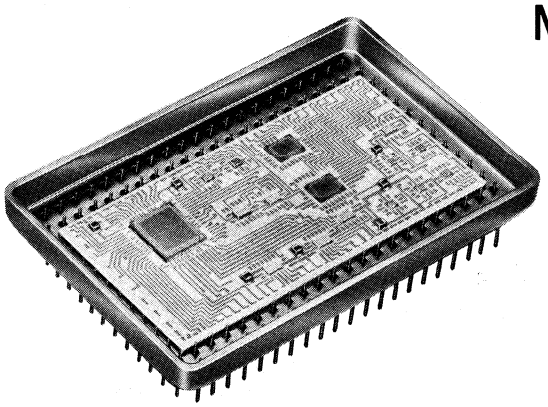
BUS-66111-883B
BUS-66106-883B

MIL-STD-883 Processing:
883B=Conforms to MIL-STD-883 DDC Procedures
Blank=Same, except burn-in is omitted

#464340040037 State Sequencer PLS

The information provided in this Data Sheet is believed to be accurate; however, no responsibility is assumed by ILC Data Device Corporation for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.

MIL-STD-1553 RTU PROTOCOL HYBRID



DESCRIPTION

BUS-66108 generates the complete protocol, timing and control functions required by a dual redundant MIL-STD-1553 Remote Terminal Unit (RTU). It provides decoding and response to 13 mode codes with no subsystem intervention required. Any combination of mode codes can be illegalized with the use of an external PROM. The BUS-66108 subsystem interface is simple and easy to use. It provides a selectable 8 bit or 16 bit data highway I/O with drive capability of 7 TTL loads. Data transfers are accomplished with a DMA type control handshaking. Separate latched outputs are provided for Command Word and Word Count.

The BUS-66108 provides channel selection and control, and multiplexing for dual MIL-STD-1553 Dumb RTUs, as well as Bus Controller (BC) Protocol circuits. In addition, it provides complete message validation, fail-safe timeout, and BIT fault processing. BUS-66108 is packaged in a 107 pin 1.6 x 2.4 inch hermetic hybrid. It operates over the −55°C to +125°C temperature range.

A complete dual redundant RTU/BC may be implemented with just four standard product DDC hybrids. The hybrid set includes: two BUS-65102 Dumb RTU hybrids, a BUS-66108 RTU Protocol hybrid, and a BUS-66106 BC Protocol hybrid.

FEATURES

- *GENERATES COMPLETE PROTOCOL TIMING AND CONTROL FOR MIL-STD-1553 REMOTE TERMINAL UNIT*
- *SUPPORTS 13 MODE CODES – ANY COMBINATION CAN BE ILLEGALIZED*
- *TRANSFERS DATA WITH DMA TYPE HANDSHAKING*
- *8 BIT OR 16 BIT DATA HIGHWAY INTERFACE WITH 7 TTL LOAD DRIVE CAPABILITY*
- *LATCHED OUTPUTS FOR COMMAND WORD AND WORD COUNT*
- *INTERFACES DIRECTLY WITH STANDARD PRODUCT DUMB RTU HYBRID AND BC PROTOCOL HYBRID FOR COMPLETE RTU/BC IMPLEMENTATION*
- *BIT WORD REGISTER*

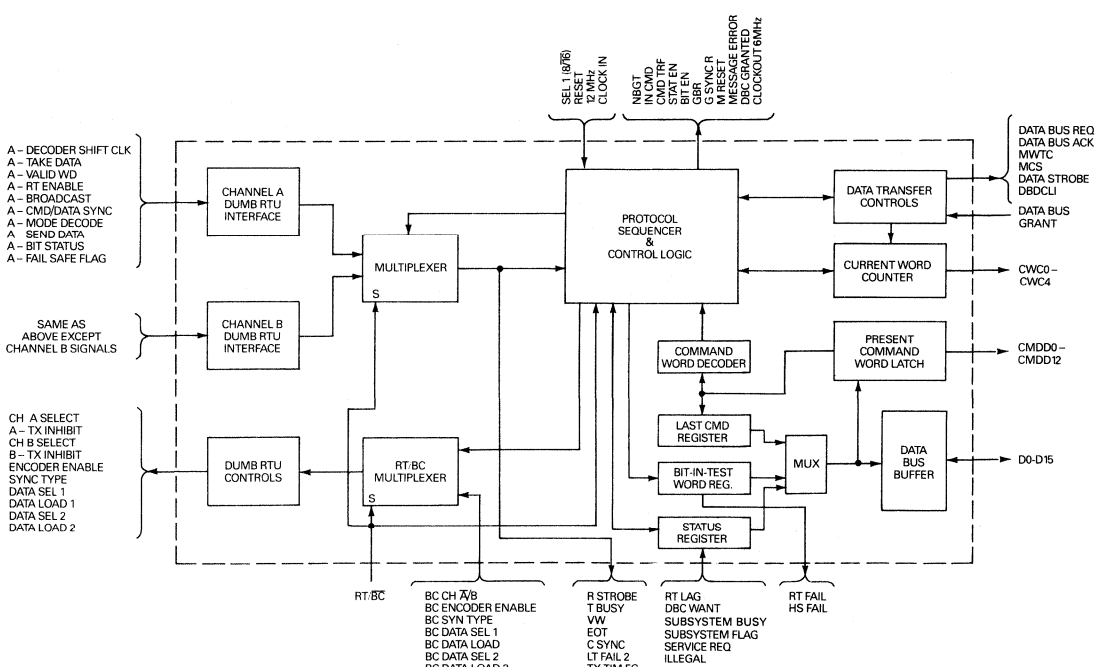


FIGURE 1. BUS-66108 BLOCK DIAGRAM

SPECIFICATIONS

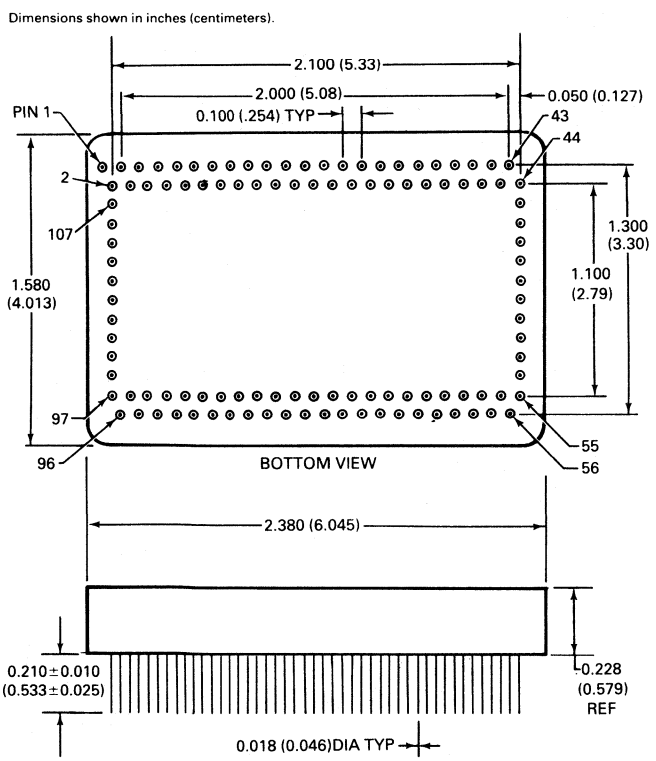
Values at nominal power supply voltage over the operating temperature range.

PARAMETER	UNITS	VALUE
LOGIC*		
Category A (CMOS Inputs)		
V_{IH}	V	2.4 min
V_{IL}	V	0.8 max
I_{IH} @ V_{IH} = 2.7V	µA	10 max
I_{IL} @ V_{IL} = 0.4V	µA	10 max
Category B (CMOS Outputs)		
V_{OH} @ I_{OH} = 360µA	V	2.4 min
V_{OL} @ I_{OL} = 1.6mA	V	0.4 max
Category C (CMOS Outputs)		
V_{OH} @ I_{OH} = 360µA	V	2.4 min
V_{IL} @ I_{OL} = 1.2mA	V	0.4 max
Category D (LS TTL Inputs)		
V_{IH}	V	2.0 min
V_{IL}	V	0.7 max
I_{IH} @ V_{IH} = 2.7V	µA	20 max
I_{IL} @ V_{IL} = 0.4V	µA	400 max
Category E (LS TTL Inputs)		
V_{IH}	V	2.0 min
V_{IL}	V	0.7 max
I_{IH}	µA	20 max
I_{IL}	µA	200 max
Category F (LS TTL Outputs)		
V_{OH} @ I_{OH} = 400µA	V	2.4 min
V_{OL} @ I_{OL} = 4mA	V	0.4 max
Category G (LS TTL Outputs)		
V_{OH} @ I_{OH} = 3mA	V	2.4 min
V_{OL} @ I_{OL} = 12mA	V	0.4 max

PARAMETER	UNITS	VALUE
Category H (LS TTL Bi-directional)		
V_{OH} @ I_{OH} = 3mA	V	2.4 min
V_{OL} @ I_{OL} = 12mA	V	0.4 max
V_{IH}	V	2.0 min
V_{IL}	V	0.7 max
I_{IH} @ V_{IH} = 2.7V	µA	40 max
I_{IL} @ V_{IL} = 0.4V	µA	400 max
Category I (CMOS/LS Input)		
V_{IH}	V	2.4 min
V_{IL}	V	0.7 max
I_{IH} @ V_{IH} = 2.7V	µA	90 max
I_{IL} @ V_{IL} = 0.4V	µA	1200 max
POWER SUPPLY CHARACTERISTICS		
Voltage	V	+5.0 ±10%
Current	mA	370 typ 500 max
TEMPERATURE RANGE		
Operating (Case)	°C	−55 to +125
Storage	°C	−65 to +150
PHYSICAL CHARACTERISTICS		
Size	in	2.4 x 1.6 x 0.23 (6.1 x 4 x 0.6cm)
Weight	oz.	2.5 (71g)

* See Pin Function Table for signals in each Logic Category.

MECHANICAL OUTLINE BUS-66108



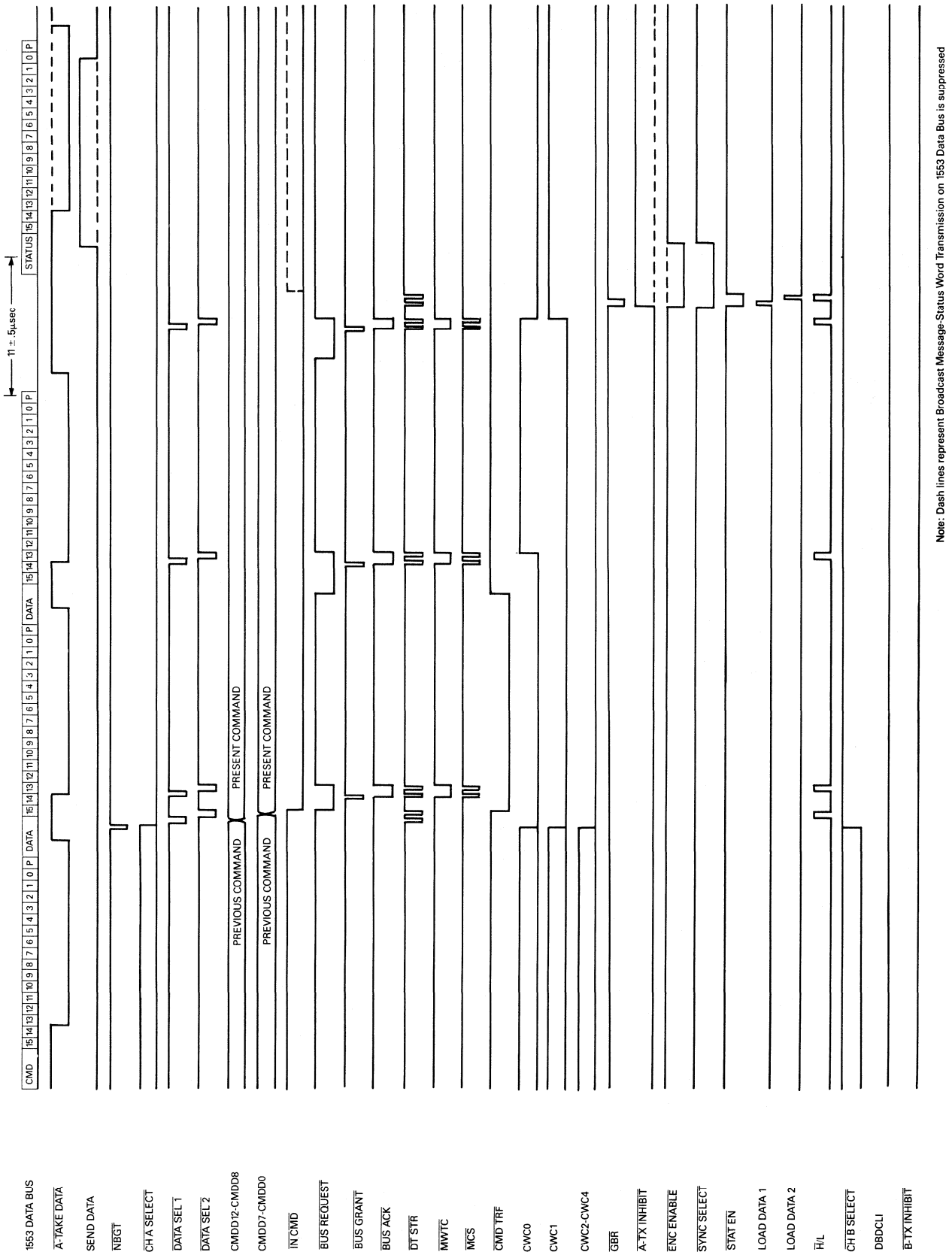


FIGURE 2. RECEIVE TWO WORDS (8 BIT, CHANNEL A)

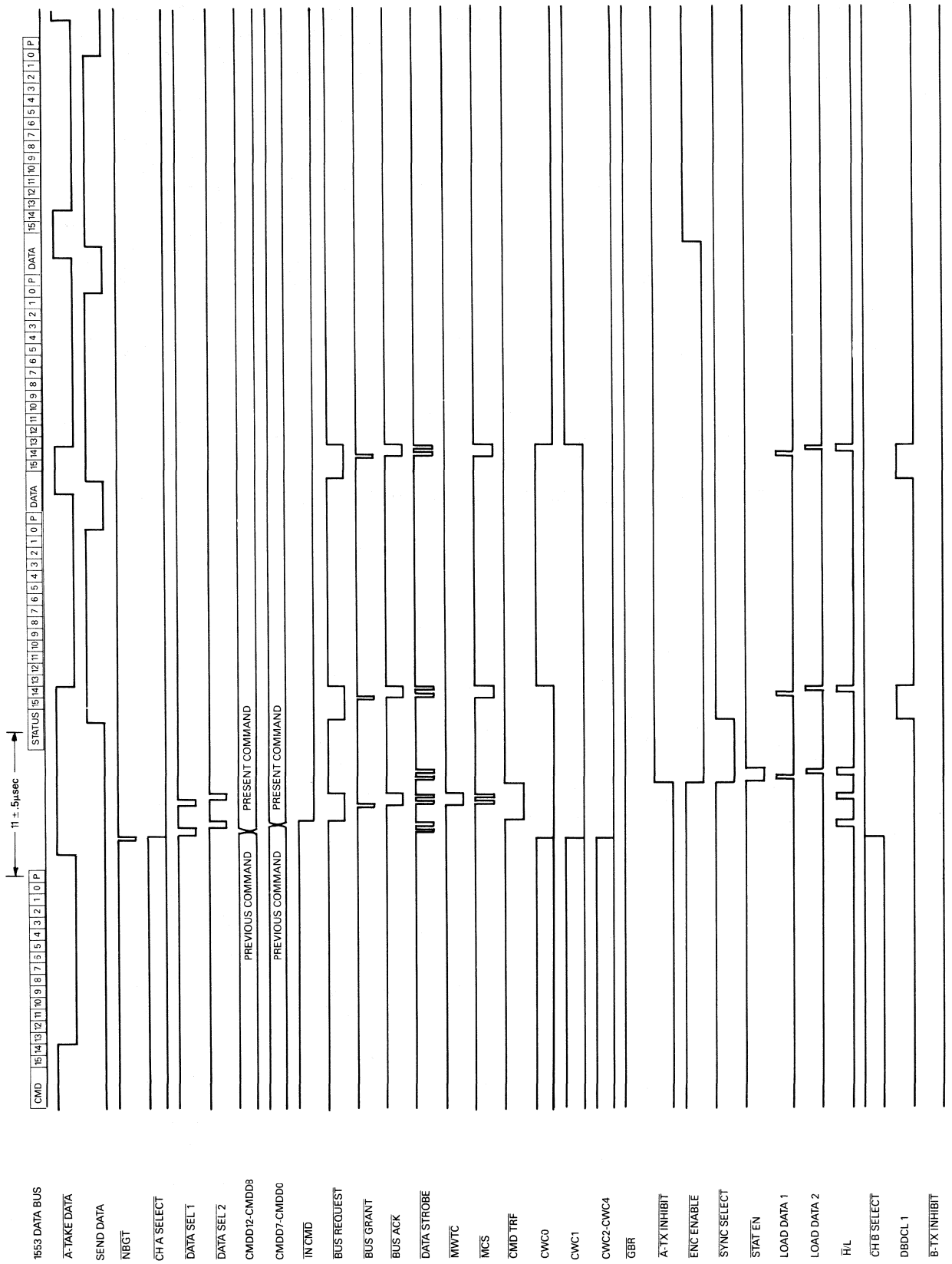
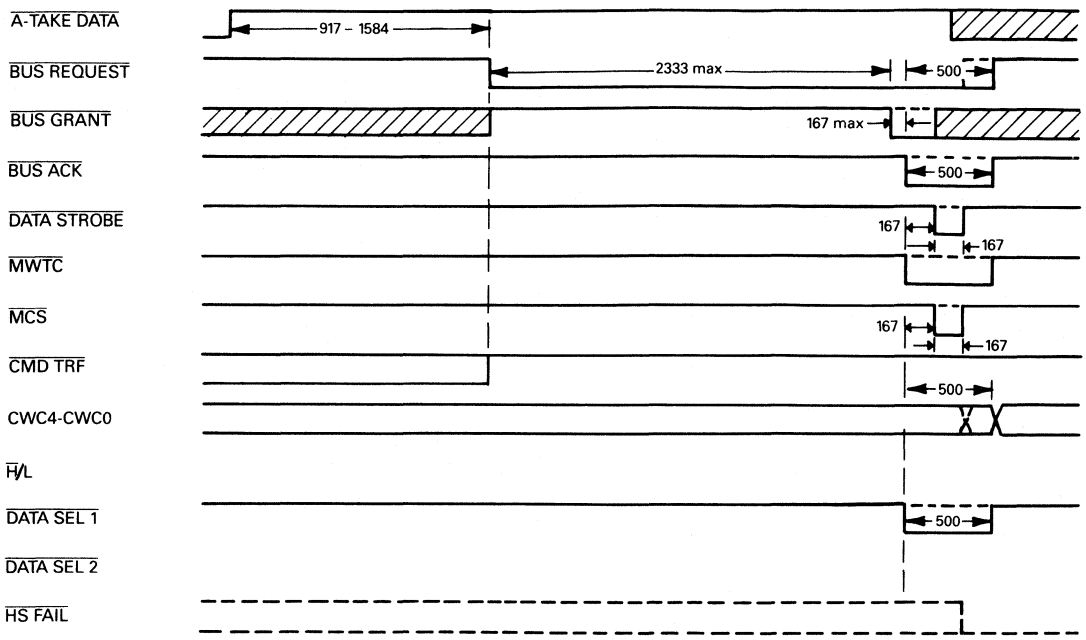
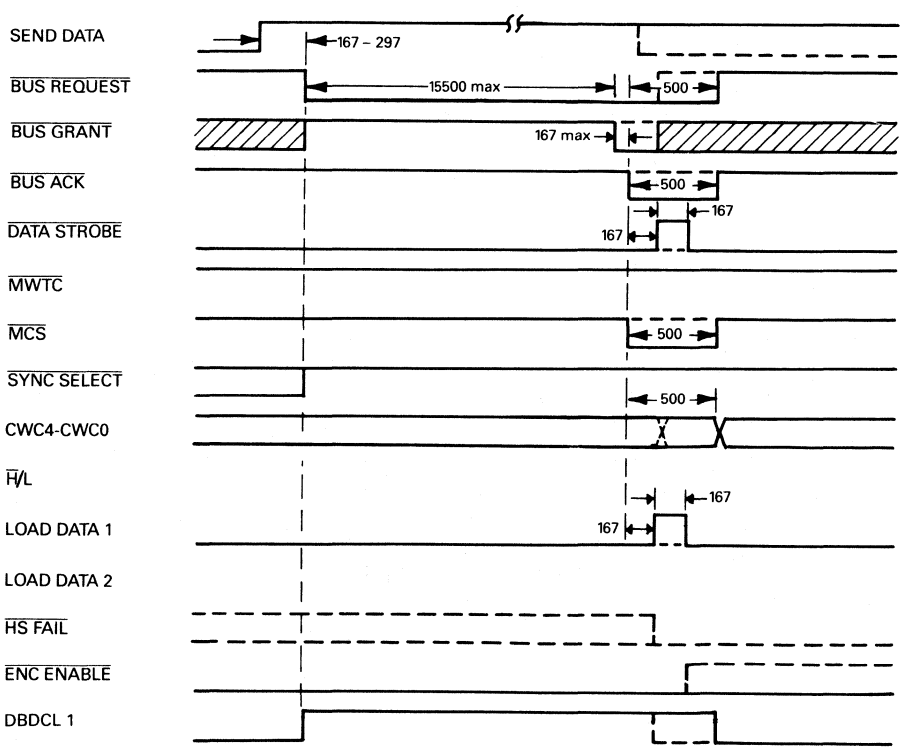


FIGURE 3. TRANSMIT TWO WORDS (8 BIT, CHANNEL A)



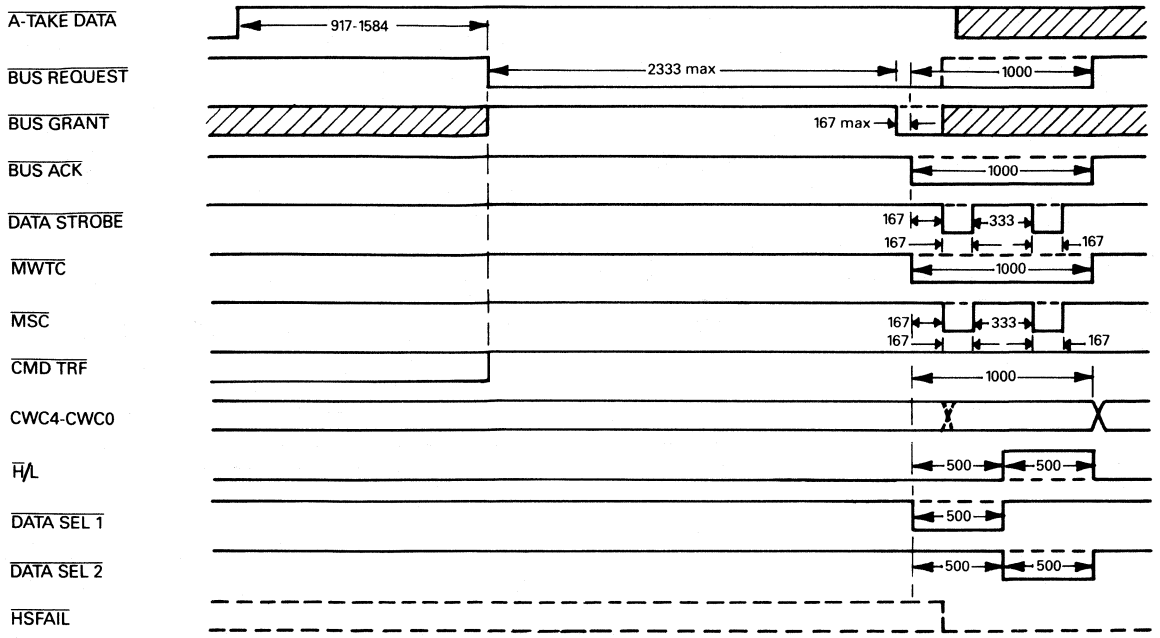
Note: All timing intervals are in nanoseconds

FIGURE 4. RECEIVE DATA HANDSHAKE SEQUENCE (16 BIT DATA)



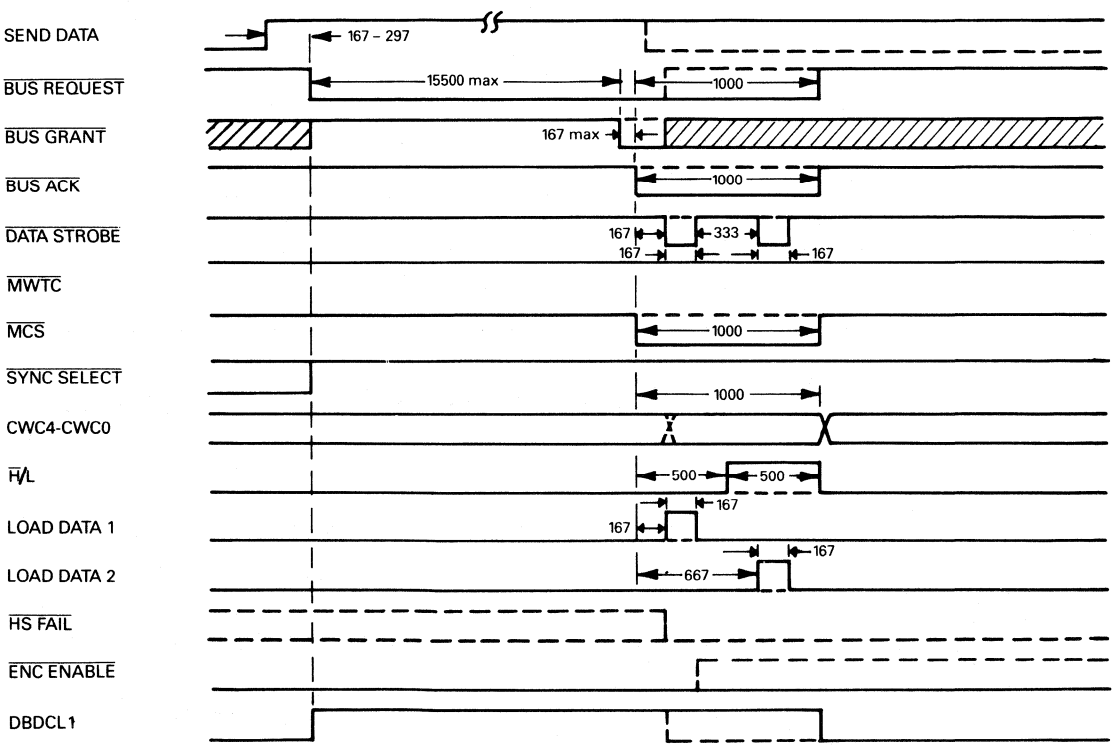
Note: All timing intervals are in nanoseconds

FIGURE 5. TRANSMIT DATA HANDSHAKE SEQUENCE (16 BIT DATA)



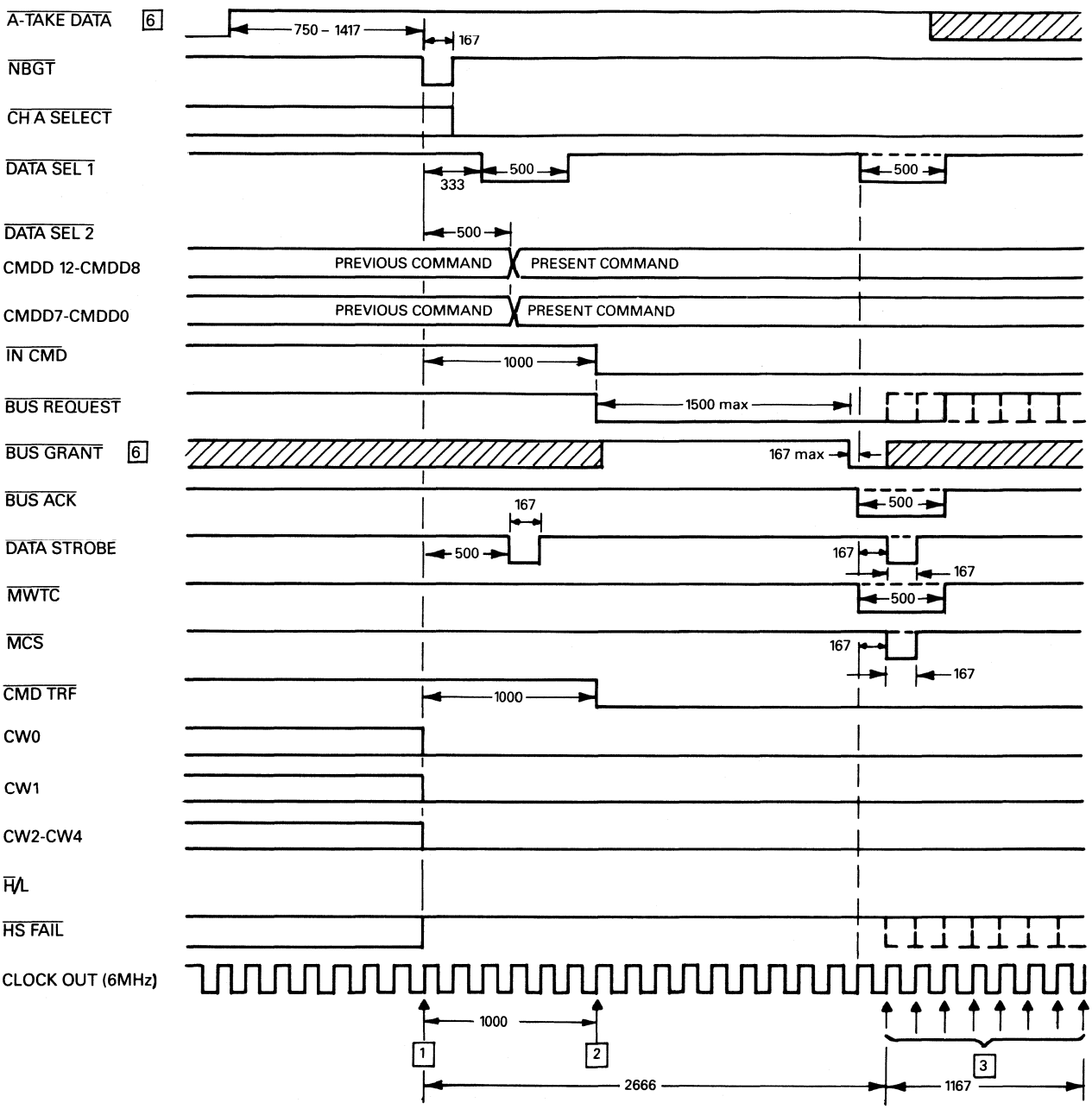
Note: All timing intervals are in nanoseconds

FIGURE 6. RECEIVE DATA HANDSHAKE SEQUENCE (8 BIT DATA)



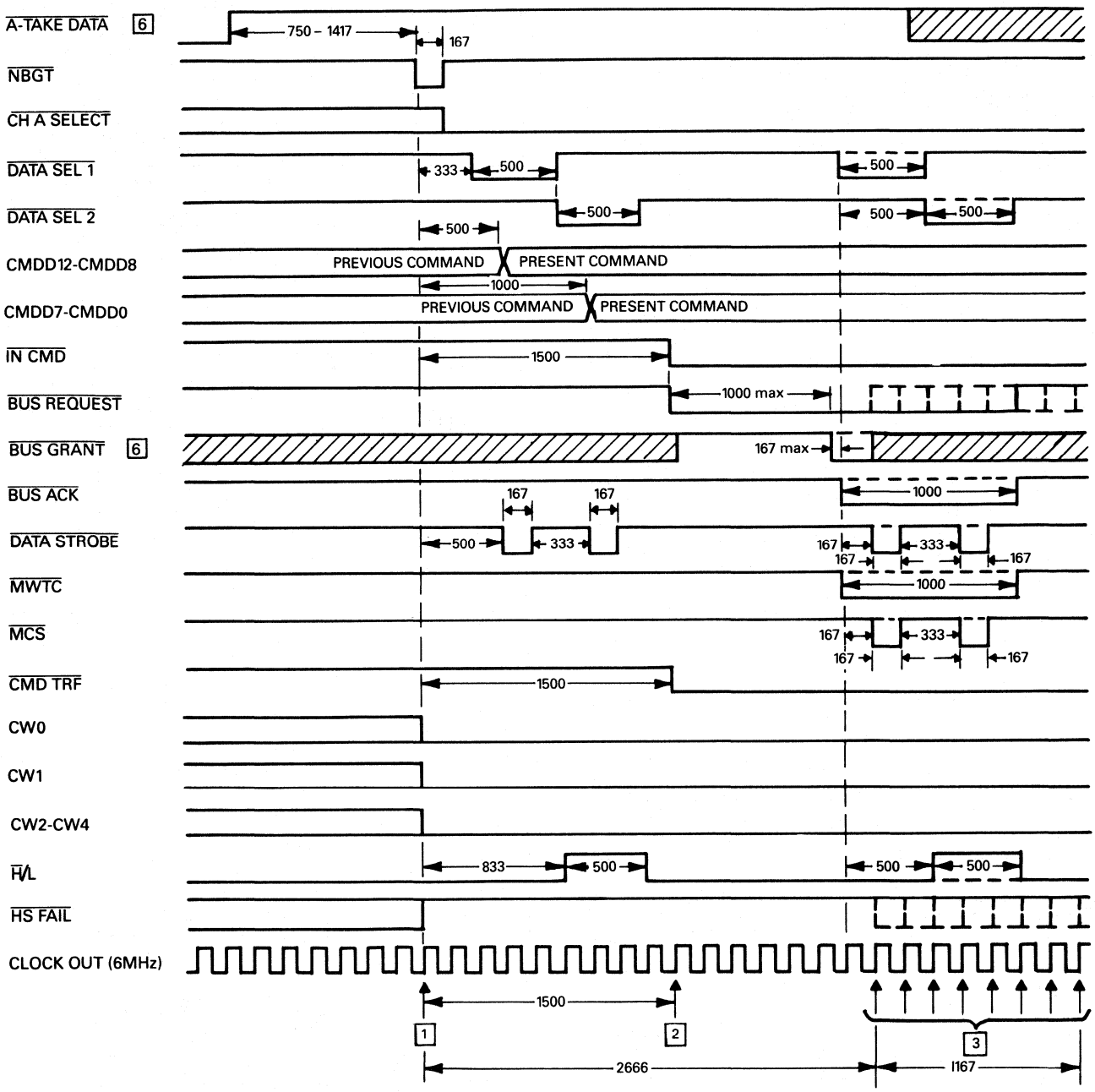
Note: All timing intervals are in nanoseconds

FIGURE 7. TRANSMIT DATA HANDSHAKE SEQUENCE (8 BIT DATA)



NOTES:
1 – Start of Command Word Servicing
2 – ILLEGAL Input strobed in here
3 – RT FLAG, DCB WANTED, SUBSYSTEM FLAG, SUBSYSTEM BUSY & SERVICE REQUEST inputs are strobed in on one of the rising clock edges
4 – Dash lines represent sequence if BUS GRANT was not given in time. Maximum allowable time for BUS GRANT in response to BUS REQUEST for the Command Word Transfer is 1μsec for 8 bit operation or 1.5μsec for 16 Bit.
5 – All time intervals are typical value specified in nanoseconds
6 – A-TAKE DATA & BUS GRANT are inputs

FIGURE 8. COMMAND WORD SEQUENCE (16 BIT DATA)



NOTES:
1 – Start of Command Word Servicing
2 – ILLEGAL input strobed in here
3 – RT FLAG, DBC WANTED, SUBSYSTEM FLAG, SUBSYSTEM BUSY & SERVICE REQUEST inputs are strobed in on one of the rising clock edges
4 – Dash lines represent sequence if BUS GRANT was not given in time. Maximum allowable time for BUS GRANT in response to BUS REQUEST for the Command Word Transfer in 1μsec for 8 bit operation or 1.5μsec for 16 bit.
5 – All time intervals are typical value specified in nanoseconds
6 – A-TAKE DATA & BUS GRANT are inputs

FIGURE 9. COMMAND WORD SEQUENCE (8 BIT DATA)

BUS-66108 PIN FUNCTION TABLE

PIN	NAME	DESCRIPTION	LOG. CAT.*
1	CASE	Caseground	–
2	A CMD/$\overline{\text{DATA}}$ SYNC	A HIGH on this input indicates receipt of a Command or Status Word on Bus A. A LOW indicates receipt of a Data Word on Bus A.	A
3	A $\overline{\text{VALID WORD}}$	A LOW on this input indicates receipt of a valid word on Bus A.	A
4	A $\overline{\text{MODE DECODE}}$	A LOW on this input indicates receipt of a receipt of a valid Command Word whose subaddress field contains all 1's or 0's on Bus A.	A
5	A RT ENABLE	A HIGH on this input indicates receipt of a valid Command Word containing the correct 5 bit terminal address plus address parity on Bus A.	A
6	A BROADCAST	A HIGH on this input indicates receipt of a valid Command Word whose address field contains all 1's on Bus A.	A
7	A SEND DATA	A HIGH on this input indicates that the transmit cycle data shifting is occurring on Bus A.	A
8	A $\overline{\text{BIT STATUS}}$	A LOW on this input, during wrap-around self-test only, indicates that the last word decoded was identical to the last word encoded on Bus A.	A
9	A FAIL-SAFE	A HIGH on this input indicates that a transmitted message has exceeded 768μs and that transmission has been terminated on Bus A.	A
10	B $\overline{\text{TAKE DATA}}$	A LOW on this input indicates that the received data is being shifted into the decoder output register and is available at Serial Data Output on Bus B.	A
11	B DSC	LOW to HIGH transitions on this 1MHz clock input, when $\overline{\text{TAKE DATA}}$ is LOW, causes decoder cycle data shifting to occur on Bus B.	A
12	B CMD/$\overline{\text{DATA}}$ SYNC	A HIGH on this input indicates receipt of a Command or Status Word on Bus B. A LOW indicates receipt of a Data Word on Bus B.	A
13	B $\overline{\text{VALID WORD}}$	A LOW on this input indicates receipt of a valid word on Bus B.	A
14	B $\overline{\text{MODE DECODE}}$	A LOW on this input indicates receipt of a valid Command Word whose sub-address field contains all 1's or all 0's on Bus B.	A
15	B RT ENABLE	A HIGH on this input indicates receipt of a valid Command Word containing the correct 5 bit terminal address plus address parity on Bus B.	A
16	B BROADCAST	A HIGH on this input indicates receipt of a valid Command Word whose address field contains all 1's on Bus B.	A
17	B SEND DATA	A HIGH on this input indicates that the transmit cycle data shifting is occurring on Bus B.	A
18	B $\overline{\text{BIT STATUS}}$	A LOW on this input, during wrap-around self-test only, indicates that the last word decoded was identical to the last word encoded on Bus B.	A
19	B FAIL-SAFE	A HIGH on this input indicates that a transmitted message has exceeded 768μs and that transmission has been terminated on Bus B.	A
20	B $\overline{\text{TX INHIBIT}}$	A LOW on this output inhibits the transmitter on Bus B.	B
21	A $\overline{\text{TX INHIBIT}}$	A LOW on this output inhibits the transmitter on Bus A.	B
22	BC CH$\overline{\text{A}}$/B	A LOW on this input, when RT/$\overline{\text{BC}}$ is LOW, causes pin 91 $\overline{\text{CH A SELECT}}$ output to go LOW. A HIGH on this input, when RT/BC is LOW; causes pin 92 $\overline{\text{CH B SELECT}}$ to go LOW.	D
23	$\overline{\text{ENC ENABLE}}$	A LOW on this output causes the encoding cycle to start at the next HIGH to LOW transition of ESC.	F
24	$\overline{\text{BC ENC ENABLE}}$	A LOW on this input, when RT/$\overline{\text{BC}}$ is LOW, causes pin 23 $\overline{\text{ENC ENABLE}}$ output to go LOW.	D
25	$\overline{\text{SYNC SELECT}}$	A HIGH on this output results in a transmitted Data Sync. A LOW on this output results in a transmitted Command or Status Sync.	F
26	$\overline{\text{BC SYNC SELECT}}$	A LOW on this input, when RT/$\overline{\text{BC}}$ is LOW, causes pin 25 $\overline{\text{SYNC SELECT}}$ output to go LOW.	D

BUS-66108 PIN FUNCTION TABLE (CONTINUED)

PIN	NAME	DESCRIPTION	LOG. CAT.*
27	$\overline{\text{BC LOAD DATA 1}}$	A LOW on this input, when RT/$\overline{\text{BC}}$ is LOW, causes pin 90 LOAD DATA 1 output to go HIGH.	D
28	$\overline{\text{DATA SEL 1}}$	A negative pulse on this output, when 8/$\overline{16}$ is LOW, causes the decoder register output to appear on D0 through D15 of the parallel tri-state I/O. When 8/$\overline{16}$ is HIGH, a negative pulse causes the decoder Most Significant Byte to appear on D0 through D7.	F
29	$\overline{\text{BC DATA SEL 1}}$	A LOW on this input, when RT/$\overline{\text{BC}}$ is LOW, causes pin 28 $\overline{\text{DATA SEL 1}}$ output to go LOW.	D
30	$\overline{\text{IN CMD}}$	A LOW on this output indicates that the RTU is servicing a valid Command Word and CMDD0 thru CMDD12 are valid.	C
31	$\overline{\text{RT FAIL}}$	A LOW on this output indicates an RTU fault condition. Cleared on each Status transmission	B
32	$\overline{\text{NB GT}}$	A negative pulse on this output indicates the RTU is starting to service a valid Command Word.	B
33	$\overline{\text{CMD TRF}}$	A LOW on this output indicates the transfer of the Command Word to the subsystem.	B
34	$\overline{\text{BIT EN}}$	A LOW on this output indicates that the BIT WORD is on the tri-state data highway.	B
35	$\overline{\text{MESSAGE ERROR}}$	A LOW on this output indicates that a message error has occurred in the RTU reception.	B
36	$\overline{\text{HS FAIL}}$	A LOW on this output indicates that the subsystem did not provide a $\overline{\text{BUS GRANT}}$ input in time to transfer the Data or Command Word.	B
37	$\overline{\text{G SYNC R}}$	A negative pulse on this output indicates that a valid Synchronize Mode Code has been received.	B
38	$\overline{\text{STAT EN}}$	A LOW on this output indicates that the Status Word is on the tri-state data highway.	B
39	$\overline{\text{DBC GRANTED}}$	A LOW on this output indicates that the subsystem has accepted control of the 1553 data bus.	B
40	$\overline{\text{GBR}}$	A negative pulse on this output indicates that a good data block has been received and transferred to the subsystem.	B
41	$\overline{\text{M RESET}}$	A negative pulse on this output indicates the receipt of a valid Reset Mode Code.	B
42	SELECT 1 (8/$\overline{16}$)	A LOW on this input selects the 16 bit parallel data highway mode. A HIGH selects the 8 bit data highway.	I
43	$\overline{\text{DBC WANTED}}$	A LOW on this input indicates that the acceptance bit in the Status Word should be set if a Dynamic Bus Control Mode Code is received.	A
44	$\overline{\text{RT FLAG}}$	Input used to control the Terminal Flag Bit in the Status Register. If LOW when the status word is updated, the Terminal Flag will set, if HIGH, it will be cleared. Normally connected to $\overline{\text{RT FAIL}}$ (PIN 31).	A
45	$\overline{\text{SUBSYSTEM FLAG}}$	Input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated; the subsystem flag bit will be set, if HIGH; it will be cleared.	A
46	$\overline{\text{SUBSYSTEM BUSY}}$	Input from the subsystem used to control the busy bit in the status register. If LOWwhen the status word is updated, the busy bit is set, if HIGH, the busy bit will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will still be transferred to subsystem.	A
47	$\overline{\text{SERVICE REQUEST}}$	A LOW on this input, when the status word is updated, cuases the service request bit to be set in the Status Word.	A
48	$\overline{\text{ILLEGAL}}$	A LOW on this input causes the received command word to be treated as illegal. The Message Error Bit will be set in the status register. On received commands, $\overline{\text{GBR}}$ (PIN 40) will be masked, on Transmit Command, no data will be requested or transmitted.	A
49	CWC 0	LSB of the 5 bit current word count.	B

BUS-66108 PIN FUNCTION TABLE (CONTINUED)

PIN	NAME	DESCRIPTION	LOG. CAT.*
50	CWC 2	Part of the 5 bit current word count.	B
51	CWC 1	Part of the 5 bit current word count.	B
52	CWC 3	Part of the 5 bit current word count.	B
53	CMDD0	Part of the 13 bit Command Word output. (LSB of the word count field) valid during $\overline{\text{INCMD}}$.	B
54	CMDD2	Part of the 13 bit Command Word output. (Part of the word count field) Valid during $\overline{\text{INCMD}}$.	B
55	CMDD9	Part of the 13 bit Command Word output. (MSB of the subaddress field) Valid during $\overline{\text{INCMD}}$.	B
56	CMDD10	Part of the 13 bit Command Word output. (T/$\overline{\text{R}}$ bit) Valid during $\overline{\text{INCMD}}$.	B
57	CMDD11	Part of the 13 bit Command Word output. (A HIGH indicates a received Broadcast Command) Valid during $\overline{\text{INCMD}}$.	B
58	CWC4	MSB of the 5 bit current word count.	B
59	CMDD1	Part of the 13 bit Command Word output. (Part of the word count field) Valid during $\overline{\text{INCMD}}$.	B
60	CMDD3	Part of the 13 bit Command Word output. (Part of the word count field) Valid during $\overline{\text{INCMD}}$.	B
61	CMDD4	Part of the 13 bit Command Word output. (MSB of the word count field) Valid during $\overline{\text{INCMD}}$.	B
62	CMDD5	Part of the 13 bit Command Word output. (LSB of the subaddress field) Valid during $\overline{\text{INCMD}}$.	B
63	CMDD6	Part of the 13 bit Command Word output. (Part of the subaddress field) Valid during $\overline{\text{INCMD}}$.	B
64	CMDD7	Part of the 13 bit Command Word output. (Part of the subaddress field) Valid during $\overline{\text{INCMD}}$.	B
65	CMDD8	Part of the 13 bit Command Word output. (Part of the subaddress field) Valid during $\overline{\text{INCMD}}$.	B
66	CMDD12	Part of the 13 bit Command Word output. (A HIGH indicates a received Mode Command) Valid during $\overline{\text{INCMD}}$.	B
67 thru 82	D 15 thru D 0**	MSB through LSB of parallel tri-state data highway.	H
83	$\overline{\text{VW}}$	A LOW on this output, when RT/$\overline{\text{BC}}$ is LOW, indicates the selected data bus channel $\overline{\text{VALID WORD}}$ went LOW.	B
84	$\overline{\text{T BUSY}}$	A LOW on this output, when RT/$\overline{\text{BC}}$ is LOW, indicates the selected data bus channel SEND DATA went HIGH.	B
85	$\overline{\text{TX TIM FG}}$	A LOW on this output indicates that the transmitter has been shut down due to fail-safe timeout.	B
86	$\overline{\text{LT FAIL 2}}$	A negative pulse on this output indicates that the last word transmitted contained an error.	B
87	CLOCK IN	12 MHz clock input.	E
88	+5V	+5 VDC power supply input.	–
89	GND	Ground.	–
90	LOAD DATA 1	A positive pulse on this output, when 8/$\overline{\text{16}}$ is LOW, causes the data word to be transferred to the encoder register. When 8/$\overline{\text{16}}$ is HIGH, a positive pulse causes the Most Significant Byte to be transferred to the encoder register.	G
91	$\overline{\text{CH A SELECT}}$	A LOW on this output causes the Bus A encoder/decoder to be enabled.	G
92	$\overline{\text{CH B SELECT}}$	A LOW on this output causes the Bus B encoder/decoder to be enabled.	G
93	DBDCL1	A HIGH on this output indicates that a data transfer from sybsystem to RTU has been requested but not yet completed. Otherwise this output is LOW. This output indicates direction of data bus transfer.	G
94	$\overline{\text{MCS}}$	A negative pulse on this output indicates that valid data is on the parallel tri-state data highway.	F
95	$\overline{\text{BUS ACK}}$	A LOW on this output indicates that data is on the parallel tri-state data highway.	G
96	$\overline{\text{BUS REQUEST}}$	A LOW on this output indicates to the subsystem that the RTU has data to transfer.	G

BUS-66108 PIN FUNCTION TABLE (CONTINUED)

PIN	NAME	DESCRIPTION	LOG. CAT.*
97	$\overline{\text{BUS GRANT}}$	A LOW on this input causes the RTU data to be transferred to the subsystem.	D
98	$\overline{\text{MWTC}}$	A LOW on this output, when $\overline{\text{BUS ACK}}$ is LOW, indicates that data will be transferred from the RTU to the subsystem.	F
99	RT/$\overline{\text{BC}}$	A LOW on this input selects the Bus Controller operating mode. A HIGH selects the Remote Terminal mode.	E
100	$\overline{\text{R STROBE}}$	A negative pulse on this output, when RT/$\overline{\text{BC}}$ is LOW, indicates that a new word was received.	F
101	C SYNC	A HIGH on this output indicates that the word being transferred over the selected data bus has a Command Sync.	G
102	EOT	A HIGH on this output indicates end of transmission.	G
103	CLOCK OUT	6 MHz clock output.	G
104	$\overline{\text{DATA STROBE}}$	A negative pulse on this output indicates that data is on the parallel tri-state data highway.	G
105	$\overline{\text{RESET}}$	A LOW on this input causes initialization of the RTU.	E
106	A $\overline{\text{TAKE DATA}}$	A LOW on this input indicates that the received data is being shifted into the decoder output register and is available at Serial Data Output on Bus A.	A
107	A DSC	LOW to HIGH transitions on this 1MHz clock input, when $\overline{\text{TAKE DATA}}$ is LOW, causes decoder cycle data shifting to occur on Bus A.	A

* See Specification Table for values in each Logic Category.

** If SELECT 1 (PIN 42) is LOW, then D15 thru D0 appear on pins 67 thru 82.

If SELECT 1 (PIN 42) is HIGH, then pins 67 thru 82 have the following function:

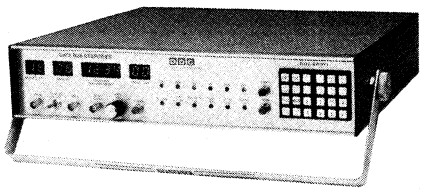
67 68 69	–	No Connection
70	$\overline{\text{BC DATA SEL 2}}$	A LOW on this input, when RT/$\overline{\text{BC}}$ is LOW, causes pin 73 $\overline{\text{DATA SEL 2}}$ output to go LOW.
71	$\overline{\text{BC LOAD DATA 2}}$	A LOW on this input, when RT/$\overline{\text{BC}}$ is LOW, causes pin 72 LOAD DATA 2 output to go HIGH.
72	LOAD DATA 2	A positive pulse on this output causes the Least Significant Byte to be transferred to the encoder register.
73	$\overline{\text{DATA SEL 2}}$	A negative pulse on this output causes the decoder register to output the Least Significant Byte onto the parallel tri-state I/O (D0 through D7).
74	$\overline{\text{MSB}}$/LSB	A LOW on this output indicates that the Most Significant Byte is being transferred on the paralled tri-state I/O.
75 thru 82	D7 thru D0	MSB through LSB of parallel tri-state data highway.

ORDERING INFORMATION

BUS-66108-883

MIL-STD-883 Processing:
883= Conforms to MIL-STD-883 DDC Procedures
Blank= Same, except burn-in is omitted

MIL-STD-1553 DATA BUS EXERCISER



DESCRIPTION

The BUS-68003 is a low cost portable instrument for testing and troubleshooting MIL-STD-1553 systems. It is designed to complement much more expensive top-of-the-line testers. Its price/performance makes it a leader for test applications requiring Bus Controller (BC) or Remote Terminal Unit (RTU) simulation.

BUS-68003 offers simple and flexible operation including either local programming via a front panel 24 pad keyboard and 10 character alphanumeric display, or remote programming via an 8 bit parallel I/O port or IEEE-488 and RS-232 interfaces. Additional features include error generation and error detection, single or repeat messages, variable response time, variable message gap, variable transmitter amplitude, and built-in self test. All MIL-STD-1553 message formats can be simulated by the BUS-68003.

FEATURES

- *LOW COST:*
  COMPLEMENTS TOP-OF-THE-LINE TESTERS
- *FLEXIBLE OPERATION:*
  BUS CONTROLLER
  REMOTE TERMINAL
- *PROGRAMMABILITY:*
  24 PAD KEYBOARD
  8 BIT PARALLEL I/O
  IEEE-488 I/O
  RS-232 I/O
- *ERROR GENERATION*
- *ERROR DETECTION*
- *VARIABLE TRANSMITTER AMPLITUDE*
- *10 CHARACTER ALPHANUMERIC DISPLAY*

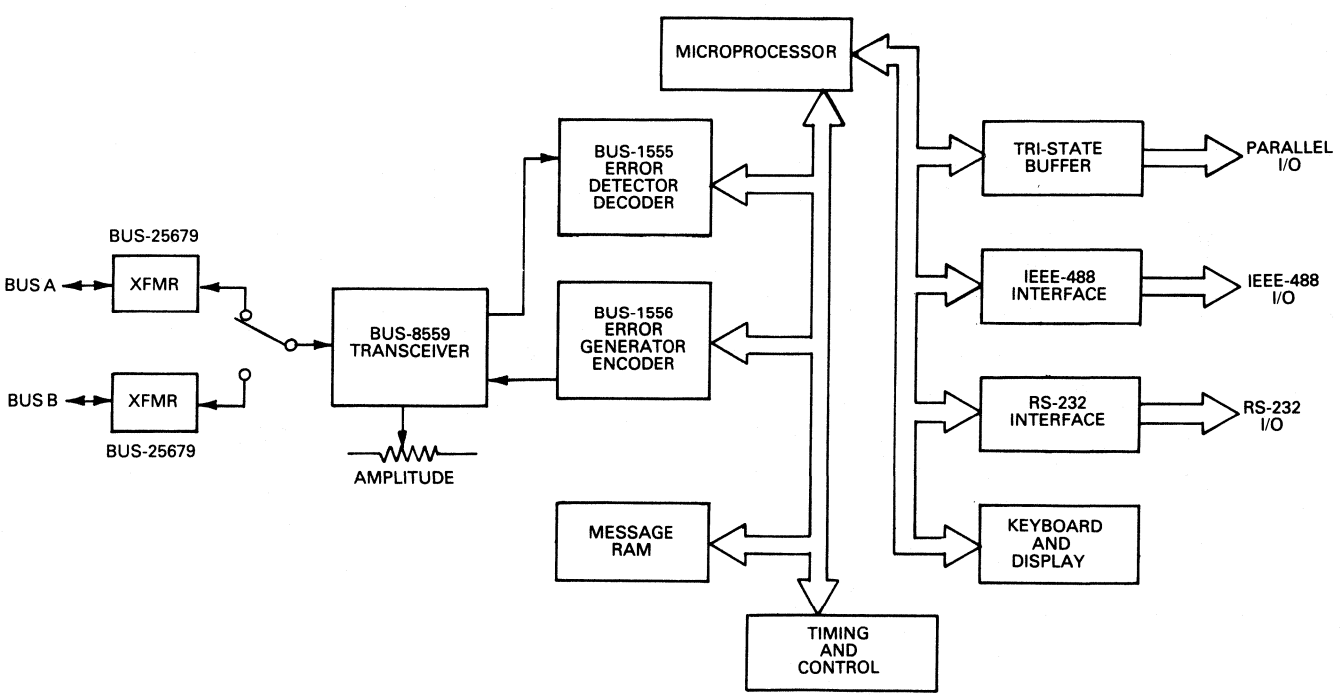


FIGURE 1. BUS-68003 BLOCK DIAGRAM

CHARACTERISTICS

PARAMETER	VALUE
DATA BUS INTERFACE	
Channels	2 (switch selectable)
Coupling	Direct (front panel) or stub (rear panel)
Transmitter	
Output Voltage	Adjustable: 0 to 6.5V_{p-p} (direct coupled across 35 ohms)
Rise/Fall Time	130 nsec typ
Output Noise	10mV_{p-p} max (differential)
Receiver	
Input Voltage	40V_{p-p} max (differential)
Input Impedance	4KΩ min (differential)
Threshold Level	1V_{p-p} typ (direct coupled)
CMRR	40dB min
BUS CONTROLLER MODE[1]	
Message Formats	RT to BC, BC to RT, RT to RT (with Mode Code and Broadcast)
Message Repetition	Single or Repeat
Messages Per Frame	Programmable 1 to 8
Words Per Message	Programmable 1 to 49
Intermessage Gap	Programmable 10 to 255 μsec
Frame Time	Programmable 2 to 500 msec
REMOTE TERMINAL MODE	
Message Formats	RT to BC, BC to RT, RT to RT (with Mode Code and Broadcast)
Message Repetition	Single or Repeat
Simulated RTUs	Programmable 1 to 8
Response Time	Programmable 8 to 32 μsec
Address	Programmable 0 to 31
ERRORS GENERATED	
Manchester Error	Any bit position
Parity Error	Any word
High or Low Bit Count	Any word
Sync Type Error	Command or Data Word
Sync Field Error	Incorrect mid-bit crossing
High or Low Word Count	Any message
Response Time Error	Any message
Format Error	Incorrect T/R bit any message
ERRORS DETECTED	
Manchester Error	
Parity Error	
Bit Count Error	
Word Count Error	
Sync Type Error	
Response Timeout	16 μsec
Transmitter Timeout	800 μsec
REMOTE INTERFACES	
8 Bit Parallel (3-State)	Standard on BUS-68003
IEEE-488	
RS-232	
AC POWER INPUT	
Voltage	115V/230V ± 10% (switch selectable)
Power	60 VA max
Frequency	47-63 Hz
OPERATING TEMPERATURE RANGE	0°C to +70°C
MECHANICAL OUTLINE	17" x 14.5" x 3.5" (43 x 37 x 9.0 cm)
WEIGHT	18 lbs (8.2 kg)

Notes:
(1) In BC Mode, unit can simulate BC and one RT, for an RT to RT transfer.

GENERAL

As a Bus Controller, the BUS-68003 controls the command/response data transfer with one or more RTUs. Messages are loaded either manually or remotely and can be programmed to contain errors such as Manchester coding, parity, sync, and high or low bit count or word count. Up to 8 messages of 49 words each may be loaded at one time. Inter-message gap can be selected from 10 to 256 microseconds, in 1 microsecond steps. The BUS-68003 evaluates the response to each command, and flags and displays errors such as response time, contiguity, fail-safe timeout, Manchester coding, sync, parity, and high or low bit count or word count.

In the Bus Controller mode, the BUS-68003 implements BC to RT, RT to BC, and RT to RT message transfer formats. Each format may include broadcast or mode code commands. Furthermore, the Exerciser can be configured to simulate both the BC and one of the RTUs in an RT to RT transfer. Commands and responses are stored in the BUS-68003 internal RAM, and may be viewed word by word by means of the 10 character front panel alphanumeric displays or the remote I/O port.

As a Remote Terminal Unit, the BUS-68003 receives, validates and stores data bus commands containing its (selectable) address. Up to 8 RTU's can be simulated at one time. It responds to commands with status and data, as appropriate. Response time can be programmed from 8 to 32 microseconds, in 1 microsecond steps. Up to eight messages of 49 words each may be stored at one time in the BUS-68003 internal RAM. These messages may be accessed via the keyboard for viewing on the front panel alphanumeric display.

In the Remote Terminal Unit mode, the BUS-68003 evaluates each command, and flags and displays errors such as format, response timeout, fail-safe timeout, Manchester coding, parity, sync, and high or low bit count or word count.

The BUS-68003 is packaged in a 3.5" x 14.5" x 17" enclosure with a handle that can be used as a tilt-stand. It operates from 115 VAC or 230 VAC 47-63 Hz power. With its flexible manual or remote programmability and its error generation and detection, the BUS-68003 is ideal for simulation of Bus Controllers or Remote Terminal Units for bench, field or factory test applications.

SET-UP PROCEDURE

In order to insure correct operation of the BUS-68000, the following step-by-step set-up procedure is recommended:

(1) Set the Power Input Switch on the rear panel to the correct line voltage (115 VAC or 230 VAC) and connect the line cord to the BUS-68003.

(2) Connect the MIL-STD-1553 cable to the BUS-68003 Channel A and Channel B connectors. Direct coupled data bus connections are made to the front panel connectors. Stub coupled data bus connections are made to the rear panel connectors. Figure 2 is an interconnection diagram illustrating the BUS-68003 data bus interfaces at the front and rear panel connectors.

(3) Set the Channel Select Switch on the front panel to Channel A or Channel B.

(4) Connect J2 (Parallel I/O), J3 (RS-232) and/or J4 (IEEE-488) remote interface cables to the rear panel connectors. Set I/O select switch S8.

(5) Plug in the line cord and set the Power Switch to ON.

(6) Observe the front panel display indications:

DISPLAY	LED	INTERVAL
RANDOM	RANDOM	1 second
BLANK	OFF	1 second
88 88 8888 88	ON	1 second
PASS	OFF	1 second
IT 01 0840 00	DEFAULT	FIXED

The BUS-68003 performs a complete internal self-test upon power turn-on. First the front panel display and LEDs are checked, then a wraparound test is performed which checks 1553 encoder, decoder, PROM and RAM.

After the PASS indication appears, the display and LEDs show the power on default condition of the BUS-68003. The LEDs show Local operation in the Bus Controller mode, with a Single message block. The display shows Block 1, with Transmit Direction, Word 1, default Command Word, and no errors injected. The default Command Word (0840) is a receive command for 32 words to RTU address #1 and subaddress #2.

In the event that the power on self-test yields a failure, the display will be fixed with a FAIL indication and a 2 digit error code. The meaning of the error code is as follows:

ERROR CODE	FAILURE
10	Encoder/decoder wraparound test
08	RT trigger RAM test
04	Message RAM test
03	Checksum test-3 PROMS
02	Checksum test-2 PROMS
01	Checksum test-1 PROM

Troubleshooting procedures are detailed in the BUS-68003 Instruction Manual. If it is desired to isolate the source of the self-test failure, or to program the BUS-68003 after a self-test failure has occurred, the CLR key must be depressed to reset the instrument.

(7) Set the desired data bus line voltage by monitoring the SYNC waveform while varying the AMPL ADJ control on the front panel. This will first require pressing the CNTL SNRP key to yield REPEAT operation and then pressing the RUN button.

MANUAL PROGRAMMING

Manual programming of the BUS-68003 Exerciser is a straightforward operation that is illustrated in the Figure 4 Flow Diagram. A functional description of each of the programming keys is contained in Figure 3. Figure 5 is a chart of message formats and their corresponding 2 digit entries, which are used as part of the CNTL FRMT key entry sequence of programming. Figure 6 is a chart of transmitted errors and their corresponding 2 digit entries, which are used as part of the PROG key entry sequence. Figure 7 is a chart of error position codes, which are used as part of the CNTL ER BP key entry sequence of programming. Figure 8 is a chart of error codes, which are displayed on the front panel as part of the READ key sequence when checking the BUS-68003 internal memory. Figure 9 is a timing diagram showing a typical message block and frame repetition.

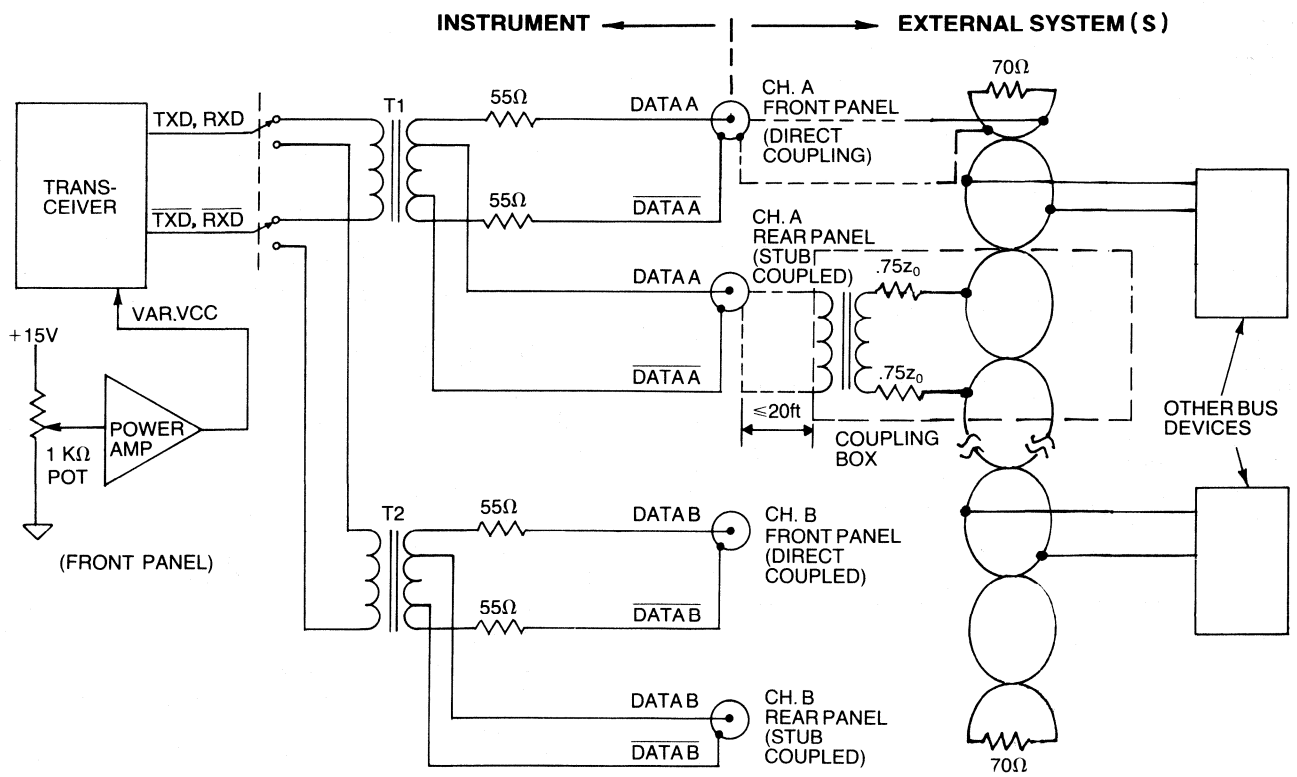
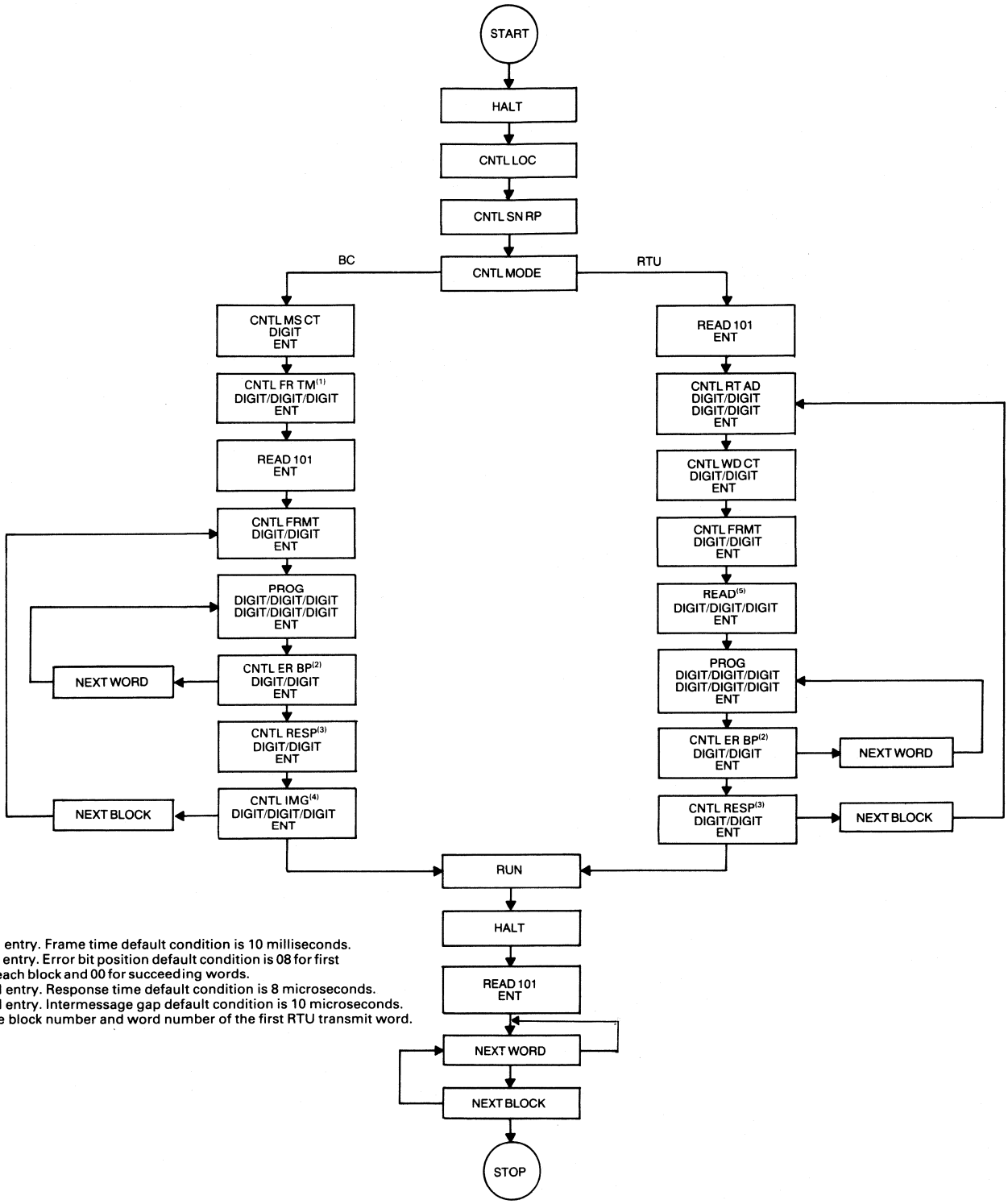


FIGURE 2. DATA BUS INTERCONNECT DIAGRAM

FIGURE 3. KEYBOARD AND DISPLAY FUNCTIONS

KEY SEQUENCE	FUNCTION	DISPLAY/INDICATION
CNTL LOC	Selects Local mode of exerciser control.	LOCAL indicator light illuminates.
CNTL MODE	Selects Bus Controller or Remote Terminal mode of operation with alternating activation of the MODE key.	BC or RT indicator light illuminates in coincidence with the MODE key's state.
CNTL SN RP	Selects single or repeat mode of operation with alternating activation of the SN RP key.	SINGLE or REPEAT indicator lights illuminate in coincidence with the SN RP key's state.
CNTL FRMT *DIGIT* *DIGIT* ENT	Information transfer format for a given block is selected with 2 (HEX) digits. See Figure 5.	The 4 digit (HEX) display will indicate the one or two-digit format.
CNTL RTAD D or E 0 or 1 *DIGIT* *DIGIT* ENT	Used only in the RTU mode. The RT address for a given message block is programmed. The first digit Enables (E) or Disables (D) the block. The second digit specifies whether to trigger on a Transmit (1) or Receive (0) Command Word. The third and fourth digits specify the 2-digit (decimal) RT address (00 to 31).	The 4-digit (HEX) data section of the 16 Bit Data field will show the entered RT address information.
CNTL RESP *DIGIT* *DIGIT* ENT	Simulated RT response time is entered as 2-digits (decimal). The allowable range for response time is from 8 to 32 microseconds.	The 4-digit(HEX) data section of the 16 Bit Data field will indicate the 1 or 2-digit response time in microseconds.
CNTL IMG *DIGIT* *DIGIT* *DIGIT* ENT	Used only in BC mode. The Intermessage Gap time preceding a given message block is entered as 3 (decimal) digits. Allowable range is from 10 to 255 microseconds (see Figure 9, Block/Frame Timing Diagram).	The 4 digit (HEX) data section of the 16 Bit Data field will indicate the 2 or 3 (decimal) digit Intermessage Gap Time in microseconds.
CNTL WD CT *DIGIT* *DIGIT* ENT	The data word count for a given message block is entered as 2 (decimal) digits. For RT mode, this parameter must be programmed. For BC mode, word count defaults to the correct value if unspecified. Allowable range for Word Count is from 0 to 45 words.	The 4 digit (HEX) data section of the 16 Bit Data field will indicate the 1 or 2-digit data word count.
CNTL ER BP *DIGIT* *DIGIT* ENT	The Sync and/or Manchester Error position for the current word is entered as 2 (HEX) digits. See Figure 7.	The Block and Word number are displayed in their normal positions. The 1 or 2-digit (HEX) error position code will appear in the 4-digit (HEX) data section of the 16 Bit Data field.
CNTL FR TM *DIGIT* *DIGIT* *DIGIT* ENT	Used in BC mode only. The Frame Time or overall repetition time for a series of messages to be executed is entered as 3 (decimal) digits. The allowable range for Frame Time is 2 to 500 milliseconds. (see Block/Frame Timing Diagram).	The 4 digit (HEX) data section of the 16 Bit Data field will display the entered data.
CNTL PRNT	A user friendly message, conveying all information about the current message block is outputted via the instrument's RS-232 port. It may be displayed on a CRT or a hard copy may be printed if configured with the I/O port.	No change from previous indication.
CNTL MS CT *DIGIT* ENT	Used in BC mode only. The number of messages (blocks) to be executed is specified. The allowable Message Count is 1 to 8.	The 4-digit (HEX) data section of the 16 Bit Data field will display the entered Message Count information.
CLR	Clear function (terminates data or parameter entry). Also used to enable instrument operation in the event of Self Test failure at power turn-on.	The display reverts back to its last Command Word.
NEXT WORD	The current Word Number field (within the current block) is incremented by one. If the current word is the last word in the block, the next word becomes the first word of the current block. NEXT WORD is also used in conjunction with the PROG key.	The next (or first) word in the message block is displayed in the Block, DIR, Word Number, 16 Bit Data and Error Code fields.
NEXT BLOCK	The Block field is incremented to the next highest block or to block 1 if the current block number is 8. The Word Number field then displays the first word of the new current block.	The first word of the new current block is displayed in the Block, DIR, Word Number, 16 Bit Data and Error Code fields.
PROG *DIGIT* • • *DIGIT* NEXT WORD *DIGIT* • • *DIGIT* ENT	The data contents and error codes of the current word, or successive words within a message block are programmed. Multiple words are separated by a NEXT WORD key entry. ENT terminates entry of the string of words. If the entry code for a given string is four (HEX) digits or less, the string represents right justified data only, with the Error Code field defaulting to 00. If programmed, the fifth and sixth (HEX) digits represent the right justified Error Code field for the word.	The block number, DIR, Word Number, 16 Bit Data and Error Code fields for each word will be displayed as entered.
READ *DIGIT* *DIGIT* *DIGIT* ENT	The READ command reviews a specific block and word. The block number is specified by the first digit entered. The word number within the block is specified by the second digit (right justified) or second and third digits entered.	The appropriate word is displayed from the selected Block Number, including DIR bit, Word Number, 16 Bit Data and Error Code. The DIR field is decoded as follows: T=Transmit Word R=Received Word P=Word Pending Reception
CNTL SELF TEST	Causes the instrument to perform its internal self-test. This test exercises PROM, Message and RT Trigger RAMS and a wraparound test of MIL-STD-1553 encoder/decoder circuitry. Following self test the instrument re-initializes to its power turn-on state Bus Controller mode, Local, Single Frame and Single Block.	In sequence: (1) All LED's blank (1 second) (2) All LED's illuminate (1 second) (3) PASS or FAIL is displayed in the 4-digit (HEX) data section of the 16 Bit Data field. If FAIL is displayed a 2-digit Fail Code is displayed in the Error Code field.



NOTES:
(1) Optional entry. Frame time default condition is 10 milliseconds.
(2) Optional entry. Error bit position default condition is 08 for first word of each block and 00 for succeeding words.
(3) Optional entry. Response time default condition is 8 microseconds.
(4) Optional entry. Intermessage gap default condition is 10 microseconds.
(5) Enter the block number and word number of the first RTU transmit word.

FIGURE 4. MANUAL PROGRAMMING FLOW DIAGRAM

FORMAT ENTRY	MODE	FORMAT	SIMULATION
00[1]	BC RTU	RT to BC or BC to RT RT to BC or BC to RT	BC RTU
01[2]	BC RTU	RT to RT RT to RT	BC RTU(TX)
02[2]	BC RTU	RT to RT RT to RT	BC and RTU(TX) RTU(TX) and RTU(RX)
03[2]	BC RTU	RT to RT RT to RT	BC and RTU(RX) RTU(RX)
04	BC RTU	MODE CODE MODE CODE	BC RTU
08	BC RTU	BROADCAST BROADCAST	BC RTU(RX)
09	BC RTU	BROADCAST and RT to RT BROADCAST and RT to RT	BC RTU(TX)
0A	BC RTU	BROADCAST and RT to RT BROADCAST and RT to RT	BC and RTU(TX) RTU(TX) and RTU(RX)
0B	BC RTU	BROADCAST and RT to RT BROADCAST and RT to RT	BC and RTU(RX) RTU(RX)
0C	BC RTU	BROADCAST and MODE CODE BROADCAST and MODE CODE	BC RTU(RX)
10[3]	BC RTU	T/R FORMAT REVERSAL ERROR T/R FORMAT REVERSAL ERROR	BC RTU
20[4]	BC	SELF TEST	NONE

Notes

(1) In the BC mode, the T/R bit of the Command Word determines whether the **BUS-68003** transmits or receives data. In the RTU mode the T/R bit of the programmed 4 (decimal) digit CNTL/RT AD word determines whether the **BUS-68003** transmits or receives data.

(2) In an RT to RT message format, when the **BUS-68003** is in the RTU mode, the T/R bit of the programmed 4 (decimal) digit CNTL/RT AD word must be set to logic "0" (Receive).

(3) In the BC mode, the **BUS-68003** trans mits the Command Word and then acts as if the opposite T/R bit condition were true. In the RTU mode, the **BUS-68003** receives the Command Word and then acts as if the opposite T/R bit condition were true.

(4) In the BC mode only, a wraparound self-test will be implemented on message block #1. The transmitter is inhibited and the encoder drives the decoder directly. The last data word received is stored in **BUS-68003** memory.

FIGURE 5.
MESSAGE FORMAT (CNTL/FRMT) KEY ENTRIES

KEY SEQUENCE	TRANSMITTED ERROR
01	Long Word
02	Short Word
04	Data Manchester Error
08	Parity Error
10	Sync Error
20	Parity Manchester Error
40	Sync Type Error

FIGURE 6. TRANSMITTED ERROR KEY ENTRIES

KEY SEQUENCE	ERROR POSITION
00 Thru 0F	Data Position 1 Thru Data Position 16
10	Alternate Sync Error Position

FIGURE 7. ERROR POSITION KEY ENTRIES

DISPLAY ERROR CODE	ERROR
01	Long Word
02	Short Word
04	Manchester Error
08	Parity Error
10	Message Error
20	Response Time Out
40	Incorrect Sync Type

FIGURE 8. DISPLAYED ERROR CODES

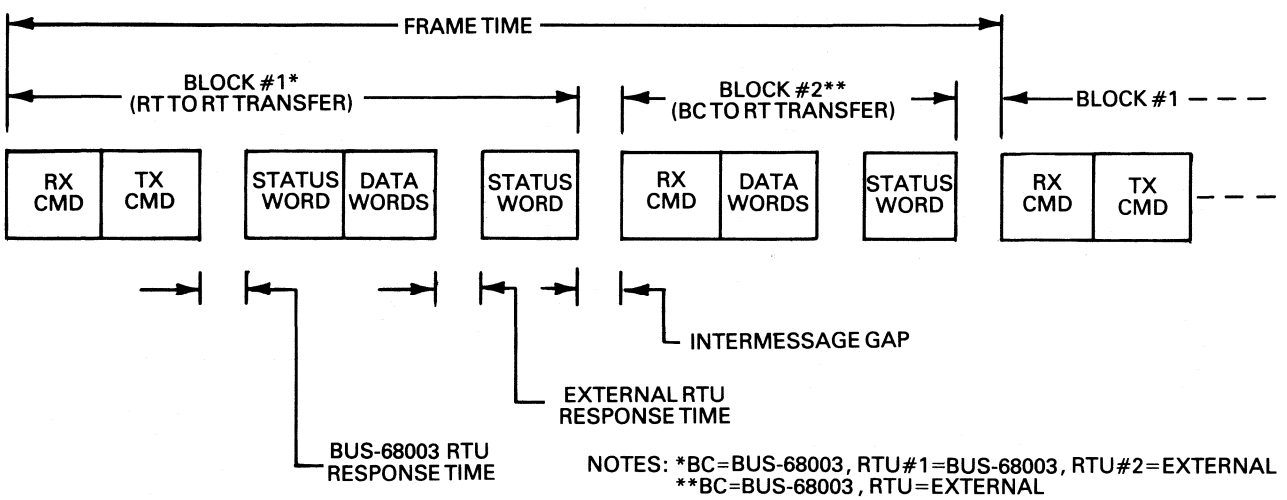


FIGURE 9. BLOCK AND FRAME TIMING DIAGRAM (BC MODE)

FRONT PANEL INDICATOR FUNCTIONS	
INDICATOR	**FUNCTION**
LOCAL	Indicates that the Local mode of Exerciser control has been selected.
REMOTE	Indicates that the Remote mode of Exerciser control has been selected.
BC	Indicates that the Bus Controller mode of Exerciser operation has been selected.
RT	Indicates that the Remote Terminal mode of Exerciser operation has been selected.
SINGLE	Indicates that the Single mode of Exerciser operation has been selected.
REPEAT	Indicates that the Repeat mode of Exerciser operation has been selected.
ON-LINE	Indicates that the Exerciser is ready to receive (RT mode) or is transmitting in the Repeat mode (BC mode).
LINE ACTIVE	Indicates that there is activity on the selected 1553 data bus.
BUS FAULT	Indicates an error in the word or message received from the 1553 data bus.
REPLY T/OUT	Indicates that a 16μs response timeout fault (BC mode) has occurred.
XMTR T/OUT	Indicates that a 800μs terminal fail-safe timeout fault has occurred.

J3 PIN FUNCTIONS (RS-232 I/O)		
PIN	**FUNCTION**	**DESCRIPTION**
1	PROT GND	Chassis ground.
2	TXD	Transmit Data output.
3	RXD	Receive Data input.
4	RTS	Request to Send output.
5	CTS	Clear to Send input.
6	NC	No connection.
7	SIG GND	Signal ground.
8	DCD	Data Carrier Detect input.
9 THRU 25	NC	No connection.

J2 PIN FUNCTIONS (PARALLEL I/O)		
PIN	**FUNCTION**	**DESCRIPTION**
1	T7	MSB of 8 bit parallel tri-state I/O bus.
2	T6	Part of 8 bit parallel tri-state I/O bus.
3	T5	Part of 8 bit parallel tri-state I/O bus.
4	T4	Part of 8 bit parallel tri-state I/O bus.
5	T3	Part of 8 bit parallel tri-state I/O bus.
6	T2	Part of 8 bit parallel tri-state I/O bus.
7	T1	Part of 8 bit parallel tri-state I/O bus.
8	T0	LSB of 8 bit parallel tri-state I/O bus.
9	$\overline{\text{READ}}$	A LOW on this input causes a read data sequence.
10	$\overline{\text{WRITE}}$	A LOW on this input causes a write data sequence.
11	$\overline{\text{T ACK}}$	A LOW on this output indicates composite transfer acknowledge.
12	$\overline{\text{SERV REQ}}$	A LOW on this output indicates a service request.
13	GND	Digital ground.
14	$\overline{\text{R ACK}}$	A LOW on this output indicates data output transfer acknowledge.
15	$\overline{\text{W ACK}}$	A LOW on this output indicates data input transfer acknowledge.
16	CHASS GND	Chassis ground.
17 THRU 25	NC	No connection.

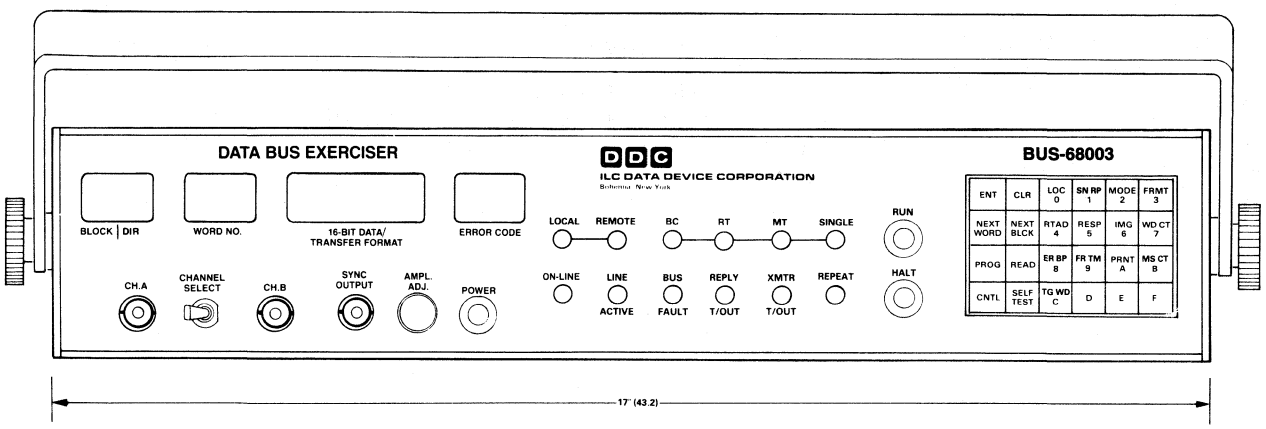
J4 PIN FUNCTIONS (IEEE-488 I/O)		
PIN	**FUNCTION**	**DESCRIPTION**
1	D101	LSB of 8 bit tri-state GPIB bus.
2	D102	Part of 8 bit tri-state GPIB bus.
3	D103	Part of 8 bit tri-state GPIB bus.
4	D104	Part of 8 bit tri-state GPIB bus.
5	$\overline{\text{EOI}}$	End or Identify input/output.
6	$\overline{\text{DAV}}$	Data Available input/output.
7	RFD	Ready for Data input/output.
8	DAC	Data Accepted input/output.
9	$\overline{\text{IFC}}$	Interface Clear input.
10	$\overline{\text{SRQ}}$	Service Request output.
11	$\overline{\text{ATN}}$	Attention input.
12	CHAS GND	Chassis ground.
13	D105	Part of 8 bit tri-state GPIB bus.
14	D106	Part of 8 bit tri-state GPIB bus.
15	D107	Part of 8 bit tri-state GPIB bus.
16	D108	MSB of 8 bit tri-state GPIB bus.
17	$\overline{\text{REN}}$	Remote Enable input.
18 THRU 24	GND	Digital ground.

MANUAL SWITCH/CONTROL FUNCTIONS		
SWITCH	**FUNCTION**	**REMARKS**
RUN	Starts the 1553 data bus message transfer cycle.	The ON-LINE indicator lights up and the display reads BUSY.
HALT	Stops the 1553 data bus message transfer cycle.	The ON-LINE indicator shuts off and the display reads HALT.
CHANNEL SELECT	Selects 1553 data bus A or data bus B	Front panel or rear panel data bus connections.
I/O SELECT	Selects I/O interface of either parallel or IEEE-488 or RS232.	Rear panel switch.
GPIB ADDRESS	Selects the Exerciser's GPIB (IEEE-488) address.	Address has 5 bits. Rear panel switch.
AMPL ADJ	Adjusts the amplitude of the 1553 transmitter output.	Amplitude range is 0 to 6.5 volts peak-to-peak (across 35 ohms).
POWER	Turns on the internal power supply.	An initialization and self-test sequence is performed immediately after power turn-on.
VOLTAGE SELECT	Selects 115 V or 230 V AC line voltage.	Rear panel switch.

MECHANICAL OUTLINE

DIMENSIONS IN INCHES (CENTIMETERS)
17 x 14.5 x 3.5 (43.2 x 37 x 9.0)

FRONT PANEL



REAR PANEL

ORDERING INFORMATION

BUS-68003
└ INTERFACE OPTIONS
- 0 – Discontinued. Replaced with Bus-68003.
- 1 – Discontinued. Replaced with Bus-68003.
- 2 – Discontinued. Replaced with Bus-68003.
- 3 – Standard unit with parallel, IEEE-488, and RS-232 interfaces.

1553 Mating Connector-Trompeter PL 75-47

MIL-STD-1553 DATA BUS TESTER

DESCRIPTION

The BUS-68010 is a low cost bench top portable instrument for testing and troubleshooting MIL-STD-1553 systems. Its price/performance makes it a leader for Bus Controller, Remote Terminal or Bus Monitor simulation applications.

Its simple and flexible operation is controlled via a 24 pad keyboard, with the aid of a 16 character alphanumeric display. Packaged in a 3.5 x 8.5 x 9.3 inch enclosure, it features error generation and error detection, single or repeat messages, and variable inter-message gap time. BC to RT, RT to BC, RT to RT message formats are simulated by the BUS-68010.

The Data Bus Tester's versatility and small physical size make it an ideal choice for laboratory and field testing applications.

FEATURES

- *LOW COST*
- *SMALL SIZE: 3.5" x 8.5" x 9.3"*
- *FLEXIBLE OPERATION:*
  BUS CONTROLLER
  REMOTE TERMINAL
  BUS MONITOR
- *PROGRAMMABLE:*
  24 PAD KEYBOARD
- *ERROR GENERATION*
- *ERROR DETECTION*
- *16 CHARACTER*
  ALPHANUMERIC DISPLAY

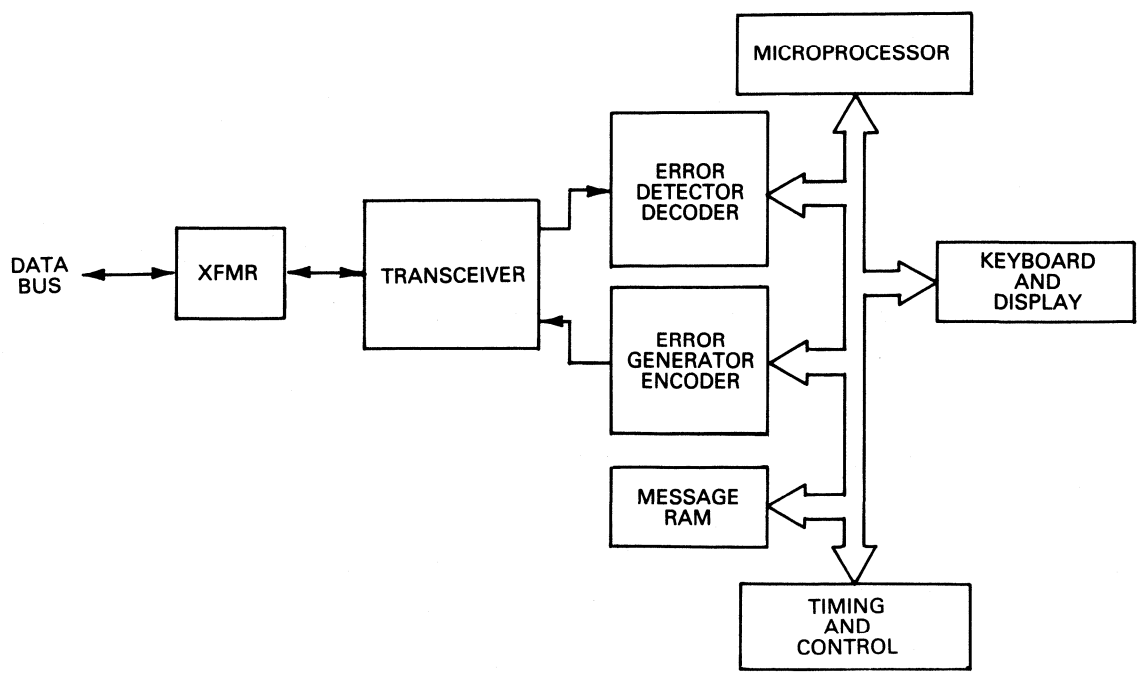


FIGURE 1. BUS-68010 BLOCK DIAGRAM

SPECIFICATIONS	
PARAMETER	**VALUE**
DATA BUS INTERFACE	
Coupling	Direct or stub
Transmitter	
Output Voltage(1)	$6V_{p-p}$ min; $9V_{p-p}$ max
Rise/Fall Time	130 nsec typ
Output Noise	$10mV_{p-p}$ max (differential)
Receiver	
Input Voltage	$40V_{p-p}$ max (differential)
Input Impedance	4KΩ min (differential)
Threshold Level	$1V_{p-p}$ typ (direct coupled)
CMRR	40dB min
MESSAGE CHARACTERISTICS	
Formats	RT to BC, BC to RT, RT (ext) to RT (ext), RT (int) to RT (ext)
Repetition	Single, Double or Continuous
Words Per Message	Programmable 1 to 40
Intermessage Gap	Programmable 5 to 1000 msec
RTU Response Time	7.5 μsec
Address (Trigger)	Programmable 0 to 31
Sync Output	Drives 10 LS TTL loads
ERRORS DETECTED	
Word Errors	
Incorrect Sync	
Invalid Word	Manchester Error, Parity Error, Word Length and Sync Errors
Message Errors	
Word Count	
T/R Bit Mismatch	
ERRORS GENERATED	
Word Errors	
Incorrect Sync	
Parity Error	
Short Word	
Long Word	
Message Errors	
Word Count	
AC POWER INPUT	
BUS-68010	115VAC±10%, 60-440 Hz
BUS-68011	230VAC±5%, 47-440 Hz
OPERATING TEMPERATURE RANGE	0°C to +70°C
DIMENSIONS	9.3" x 8.5" x 3.5" (23.6 x 21.6 x 8.9) cm
WEIGHT	5 lbs (2.27 kg)

Notes:
(1) Output voltage direct coupled across 35 ohm load.

GENERAL

As a Bus Controller, the BUS-68010 controls the command/response data transfer with one or more RTUs. Messages are loaded manually and can be programmed to contain errors such as parity, sync, and high or low bit count or word count. Intermessage gap can be selected from 5 to 1000 milliseconds, in 8 steps. The BUS-68010 evaluates the response to each command, and detects errors such as contiguity, fail-safe timeout, Manchester coding, sync, parity, and high or low bit count or word count.

In the Bus Controller mode, the BUS-68010 implements BC to RT, RT to BC, and RT to RT message transfer formats. Each format may include broadcast or mode code commands. Furthermore, it can be configured to simulate both the BC and one of the RTUs in an RT to RT transfer. Commands and responses are stored in the BUS-68010 internal RAM, and may be viewed word by word by means of the 16 character front panel alphanumeric displays.

As a Remote Terminal Unit, the BUS-68010 receives, validates and stores data bus commands containing its (selectable) address. It responds to commands with status and data, as appropriate. Response time is 7.5μsec. These messages may be accessed via the keyboard for viewing on the front panel alphanumeric display.

In the Remote Terminal Unit mode, the BUS-68010 evaluates each command, and detects errors such as format, Manchester coding, parity, sync, and high or low bit count or word count.

In the Monitor mode, the BUS-68010 receives, validates and stores data bus messages containing its programmed address (trigger). In accordance with MIL-STD-1553, it does not respond with a status word, nor does it transmit data. If programmed for single message, it will stop after one message and display any errors that have been detected. If continuous message has been selected, the BUS-68010 can be programmed to halt on error.

The BUS-68010 is packaged in a 3.5" x 8.5" x 9.3" enclosure with a handle that can be used as a tilt-stand. It operates from 115 VAC, 60-440Hz. The optional BUS-68011 operates from 230 VAC, 47-440Hz. With its flexible manual programmability and its error generation and detection, the BUS-68010 is ideal for simulation of Bus Controllers or Remote Terminal Units for bench, field or factory test applications.

SETUP PROCEDURE

In order to insure correct operation of the BUS-68010, the following step-by-step setup procedure is recommended:

Note

The BUS-68010 and BUS-68011 are identical instruments except for their power supply requirements. Check the upper left hand corner of the front panel for the part number.

(1) Connect the BUS-68010 power plug to a 115 VAC line, or the BUS-68011 power plug to a 230 VAC line.

(2) Connect the MIL-STD-1553 cable to either the direct coupled or stub coupled connector on the rear panel.

Note

The user also has access to a programmable scope trigger through a BNC connector labelled "SYNC OUTPUT" on the rear panel. The SYNC OUTPUT signal is TTL compatible and can be programmed to appear coincident with BUS-68010 transmissions onto the data bus. Since this output is synchronized with the instrument's output signals, it may be used to observe and analyze the data bus activity.

(3) Actuate the push-button power switch on the rear panel. The instrument will then spend the next 15 seconds identifying itself to the user, displaying the following information:

DDC BUS-68010/11
1553 BUS TESTER
ILC/DDC PRODUCT
SELF TEST PASSED
READY

By displaying "READY", the unit has indicated successful completion of an internal self check and the user may begin the desired functional setup. If the device encounters a problem during the self test, it will display "FAILURE" followed by a single digit message. The meaning of the message is as follows:

MESSAGE	FAILURE
FAILURE - 1	ROM Test
FAILURE - 2	1553 Test
FAILURE - 3	Multiple Tests
FAILURE - 4	Display Test

When "READY" is displayed, only the SEL or GO keys can create an action response condition. The instrument is now capable of performing as a Bus Controller, Remote Terminal or Monitor. Forty data words may be entered into the RAM locations where they may be observed or edited with the display cursor and keyboard. During data editing, the up (▲) and down (▼) arrows are used to scroll through the list of words; the left (◀) and right (▶) arrows are used to move through the different digits. Once the instrument is fully programmed following data entry and editing, pressing the GO key begins transmission.

MANUAL PROGRAMMING

After power-on self test, with the display indicating "READY", the instrument's default conditions are as follows:

DEFAULT STATE	RELATED KEYS
BUS CONTROLLER	SEL FCTN
BRO OFF, MC ON	SEL BCMC
EXPANDED FIELD	SEL CMDW
01 T 01R01 00 00	SEL DATA
BC to RT/RT to BC	SEL FRMT
IMG: 5ms	SEL #(t)
MESSAGE CORRECT	SEL WERR
TR 01 X XX XX	SEL TRIG
SINGLE MESSAGE	SEL S/C
ANGLE #3	SEL DSPL

The BUS-68010/11 now may be programmed by the user for any specific function using the front panel keyboard and liquid crystal display. Keys on the panel are grouped within two bracketed areas: FUNCTION and DATA. The FUNCTION keys are used to select a specific menu and, with the GO key, to run the chosen instrument function. The DATA keys permit entry, analysis and modification of data related to the specific function selected.

The keys are tactile-type (pressure sensitive), requiring only a light touch to activate. Note that the SEL key (within the FUNCTION brackets) is blue, matching the color of the non-numeric legends imprinted on 10 of the 16 DATA keys.

The operating sequence requires that the SEL key be pressed first, then one of the blue-legend keys. This process is repeated until the user achieves the desired configuration for the selected function.

Information is presented to the user on a 16-character alphanumeric liquid crystal display. A cursor on the display permits the user to edit data when the DATA or TRIG keys have been selected. The cursor is a horizontal bar appearing below the alphanumeric character to be modified. Its position is controlled by left (◀) and right (▶) arrow keys at the top of the FUNCTION bracket. If the cursor cannot be positioned under a character, it means that no modification to that character is necessary.

The following are the keyboard sequences for entering the four possible types of programmable words:

Command Word: WW D AATSS CC EE
Data Word: WW D S XXXX EE
Status Word: ST AA B FF DD EE
Trigger Word: TR AATSS GG

where:

WW = word number (in decimal)
D = direction of transfer
  T = instrument *will* transmit this word
  P = a word *will* be received in this slot
  R = a word *has* been received in this slot
AA = RT address (In HEX)
T = T/R Bit (R = 0, T = 1)
SS = RT sub address or mode code field (In HEX)
CC = Word count or mode code (In HEX)
EE = Sync output or induced error on transmitted words, detected error on received words
S = Sync type (C = command, D = data
XXXX = Data in four-digit HEX
ST = Status
B = Message error bit (1 = True)
FF = Instrumentation bit, service request bit, plus three reserve bits (in HEX)
DD = Broadcast command bit, busy bit, subsystem flag bit, dynamic bus control bit, and terminal flag bit (in HEX)
TR = Trigger
GG = XX (don't care) if T/R = R. Word count (in HEX) if T/R = T.

A two digit code representing a sync output, an induced error on transmitted words, or a detected error on received words will be displayed at the end of a command word. These programming possibilities are summarized in Table 1.

TABLE 1 ERROR CODES

CODE	ERROR	GENERATED	DETECTED
00	No error	—	—
01	Word sync	Yes	Yes
02	Word 1 bit short	Yes	(Note 1)
04	Word 4 bits long	Yes	(Note 1)
08	Parity	Yes	(Note 1)
10	Invalid word	(Note 2)	Yes
20	Missing word (Note 3)	No	Yes
40	Sync output	Yes	No

Notes: (1) Included in Error Code 10
(2) Error Codes 01,02, 04 and 08 must be specified.
(3) Missing word error is displayed when an RT response timeout (no response) has occurred.

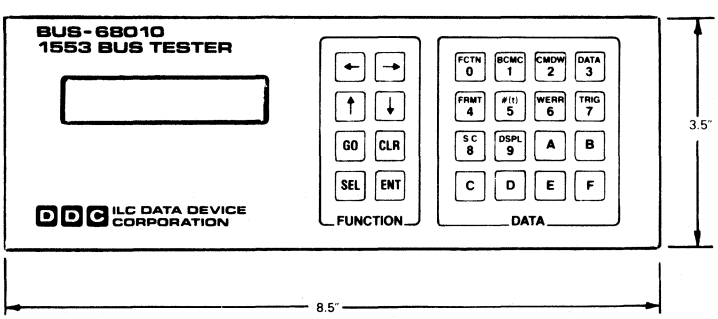
KEYBOARD AND DISPLAY FUNCTIONS		
KEY SEQUENCE	**FUNCTION**	**DISPLAY**
SEL FCTN ◄ or ► ENT	Selects Bus Controller, Remote Terminal or Monitor Mode. The arrows scroll to the next choice.	The current mode will be displayed.
SEL FRMT ◄ or ► ENT	For Bus Controller mode only. Selects Normal, RT (EXT) to RT (EXT), or RT (INT) to RT (EXT) message format.	The current message format will be displayed.
SEL S/C ◄ or ► ENT	Selects single, double or continuous message. The arrows scroll to the next choice.	The current message repetition will be displayed.
SEL TRIG *DIGIT* *DIGIT* ENT	For Remote Terminal mode. The RT address is entered with 2 (HEX) digits. For Monitor mode the trigger address is entered.	The entered address is displayed
SEL DATA ◄ or ► *DIGIT* • • *DIGIT* ENT	Data word and word errors are entered with 6 (hex) digits. Word errors include incorrect sync, parity error, long word and short word. The arrows scroll to the next word in memory. Command words are entered with 4 (HEX) digits or, when in expanded field format, 9 (HEX) digits.	The entered data and word error are displayed.
SEL WERR ◄ or ► ENT	Selects word count error 2 words short, or 1 word short, or correct, or 1 word long, or 2 words long. The arrow scrolls to the next choice.	The current word count error is displayed.
SEL BCMC ◄ or ► ENT	Selects Broadcast/Mode Code options. Either one may be ON or OFF. The arrows scroll to the next choice.	The current broadcast and mode code option is displayed.
SEL #(t) ◄ or ► ENT	Selects the intermessage gap time between 5 msec and 1000 msec. The arrows scroll to the next choice.	The current intermessage gap time is displayed.
GO	Starts operation. For continuous message operation, press CLR key to STOP.	
CLR	Stops operation. Clears last entry.	
SEL CMDW ◄ or ► ENT	Selects Command Word display format of 4-digit (HEX) or expanded field (HEX). The arrows scroll to the next choice.	The current Command Word display format choice is displayed.
SEL DSPL ◄ or ► ENT	Selects LCD viewing angle. Arrows scroll to the next choice.	The optimum display viewing angle varies through 4 choices.

FRONT PANEL CONTROLS/INDICATORS
24 PAD KEYBOARD
16 CHARACTER LCD DISPLAY

REAR PANEL SWITCHES/CONNECTORS
POWER ON/OFF SWITCH
1553 DIRECT COUPLED CONNECTOR
1553 STUB COUPLED CONNECTOR
SYNC OUTPUT

MECHANICAL OUTLINE

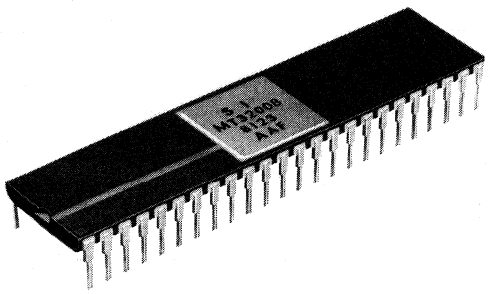
3.5" x 8.5" x 9.3"
(8.9 x 21.6 x 23.6 cm)



ORDERING INFORMATION

BUS-68010
└ Options:
0 = 115 VAC Power
1 = 230 VAC Power

DDC
ILC DATA DEVICE CORPORATION



MIL-STD-1553 ENCODER/DECODER

DESCRIPTION

The MT32008 is a single chip device, which can be used to interface between a transmitter/receiver and a 16 bit parallel highway. It can be used as the interface in either a remote terminal, or in the bus controller, since it is capable of transmitting command words.

The MT32008 encodes a 20 bit serial word in Manchester II when it is told to transmit, or decodes a 20 bit Manchester II encoded serial word when it is in the receive mode. When receiving, it checks each word for valid sync field, proper Manchester coding, its own address and correct parity. A valid word signal is generated if these tests are passed. When transmitting, it encodes the contents of the 16 bit highway and adds a sync field and generates an odd parity bit.

For RTU applications, the MT32008 has a user-selected, 5 bit hard wired address. Another single hardwired pin assigns the encoder/decoder to one of the redundant 1553 buses.

Other I/O functions allow the MT32008 to interface directly to an MT32004 Protocol Sequencer, with no additional logic, while still giving it the flexibility for use with a custom designed protocol/subsystem interface.

FEATURES

- *LOW COST*
- *MONOLITHIC*
- *SMALL SIZE*
- *FOR RT OR BUS CONTROLLER*
- *HARDWIRED ADDRESS*
- *CHECKS FOR:*
  - *VALID SYNC FIELD*
  - *MANCHESTER II CODING*
  - *BIT COUNT*
  - *OWN ADDRESS*
  - *PARITY*

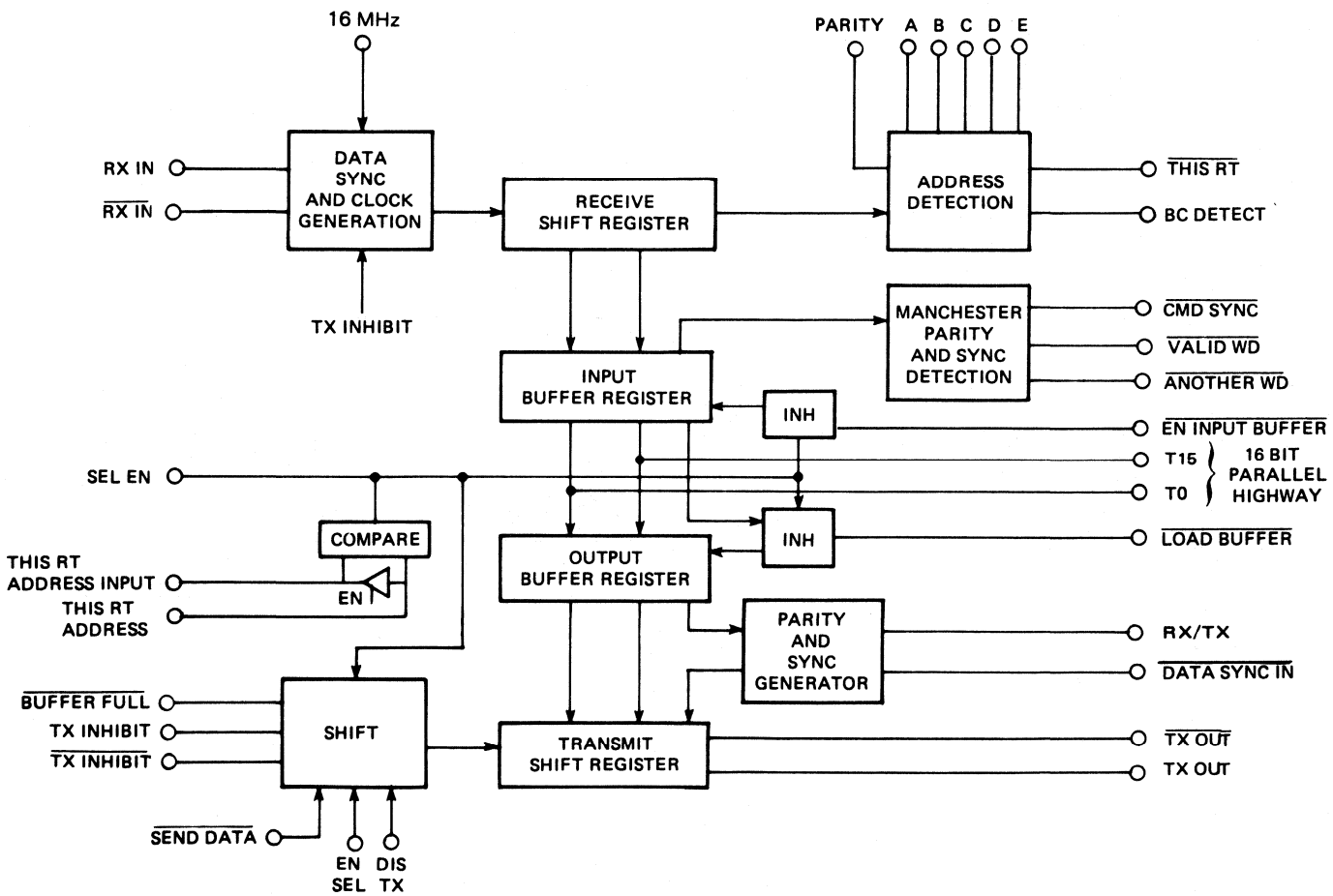


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM

SPECIFICATIONS

OPERATING CONDITIONS

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{DD}	+10 Volts
Supply voltage V_{SS}	0 Volts
Low level input voltage	V_{SS} –0·5 Volts
High level input voltage	V_{DD} +0·5 Volts
Operating free air temperature range	–55°C to +125°C
Storage temperature range	–65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage V_{DD}	4·5	5	5·5	Volts
Current drain*			3	mA
Operating free air temperature	–55		+125	°C

STATIC ELECTRICAL CHARACTERISTICS over free air temperature range (V_{DD} = 5 Volts)

	MIN	NOM	MAX	UNIT
Input type A†				
V_{IH} High level input voltage	2·40		5	Volts
V_{IL} Low level input voltage	V_{SS}		0·80	Volts
C_{IN} Input capacitance			10	pF
Input type B† (on chip resistive pull ups)				
V_{IH} High level input voltage		2·4 or 0/C	5 or O/C	Volts
V_{IL} Low level input voltage		V_{SS}	0·8	Volts
I_{IL} Low level input current			1·6	mA
C_{IN} Input capacitance			10	pF
Input/output type E†				
V_{IH} High level input voltage	2·4		5	Volts
V_{IL} Low level input voltage	V_{SS}		0·8	Volts
V_{OH} High level output voltage	4·5		5	Volts
V_{OL} Low level output voltage			0·4	Volts
I_{OH} High level output current	1.0			mA
I_{OL} Low level output current	–3.2			mA
$C_{IN/OUT}$ I/O capacitance			10	pF

DYNAMIC ELECTRICAL CHARACTERISTICS

Rise time of output V_{SS} to 3 Volts into 20 pF load = 50 ns max..

Fall time of output V_{DD} to 0·4 Volts into 20 pF load = 50 ns max.

Output type C†				
V_{OH} High level output voltage	4·5		5	Volts
V_{OL} Low level output voltage	V_{SS}		0·4	Volts
I_{OH} High level output current	1.0			mA
I_{OL} Low level output current	–3.2			mA
Output type D† (Open drain outputs)				
V_{OL} Low level output voltage			0·4	Volts
I_{OL} Low level output current	–3.2			mA

†See Pin Type Table for signal list of each type.

* With no load.

1.0 GENERAL

DECODER

The Decoder section accepts the biphase TTL signal from the transceiver, decodes and loads it into the receiver shift register, where ADDRESS detection as well as Manchester parity and sync detection are activated. The decoder flags ANOTHER WORD after each and every sync field plus the first three data bits. If the decoder validates the command word, it's own address, and proper parity, then the Command Sync (CMD SYNC), VALID WORD, and THIS RT flags will all go low at the same time. If the address is all "1"s, i.e., a broadcast command, then BDCST DETECT will go low in place of THIS RT. The signals ANOTHER WORD and VALID WORD will repeat their sequence for each data word following the command word. During VALID WORD, the decoded data is shifted into its input buffer register and is available on the 16 bit parallel (T0 thru T15) highway (HWY) for typically 20 microsecond intervals.

ENCODER

The Encoder section takes the 16 bit parallel data, adds the correct sync field and odd parity bit, and then outputs it to the BUS-63115 transceiver as biphase TTL complimentary data. The Encoder must acknowledge that THIS RT ADDR LS (hard wired on pin 20) is the same as THIS RT ADDR IP LS in order to insure that the correct redundant data bus has been selected. The Select Enable (SEL EN) signal goes high when the aforementioned redundant bus addresses are valid. Once SEL EN is valid, data is loaded into the output buffer register by the load buffer command. The SEND DATA signal controls the shift and load control logic. These signals initiate the actual biphase TTL transmission while also generating a BUFFER FULL status flag.

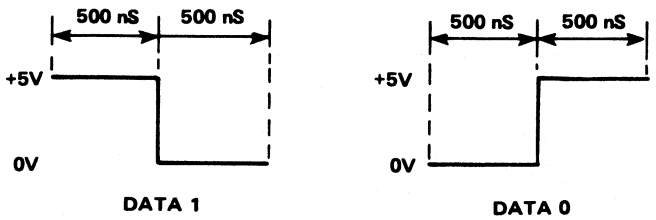
BUS CONTROLLER NOTE

The MT32008 ENCODER/DECODER has provision for being used in a Bus Controller configuration. This is faciliated by two extra control lines provided on the encoder's parity and sync generation circuitry. The type sync field desired can be set externally. The MT32008 automatically sends Command Sync immediately followed by a data sync field. External control is only required for RT to RT transfers where two contiguous command syncs are required.

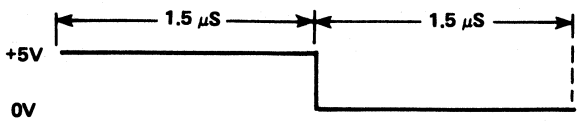
2.0 DETAILED OPERATION

RECEIVE MODE

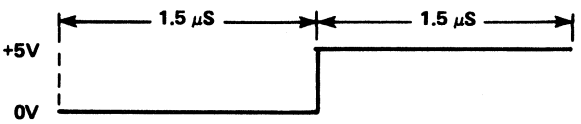
Command words or data words consisting of 20-bit (Manchester code) are serially received at the RXIN and $\overline{\text{RXIN}}$ inputs, ($\overline{\text{RXIN}}$ is the inverse of RXIN) via a transceiver at a bit rate of 1 MHz. The data is synchronized with the 16 MHz free running clock and shifted into a 40-bit shift register (2-bits of shift register for 1 Manchester code bit). The first 3-bits to be received contain either the command or data sync which are invalid Manchester Code.



ONE BIT MANCHESTER CODE

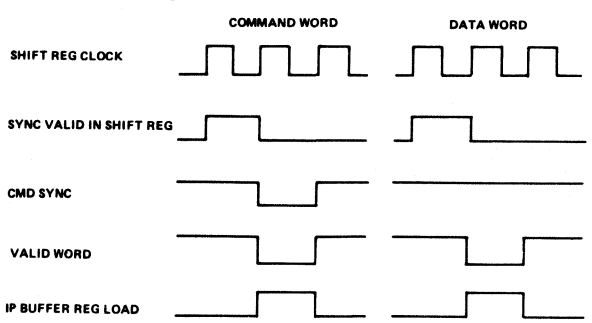


COMMAND SYNC



DATA SYNC

The first 6-bits of the shift register (3 data bits) are being continuously monitored detecting either a command sync or data sync. If a command sync is detected the output CMD SYNC becomes valid for 500 nS. When a command or data sync is detected, the data in the shift register is checked for word count, correct Manchester coding and odd parity. If there are no errors, the 16 data bits in the shift register (bits 4-19) are transferred to the input buffer register and then enabled onto the 16 bit highway via VALID WORD signal for 20 microseconds.



When a command word is received the most significant 5-bits of the data are compared with a hard wired terminal address (term addr E being MSB) and the results sets the output. THIS RT valid during the same period as valid word and CMD SYNC. The 5-bit hard wired terminal address and odd parity must be valid before THIS RT becomes valid.

If at any time there are 5 received bits all a "1" inputted to the terminal address comparator then the output BROADCAST DETECT becomes valid instead of THIS RT.

When a valid command word is received, a 2-bit hard wired address (THIS RT ADDR) is enabled to the I/O pins THIS RT ADDR IP during the same period as CMD SYNC.

The last 12-bits of the shift register are being continuously monitored to give early warning of a new word being received, i.e. a command or data sync plus 3 bits of correct Manchester coding. If this has been detected the output ANOTHER WORD becomes valid for 500 ns.

The 2 I/O pins (THIS RT ADDR IP) are being continuously compared with the hard wired address (THIS RT ADDR), if equal then the output SEL EN becomes valid. With SEL EN valid a signal on the input EN INPUT BUFFER will enable the contents of the input buffer register onto the 16-bit I/O highway T0-T15. (T15 being the most significant). Also with a SEL EN valid the transmit circuitry is enabled.

TRANSMIT MODE

To transmit data from MT32008 the signal SEL EN must be valid. Data present on the 16-bit I/O highway to be transmitted is loaded into the output buffer register with input signal LOAD BUFFER. The status sync or data sync is internally generated and is also loaded into the register to be the first 3-bits of transmission. The status sync waveform is the same as a command sync waveform. From this register a parity bit is generated.

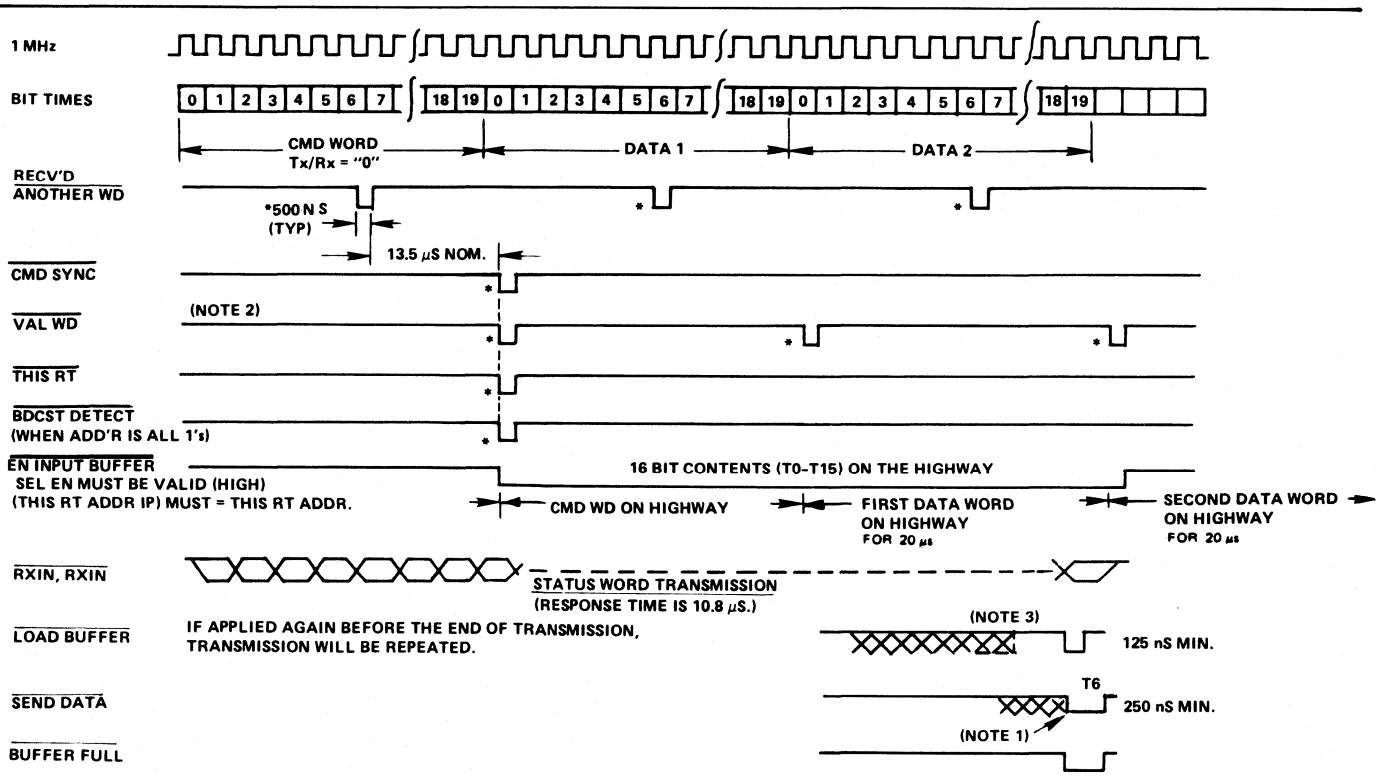
To initialize transmission an active low on SEND DATA is applied. Data will be transferred from the output buffer register, converted to Manchester code, and loaded into the 40-bit shift register and shifted out via TXOUT and TXOUT (TXOUT is the inverse of TXOUT), to the transceiver. If LOAD BUFFER is applied before the end of transmission, then the transmit sequence will be repeated when the full 20-bit word has been transmitted with no inter-word gap.

When transmission is taking place and there is another word waiting in the output buffer for transmission, the output signal BUFFER FULL becomes valid. If LOAD BUFFER is valid the contents of the buffer are overridden.

The first word for transmission will always be the status word and the top 5 bits of status are the remote terminal address. There are two methods of loading this address along with status into the buffer register.

(a) The terminal address may be applied to the highway (T11-T15) (T15 being MSB terminal address E) along with the rest of the status word and loaded into the buffer with LOAD BUFFER. To initiate transmission, SEND DATA is applied along with LOAD BUFFER or any time after LOAD BUFFER. (The terminal address being the same as the transmitting device).

(b) If bits T11-T15 are left high impedance with the status enabled onto T0-T10 then the hard wired terminal



NOTES:
1. SEND DATA MUST BE APPLIED SAME TIME AS LOAD BUFFER IF HARDWIRED RT ADDRESS IS TO BE INTERNALLY ENABLED ON T11-T15 HIGHWAY.
2. DATA WAS SHIFTED INTO THE INPUT BUFFER REGISTER PRIOR TO VAL WD.
3. LOAD BUFFER ACTIVATION WILL OVERWRITE CONTENTS OF OUTPUT BUFFER REGISTER.

*500 NS TYPICAL PULSE WIDTH.

FIGURE 2. TIMING DIAGRAM

address will be internally enabled onto T11-T15 with signal SEND DATA. Therefore, LOAD BUFFER must be applied during SEND DATA.

When the device is used in conjunction with Protocol Sequencer (MT 32004) the timing of LOAD BUFFER and SEND DATA is under total control of the Protocol Sequencer.

During a message transmission the receive part of MT32008 is disabled and the output TX INHIBIT becomes not valid (output TX INHIBIT is also available).

There are 2 other inputs to MT32008, SEL TX EN and SEL TX DIS. When SEL EN is valid, a pulse on SEL TX DIS disables transmission and a pulse on SEL TX EN enables transmission.

An active low signal on RESET will set the transmitter in the enable mode.

3.0 DETAILED TIMING

RECEIVE MODE

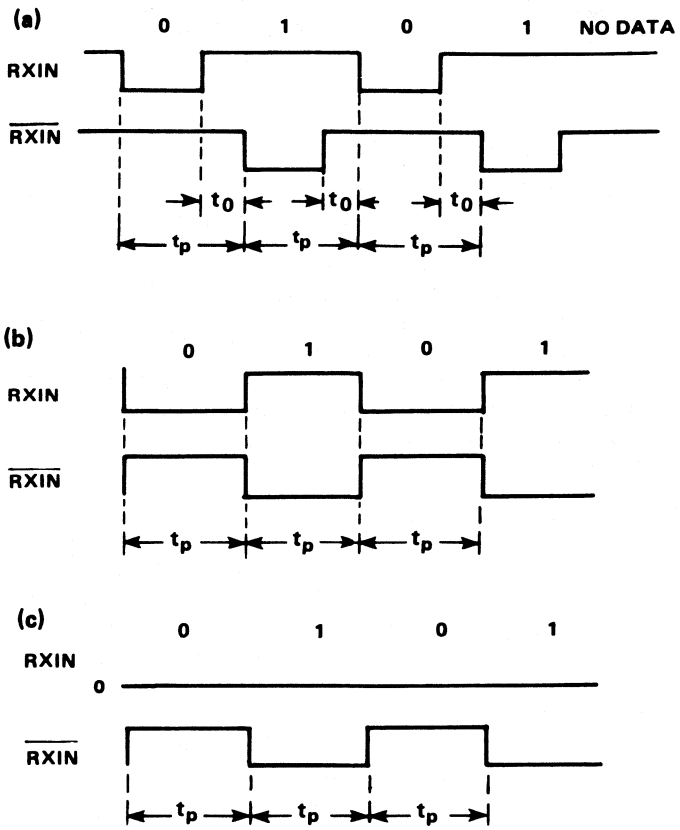
RXIN WAVEFORM REQUIREMENTS

There are three variations of waveform requirements required at the RXIN and RXIN inputs.

Waveform (a) is the ideal. With waveform (b) applied, the device is less immune to noise on these inputs than waveforms (a). With waveform (c) applied, the device is less immune to noise on these inputs than waveform (b).

The device will accept waveforms with tp varying from the ideal (including rise and fall times) of ±150 ns (i.e. 2.0 ±0.15 μs, 1.5 ±0.15 μs, 1.0 ±0.15 μs, 0.5 ±0.15 μs).

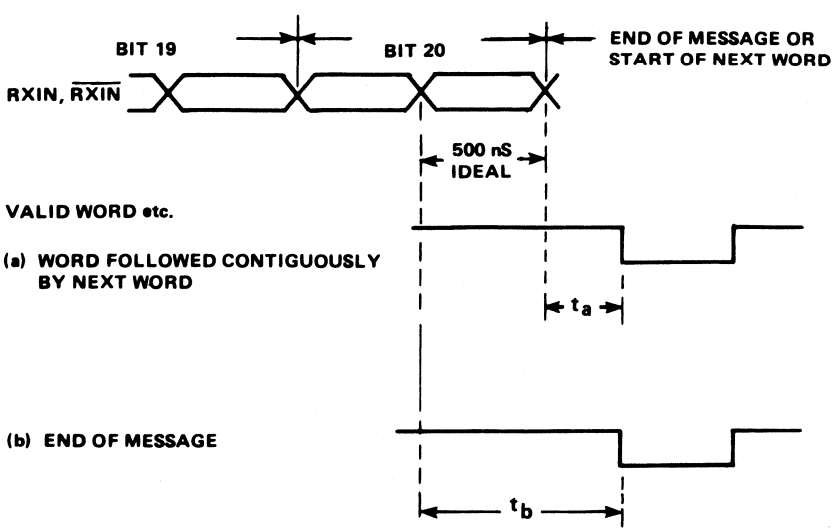
Overlap period (t_o) 10 ns min 400 ns max.



PROPAGATION DELAYS

Propagation Delays over free air temperature range VDD = 5 volts. Propagation delays do not include rise and fall time of outputs.

Propagation delay time RXIN or RXIN to VALID WORD, CMD SYNC, THIS RT, BC DETECT.



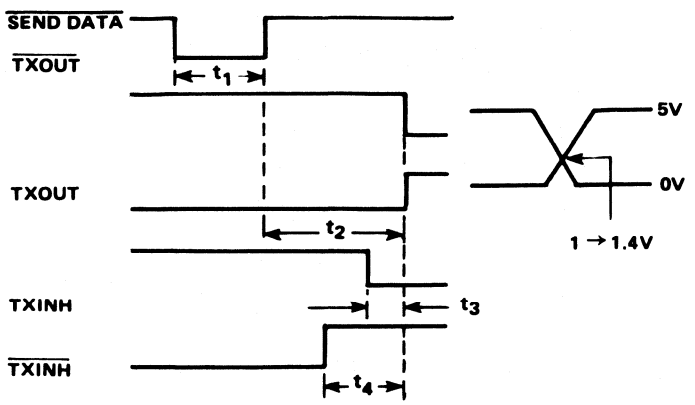
ta	300 ns min	480 ns max.
tb	800 ns min	980 ns max.

Propagation delay time:

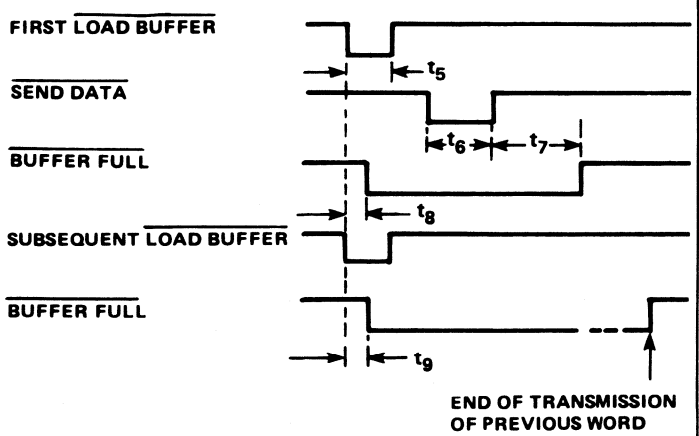
	MIN	MAX	
VAL WD to T0-T15	15	50	
CMD SYNC to THIS RT ADDR IP (remains enabled for half bit period, 500ns ideal)	25	150	ns
CMD SYNC to SEL EN	90	300	ns
EN IP BUFFER to T0-T15	20	75	ns

TRANSMIT MODE

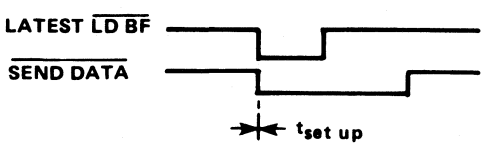
Propagation delay time $\overline{\text{SEND DATA}}$ to TXOUT, TX INH.



Propagation delay time $\overline{\text{LOAD BUFFER}}$ to $\overline{\text{BUFFER FULL}}$



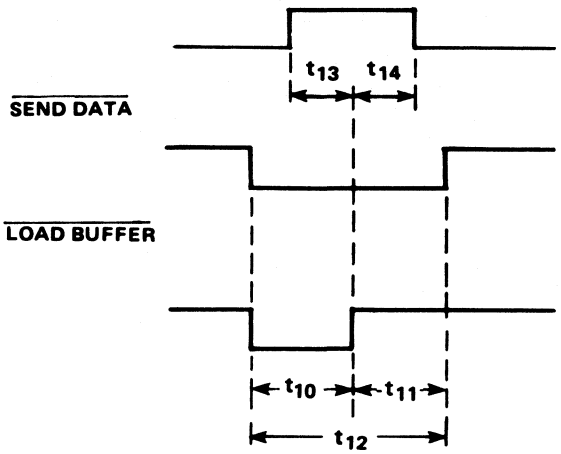
The first load buffer may occur any time before Send Data but no later than send data i.e.



$t_{set\ up}$ MIN = 0 ns

If the device is required to internally load its own RT address to be transmitted with status, then the send data and load buffer signals must be as shown.

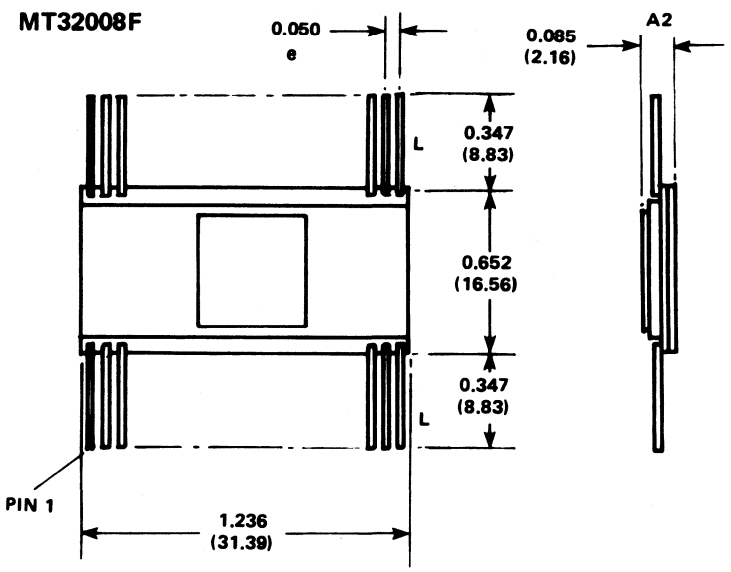
STATUS ENABLED ONTO T0-T10



	MIN	MAX			MIN	MAX	
t_1	250		ns	t_{10}	125		ns
t_2	320	600	ns	t_{11}	125		ns
t_3	30	110	ns	t_{12}	250		ns
t_4	40	150	ns	t_{13}	75		ns
t_5	125		ns	t_{14}	75		ns
t_6	250		ns				
t_7	280	500	ns				
t_8	30	100	ns				
t_9	30	100	ns				

MECHANICAL OUTLINE

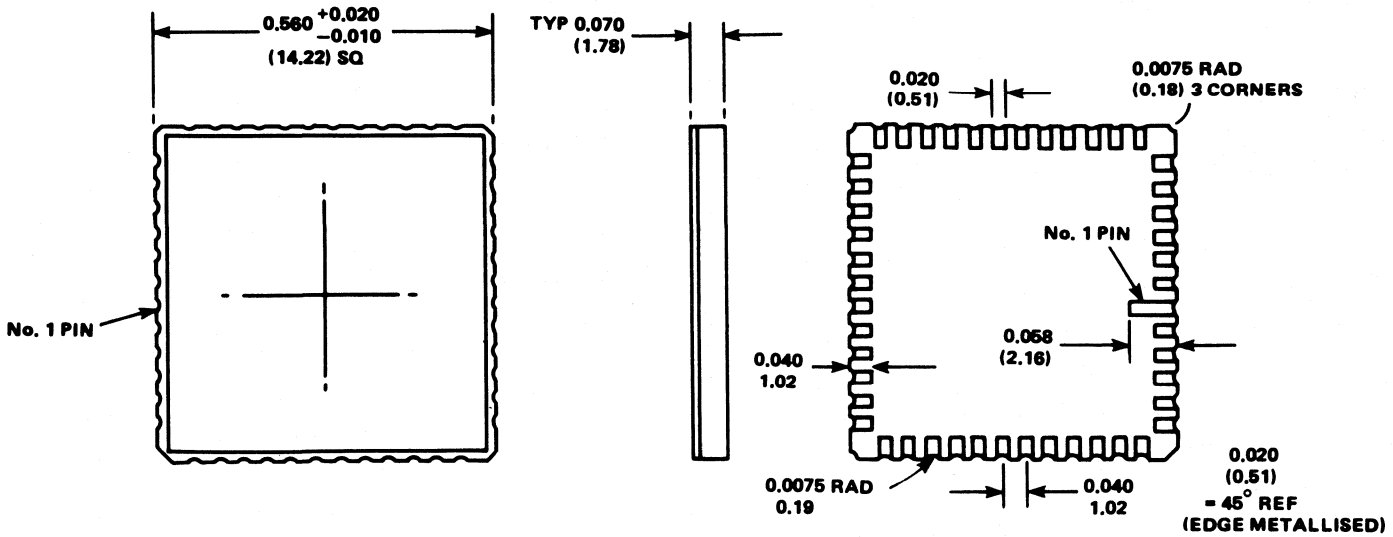
MT32008F



NOTES:
1. Dimensions are in inches (millimeters)
2. MT32008C is a 48 lead Chip carrier configuration.
3. MT32008D is a 48 lead Dual In line configuration.
4. MT30028F is a 48 lead Flatpack configuration.
5. The pin functions shown in table apply to all configurations.

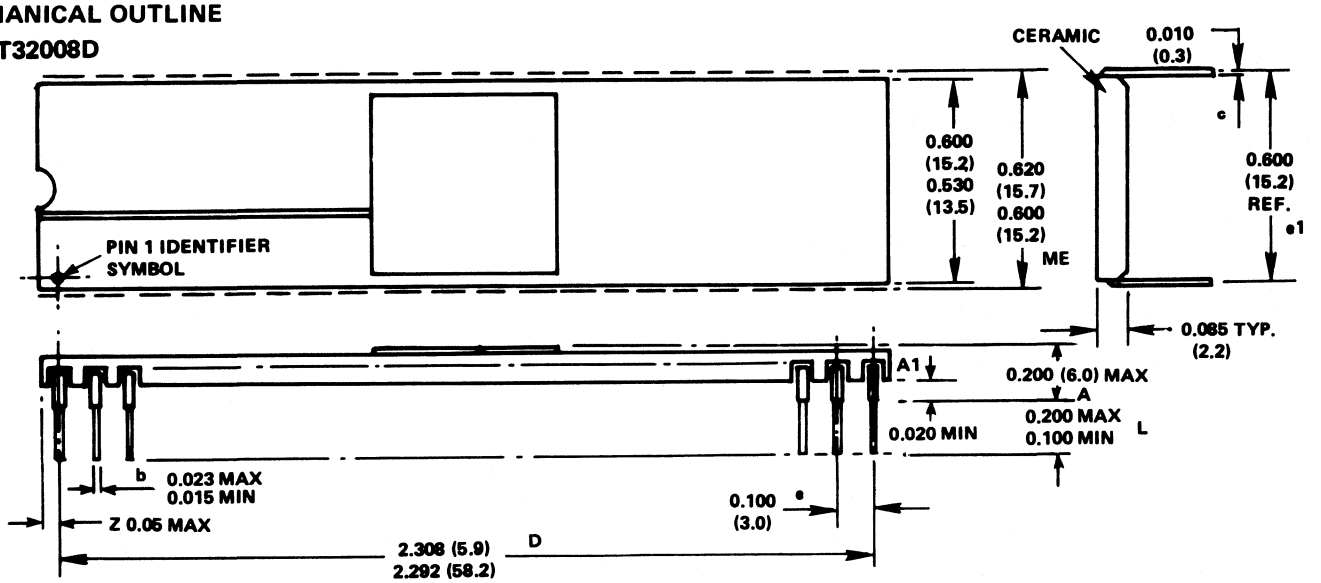
MECHANICAL OUTLINE

MT32008C



MECHANICAL OUTLINE

MT32008D



PIN TYPE TABLE**

PIN	TYPE	PIN	TYPE	PIN	TYPE	PIN	TYPE
1	E	13	C	25	E	37	D
2	E	14	C	26	E	38	D
3	E	15	D	27	E	39	D
4	E	16	C	28	E	40	B
5	E	17	A	29	E	41	A
6	E	18	B	30	E	42	A
7	E	19	B	31	B	43	A
8	A	20	E	32	B	44	D
9	A	21	A	33	B	45	A
10	D	22	—	34	B	46	A
11	C	23	E	35	B	47	—
12	A	24	E	36	D	48	E

**Specifications for each signal type are shown on page 2.

PIN FUNCTION TABLE

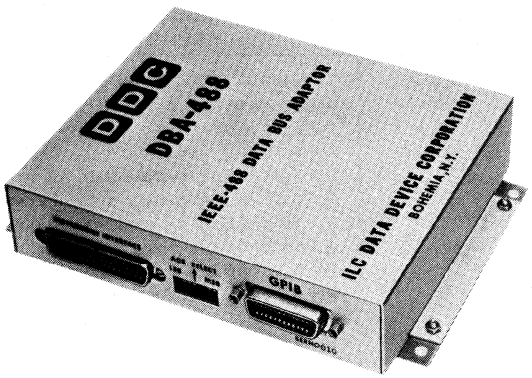
PIN	FUNCTION	DESCRIPTION	PIN	FUNCTION	DESCRIPTION
1	T1	Bit 1 of 16 bit tri-state data highway.	21	$\overline{\text{EN IP BUFFER}}$	Low input level enables the contents of the input buffer register onto the data highway, if SEL EN is valid (high).
2	T2	Bit 2 of 16 bit tri-state data highway.			
3	T3	Bit 3 of 16 bit tri-state data highway.			
4	T4	Bit 4 of 16 bit tri-state data highway.	22	VSS	Power supply ground.
5	T5	Bit 5 of 16 bit tri-state data highway.	23	T8	Bit 8 of 16 bit tri-state data highway.
6	T6	Bit 6 of 16 bit tri-state data highway.	24	T9	Bit 9 of 16 bit tri-state data highway.
7	$\overline{\text{T7}}$	Bit 7 of 16 bit tri-state data highway.	25	T10	Bit 10 of 16 bit tri-state data highway.
8	$\overline{\text{RESET}}$	Low input level initializes the encoder/ decoder and enables transmission.	26	T11	Bit 11 of 16 bit tri-state data highway.
			27	T12	Bit 12 of 16 bit tri-state data highway.
9	$\overline{\text{LOAD BUFFER}}$	Input pulse loads the contents of the data highway into the output buffer register, if SEL EN is valid (high).	28	T13	Bit 13 of 16 bit tri-state data highway.
			29	T14	Bit 14 of 16 bit tri-state data highway.
			30	T15	Bit 15 (MSB) of 16 bit tri-state data highway.
10	$\overline{\text{BUFFER FULL}}$	Low output level identifies that a transmission is taking place and the output buffer register contains the next word for transmission.	31	TERM ADDR E	Terminal address bit E (hard wired).
			32	TERM ADDR D	Terminal address bit D (hard wired).
			33	TERM ADDR C	Terminal address bit C (hard wired).
11	SEL EN	High output level identifies that input THIS RT ADDR IP is the same as THIS RT ADDR (hard wired), and this bus is selected (active).	34	TERM ADDR B	Terminal address bit B (hard wired).
			35	$\overline{\text{TERM ADDR A}}$	Terminal address bit A (hard wired).
			36	$\overline{\text{CMD/STAT SYNC}}$	Output pulse indentifies receipt of a valid command or status sync.
12	$\overline{\text{SEND DATA}}$	Input pulse initiates the serial transmission sequence.	37	$\overline{\text{ANOTHER WORD}}$	Output pulse identifies receipt of a valid sync plus 3 data bits.
13	$\overline{\text{TX OUT}}$	Inverted output to transmitter.	38	$\overline{\text{BC DETECT}}$	Output pulse identifies receipt of a Broadcast command address.
14	$\overline{\text{TX OUT}}$	Output to transmitter.			
15	$\overline{\text{TX INHIBIT}}$	Low output level identifies inhibited TX OUT.	39	$\overline{\text{THIS RT}}$	Output pulse identifies receipt of a command with the valid address.
16	TX INHIBIT	High output level identifies inhibited TX OUT.	40	ADDR PARITY	Address parity bit (hard wired odd).
			41	$\overline{\text{RXIN}}$	Inverted input from receiver.
17	THIS RT ADDR LS	Address bit (hard wired) for dual redundant bus differentiation.	42	RXIN	Input from receiver.
			43	$\overline{\text{16 MHz}}$	16 MHz clock input.
18	RX/TX	Low input level enables external sync generation via $\overline{\text{DATA SYNC IN}}$.	44	$\overline{\text{VALID WORD}}$	Output pulse identifies the receipt of a valid word.
19	$\overline{\text{DATA SYNC IN}}$	Low input level causes data sync generation. High input level causes command sync generation.	45	SEL TX EN	Input pulse enables transmission, if SEL EN is valid (high).
			46	SEL TX DIS	Input pulse disables transmission, if SEL EN is valid (high).
20	THIS RT ADDR IP LS	Input pulse identifies the active dual redundant bus address.	47	VDD	Power supply voltage input.
			48	T0	Bit 0 (LSB) of 16 bit tri-state data highway.

ORDERING INFORMATION

MT32008D

Package
- D = 48 pin DIP
- F = 48 pin Flat Pack
- C = 48 pin Chip Carrier

DATA BUS ADAPTOR FOR IEEE-488 BUS
Controls the Transmission of Data, Timing and Control Signals Between Instrument and BUS



DESCRIPTION

The main components of the DBA-488 are shown in the block diagram, Figure 1. The operation of the device is supervised by the microprocessor according to a program which is stored in the ROM. The interface controller mediates data transfer to and from the IEEE bus. The 32 identical input/output lines at the instrument interface are TTL compatible with a loading or drive capability of one standard TTL load. These 32 lines can be programmed independently for input or output by the microprocessor according to instrument requirements. The bus address of the unit, which is selected manually by the address select switches, is transferred to the interface controller memory immediately after power is turned on.

The DBA-488 Data Bus Adaptor GPIB output complies with all requirements of the IEEE-488-1975 General Purpose Interface Bus Standard. The device is also fully compatible with the Hewlett Packard HP-IB bus without programming changes.

FEATURES

- *DESIGNED TO LINK DDC'S SYNCHRO INSTRUMENTS TO THE IEEE-488 GENERAL PURPOSE INTERFACE BUS. Available as a standard option when an instrument is purchased, or for retrofit.*
- *CAN LINK NEARLY ANY CONTROL OR DATA HANDLING EQUIPMENT TO THE IEEE-488 BUS. All interfacing information is stored as firmware in a plug-in ROM which can be preprogrammed for almost any device with logic inputs or outputs.*
- *A COMPACT, SELF-CONTAINED UNIT. Uses the latest in microprocessor technology, operates from standard 110V or 220V line voltage and requires less than 10 watts. Size is 8.1 x 6.1 x 1.7 inches (20.6 x 15.6 x 4.3 cm) and weight less than 2-1/2 lbs. (1.1 kg.)*
- *EASY TO USE. The DBA-488 Data Bus Adaptor is a preprogrammed logic interface with two connectors, one for the instrument and one for the IEEE-488 bus. No adjustments are required. The bus address is selected by externally available rocker switches.*
- *APPLICATIONS INCLUDE ANY SYSTEM USING THE IEEE-488 BUS. The DBA-488 is used in computer controlled systems such as automatic test equipment (ATE) and process control systems.*

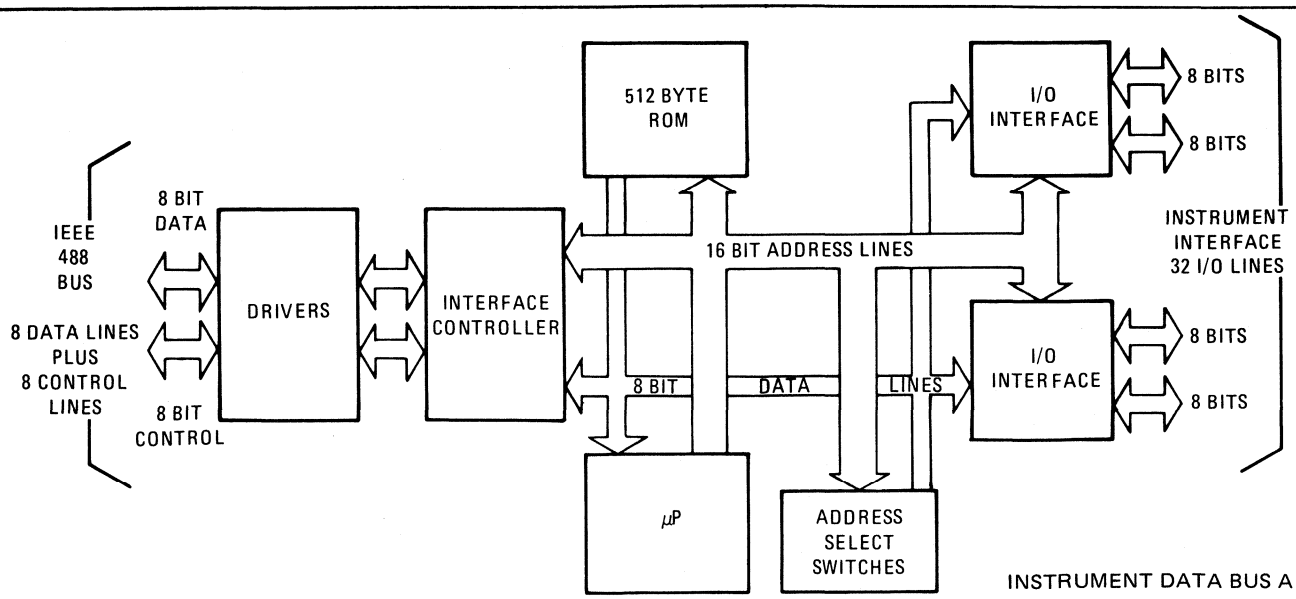


FIGURE 1. DBA-488 BLOCK DIAGRAM

INSTRUMENT DATA BUS ADAPTOR FOR IEEE-488 BUS

TECHNICAL INFORMATION

INTERCONNECTIONS

The DBA-488 is connected to the IEEE-488 bus with the standard IEEE-488 bus connector, and meets all IEEE-488-1975 compatibility standards.

The DBA-488 instrument connector, (see Figure 2) has pins for switched line voltage and up to 32 input/output logic lines. This 50 pin connector is the same as the connector used at the rear of DDC's synchro instruments.

When the DBA-488 is ordered as an option with a new DDC synchro instrument, the DBA-488 instrument connector is wired to the instrument rear connector through a cable. Pin connections are shown in Figure 3. For retrofitting, the customer may return his instrument to the factory (consult factory for prices) or order a DBA-488 separately as indicated in the ordering information. Separately ordered units include an unwired mating connector for the DBA-488 instrument connector, and the customer will usually want to wire the instrument power switch to the instrument connector.

COMMAND SEQUENCES

The two basic command sequences for DDC's synchro instruments which can be initiated by the IEEE-488 bus controller are given in Figure 4. The Talk Sequence is used with the SR-102A (HSR-102A), the SR-202 (HSR-202), and the SR-103 (HSR-103) which are all angle indicators. The Listen Sequence is used to send control words to all these instruments and to the SR-400 (SR-460) angle simulator as well. A list of control words for each instrument is given in Figure 5. Correspondence on the IEEE-488 bus is generally ASCII encoded.

The SR-400 (SR-460) must be able to listen to both data words and control words. The controller indicates which type of information will be transmitted by selecting the LSB of the MLA as indicated in Figure 4.

At the end of a transmission, the DBA-488 will respond to either an EOI line signal for an IEEE-488 bus, and/or a Carriage Return signal for the HP-IB bus. This is shown by the command sequences in Figure 4.

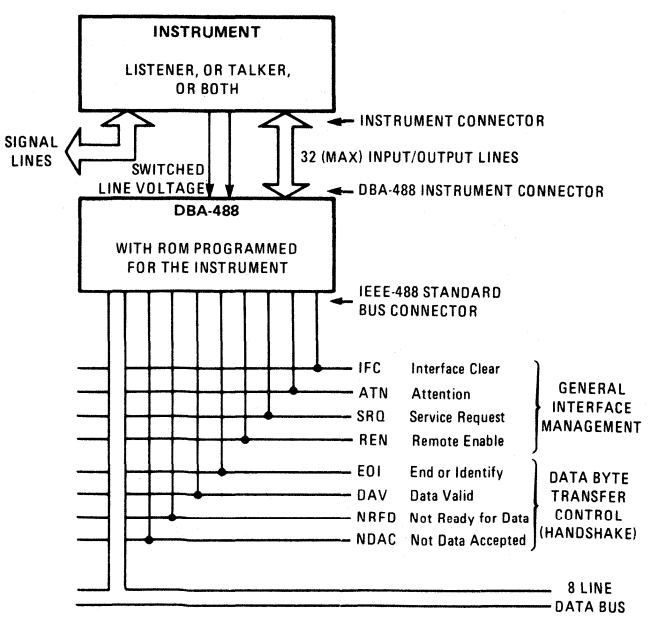


FIGURE 2. DBA-488 CONNECTION DIAGRAM

DBA-488	SR-102A; HSR-102A; SR-202; HSR-202		SR-103; HSR-103		SR-400; SR-460	
Pin No.	Function	Connects to Pin	Function	Connects to Pin	Function	Connects to Pin
1	Internal Connec.		Internal Connec.		Internal Connec.	
2	Internal Connec.		.001°	44	Internal Connec.	
3	Internal Connec.		.002°	43	Internal Connec.	
4	Internal Connec.		.004°	42	Internal Connec.	
5	Internal Connec.		.008°	41	Internal Connec.	
6	.01°	45	.01°	13	100°	33
7	.02°	28	.02°	28	200°	17
8	.04°	12	.04°	12	Internal Connec.	
9	.08°	46	.08°	29	Internal Connec.	
10	Internal Connec.		Internal Connec.		.8°	30
11	Internal Connec.		Internal Connec.		.4°	47
12	200°	17	200°	50	.2°	13
13	100°	33	100°	49	.1°	29
14	80°	50	80°	47	.08°	46
15	40°	16	40°	46	.04°	12
16	20°	32	20°	45	.02°	28
17	10°	49	10°	48	.01°	45
18	Inhibit	10	Inhibit	27	Internal Connec.	
19	Lamp Test	26	Lamp Test	38	Internal Connec.	
20	Data Enable	43	Unipolar/Bipolar	39	SYN/RES Select	1
21	Bandwidth	8	Bandwidth	20	Strobe	6
22	Converter Busy	44	Converter Busy	11	Lamp Test	26
23	Bite	27	Bite	40	Internal Connec.	
24	Control 1 for Input Level	41	Internal Connec.		Control 2 for Input Level	42
25	Control 2 for Input Level	42	Internal Connec.		Control 1 for Input Level	41
26	8°	15	8°	33	80°	50
27	4°	31	4°	16	40°	16
28	2°	48	2°	32	20°	32
29	1°	14	1°	17	10°	49
30	.8°	30	.8°	14	8°	15
31	.4°	47	.4°	31	4°	31
32	.2°	13	.2°	15	2°	48
33	.1°	29	.1°	30	1°	14
34	GND	9	GND	4	GND	9
35	GND	9	GND	4	GND	9
36	Power Hi	36*	Power Hi	36*	Power Hi	39*
37	Power Lo	38*	Power Lo	37*	Power Lo	40*
38–50	Spare Pins		Spare Pins		Spare Pins	

FIGURE 3. CONNECTIONS BETWEEN DBA-488 AND SYNCHRO INSTRUMENTS

*Switched AC line voltage must be wired to these pins from the instrument front panel power switch.

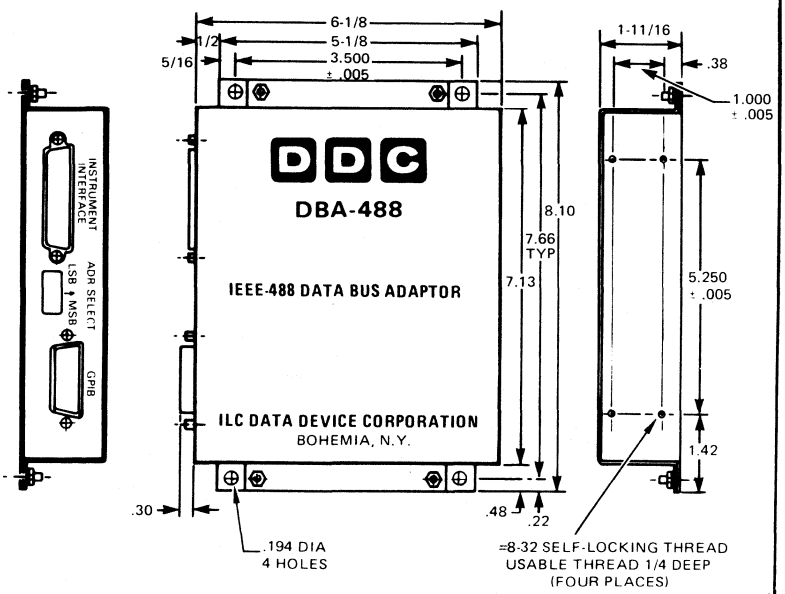
Note for SR-102A (HSR-102A) and SR-202 (HSR-202):
For synchro operation, jumper pins 1 and 2 on the instrument rear connector. For resolver operation, do not jumper.

Note For SR-103:
For synchro operation on channel 1, jumper pins 34 and 35 on instrument rear connector. For synchro operation on channel 2, jumper pins 18 and 35. For resolver operation on either channel, do not jumper.

COMMAND CODE			FUNCTION
SR-102A (HSR-102A) SR-202 (HSR-202)	SR-103 (HSR-103)	SR-400 (SR-460)	
P (Preset)			Preset to 26V L-L, high bandwidth, no inhibit, and no lamp test
	P (Preset)		Preset to unipolar input, high bandwidth, no inhibit, and no lamp test.
		P (Preset)	Preset to 26V L-L output
1 (11.8V)		1 (11.8V)	Sets L-L voltage level for
2 (26V)		2 (26V)	either angle indicator in-
9 (90V)		9 (90V)	put or angle simulator output
H (High)	H (High)		Selects high or low band-
L (Low)	L (Low)		width
		S (Synchro)	Selects Synchro or Resol-
		R (Resolver)	ver output mode
	U (Unipolar)		Selects unipolar or bi-
	B (Bipolar)		polar input
I (Inhibit)	I (Inhibit)	I (Inhibit)	Inhibits the converter or
F (Follow)	F (Follow)	F (Follow)	allows it to follow (track) the input
T (Test)	T (Test)	T (Test)	Test lamps (T) or dis-
D (Display)	D (Display)	D (Display)	plays the data (D)
A (Angle)			Sets display to input angle
Z (Zero)			(A) or to 000.00 (Z)

FIGURE 5. COMMAND CODE FUNCTIONS

MECHANICAL OUTLINE



ORDERING INFORMATION

1. DBA-488 Ordered Separately for Retrofit

When a DBA-488 is ordered separately, a mating connector for the instrument interface is supplied, but is not wired.* The standard mating connector for IEEE-488 bus is not supplied. Mounting hardware is included for the particular instrument determined by the choice of ROM programming.

DBA-488–SR103 – 220

- 220 → Line Voltage and Frequency
  - Blank = 110V and 60 Hz
  - 220 = 220V amd 50/60 Hz
- SR103 → ROM Programming
  - SR-102A = For SR-102A, HSR-102A, SR-202, and HSR-202 instruments.
  - SR103 = For SR-103 and HSR-103 instruments
  - SR400 = For SR-400 and SR-460 instruments

*The DBA-488 does not have a power switch. Line voltage is supplied via the instrument interface connector. If the power switch on an instrument is to control the DBA-488, the switch must be wired to pins on the instrument connector. This requires a modification for most DDC instruments.

2. DBA-488 and Instrument Ordered Together

To order a DBA-488 together with an SR-102A (HSR-102A), SR-103 (HSR-103), SR-202 (HSR-202) or SR-400 (SR-460) instrument, add a -DBA-488 to the end of the ordering part number. When ordered this way, the DBA-488 is mechanically and electrically connected to the instrument. For the SR-102A (HSR-102A) or the SR-103 (HSR-103), the DBA-488 is mounted adjacent to the instrument on a 19" rack panel. For the SR-202 (HSR-202) or the SR-400 (SR-460), the DBA-488 is mounted with a bracket on the rear of the instrument. In all cases, the line voltage power switch on the instrument is wired to control power to the DBA-488. The only component not supplied is the standard mating connector to the IEEE-488 bus.

3. Custom Programming

The ROM in the DBA-488 may be custom programmed for linking other devices to the IEEE-488 bus. Consult the factory for further information.

COMMAND SEQUENCE FOR LISTENING

LISTEN SEQUENCE	EXPLANATION
ATN = 1	Controller sets ATN (Attention) line to true.
MLA	Controller transmits device listen addresss on the data lines. For the SR-400 (SR-460) the LSB is set either to true to indicate that control words will be sent, or to false to indicate that data will be sent.
ATN = ϕ	Controller returns ATN line to false.
CONTROL WORDS OR DATA	Controller (or another device activated by the controller) transmits ASC II encoded control words or data on the data lines.
EOI = 1 AND/OR CARRIAGE RETURN	Controller or other device signals end of transmission by setting EOI (End or Identify) line to true during the last word or command, or by transmitting a Carriage Return after the last word or command.
ATN = 1	Controller sets ATN line to true.
UNL	Controller transmits a UNL (Unlisten) command on the data lines.
ATN = ϕ	Controller returns ATN line to false.

COMMAND SEQUENCE FOR TALKING

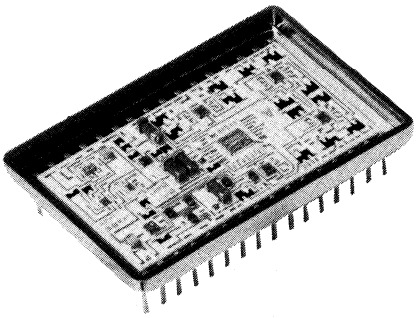
TALK SEQUENCE	EXPLANATION
ATN = 1	Controller sets ATN (Attention) line to true.
MTA	Controller transmits device talk address on the data lines.
ATN = ϕ	Controller returns ATN line to false.
DATA	Device transmits ASC II encoded data (First out is MSB) on the data lines.
EOI = 1 WITH CARRIAGE RETURN	Device signals end of transmission by setting the EOI (End or Identify) line to true and simultaneously transmitting a Carriage Return on the data lines.
ATN = 1	Controller sets ATN line to true.
UNT	Controller transmits a UNT (Untalk) command on the data lines.
ATN = ϕ	Controller returns ATN line to false.

FIGURE 4. COMMAND SEQUENCES

ADDENDUM

DDC
ILC DATA DEVICE CORPORATION

14 BIT DEGLITCHED D/A CONVERTER
10MHz Update Rate; Voltage Output



FEATURES

- *FULL FUNCTION: INCLUDES INPUT REGISTERS AND TRACK/HOLD DEGLITCHER OUTPUT*
- *HIGH SPEED: 10MHz UPDATE RATE FOR SMALL STEP CHANGES*
- *LOW GLITCH: 10mVpp GLITCH VOLTAGE*
- *SMALL SIZE: 32 PIN TDIP HYBRID*
- *WIDE OPERATING TEMPERATURE: -55° C to +125° C*

DESCRIPTION:

The DAC-02310 is a 14 bit, 10 MHz update rate, deglitched hybrid D/A converter with a low impedance voltage output. Its input registers, precision DC voltage reference and track/hold deglitcher output provide the complete solution to low noise DAC requirements. Packaged in a small 32 pin TDIP hybrid, the DAC-02310 operates over the full -55° C to +125° C temperature range and is available screened to MIL-STD-883.

DAC-02310 is available in linearity grades of 13 bits (±0.006%) and 12 bits (±0.012%). It can be pin programmed for 5 different output voltage ranges; and offset, gain, and pedestal errors can be trimmed to zero with external potentiometers.

With its 14 bit resolution, low glitch voltage output and small hermetic package, the DAC-02310 is ideal for the most demanding low noise DAC requirements. It is particularly well suited for applications such as vector-stroke CRT displays, waveform generators and automatic test equipment.

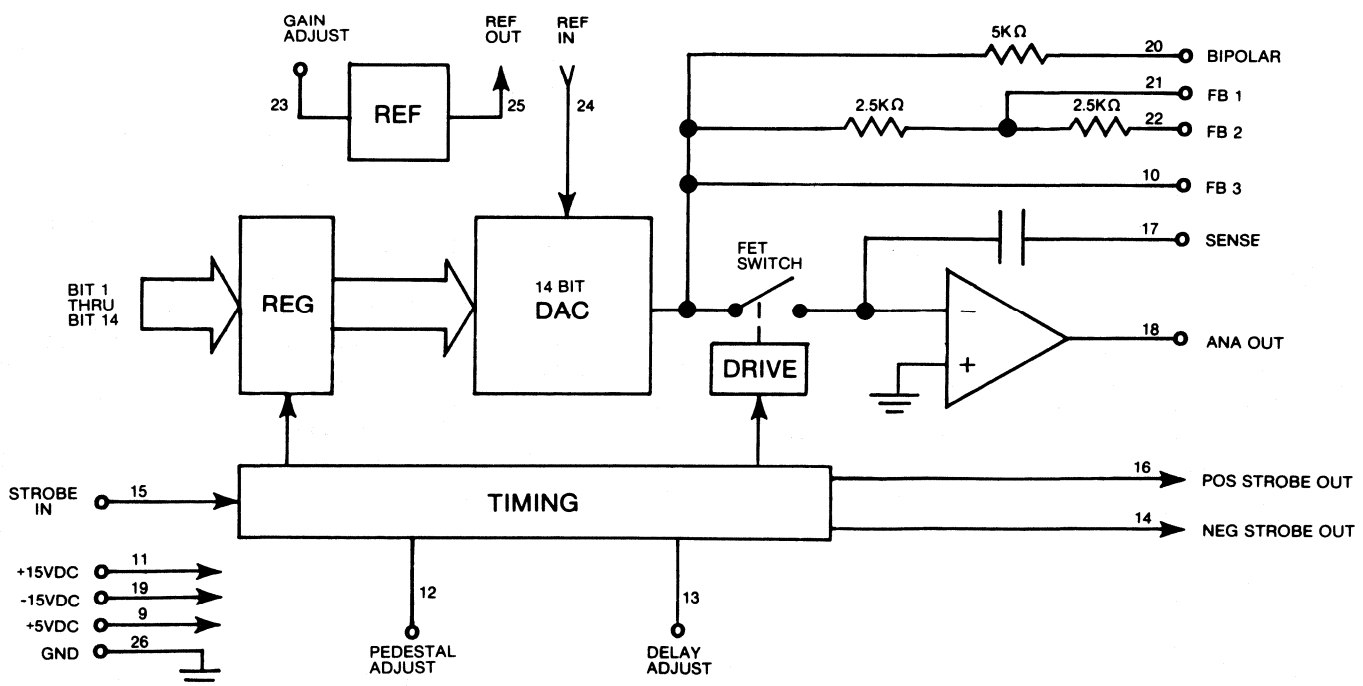


FIGURE 1. DAC-02310 BLOCK DIAGRAM

SPECFICATIONS — Typical values at +25°C and nominal power supply voltages unless otherwise specified.			
PARAMETER	UNITS	VALUE	
		13 BIT LIN	12 BIT LIN
RESOLUTION	**Bits**	**14**	**14**
ACCURACY			
Linearity Error	% FSR	± 0.006 max	± 0.012 max
Linearity Tempco	ppm/° C	± 1 max	± 2 max
Gain Error(1)	% FSR	± 0.1	± 0.2
Gain Tempco	ppm/° C	± 25 max	± 25
Offset Error(1)	mV	± 10	± 20
Offset Tempco	ppm FSR/° C	20 max	20 max
Pedestal Error(1)	mV	± 10	± 20
Pedestal Tempco(2)	µV/° C	50	50
Monotonicity	Bits	13	12
DYNAMIC CHARACTERISTICS			
Settling Time to ±½ LSB			
±10V Full Scale Change	µsec	1.8 max	
±5V Full Scale Change	µsec	1.1 max	
±2.5V Full Scale Change	µsec	0.6 max	
1 LSB Change	nsec	50 max	
Slew Rate	V/usec	20 typ 15 min	
Glitch(3)			
Voltage	mVpp	10 typ 30 max	
Energy	mV• nsec	250 typ 750 max	
DIGITAL INPUTS			
Logic Compability		TTL	
Data Inputs			
Logic "1" Level	V	+2.0 to +5	
Logic "0" Level	V	0 to +0.8	
Loading		1 standard LS TTL load	
Coding (negative output)		Offset Binary (Bipolar)	
		Binary (Unipolar)	
Strobe Input(4)			
Logic "1" Level	V	+2.0 to 5	
Logic "0" Level	V	0 to +0.8	
Loading		2 standard S TTL loads	
Width	nsec	10 min	
ANALOG OUTPUT			
Voltage Ranges(5)	V	±10, ±5, ±2.5, 0 to -10, 0 to -5	
Current Load	mA	±5 max	
Impedance	Ω	0.1 max	
Short Circuit Duration	sec	5 max	
REFERENCE			
Output Voltage	V	-10 ±0.1	
Output Current	mA	±1 max	
Input Voltage	V	0 to -10	
Input Impedance	Ω	3.3K	
POWER SUPPLIES			
+15V Supply			
Tolerance	%	±5	
Max Voltage	V	+18 max	
Current Drain	mA	40 typ 50 max	
-15V Supply			
Tolerance	%	±5	
Max Voltage	V	-18 max	
Current Drain	mA	25 typ 35 max	
+5V Supply			
Tolerance	%	±10	
Max Voltage	V	+5.5 max	
Current Drain	mA	70 typ 100 max	
TEMPERATURE RANGE			
Operating (Case)			
-1 option	°C	-55 to +125	
-3 option	°C	0 to +70	
Storage	°C	-65 to +150	
PHYSICAL CHARACTERISTICS			
Package		32 pin TDIP	
Size	in (mm)	1.15x1.75x0.21 (29x44x5)	
Weight	oz (g)	0.67 (19)	

NOTES: (1) Gain, offset, and pedestal errors are trimmable to zero.
(2) Pedestal tempco is with no delay adjust capacitor pin 13 to pin 14.
(3) Glitch is at 1 MHz update rate with a 5MHz filter.
(4) Strobe input is a positive pulse. Data is transferred on the rising edge.
(5) Output voltage ranges are pin programmable.

TECHNICAL DESCRIPTION

GENERAL

DAC-02310 is a completely self-contained deglitched D/A converter. As shown in the block diagram of Figure 1, it contains a 14 bit DAC, input registers, a precision DC reference, a track/hold deglitcher output and timing circuits. Its layout and compatible components provide the complete solution to low noise DAC design problems.

TIMING

Upon application of a STROBE IN signal the input registers are updated and the DAC-02310 output is held constant. As shown in Figure 2, the rising edge of the STROBE IN signal latches the input data. Internal timing circuits generate a POS STROBE OUT pulse which is used to open the FET switch at the op amp summing point. The output remains constant since the op amp feedback capacitor is charged. During this hold mode interval of approximately 40 nanoseconds, the DAC is changing value and its output glitch is settling to zero. At the end of the hold interval, POS STROBE OUT returns to is original track mode level and the FET switch closes. The DAC-02310 then smoothly changes to its new output level. The track/hold has effectively "masked out" the DAC glitch. POS STROBE OUT (pin 16) and NEG STROBE OUT (pin 14) should not be loaded with external circuitry.

DELAY ADJUST

The hold time interval is internally set to approximate 40 nanoseconds. For applications, such as CRT displays, which may require matched delays, an external DELAY ADJUST pin is provided. By adding a capacitor from pin 13 to pin 14, the hold time interval is made longer. This effectively increases the delay of the DAC-02310. Figure 3 illustrates the effect on hold time of adding capacitance to pin 13.

EXTERNAL TRIMS

Factory adjustment of DAC-02310 offset, gain and pedestal errors result in performance that is adequate for most applications. For more critical applications, DAC-02310 provides pins for externally trimming offset, gain and pedestal errors to zero. Figure 4 illustrates trim pot values and circuit connections for external trims.

OUTPUT VOLTAGE PROGRAMMING

DAC-02310 can be programmed for 5 different output voltage ranges by external jumpers between pins. Figure 5 illustrates the jumper connections required to yield ±10V, ±5V, ±2.5V, 0 to -10V, and 0 to -5V output voltage ranges.

INTERNAL REFERENCE

DAC-02310 contains a precision -10 volt internal reference which is made available for external use. For normal operation, REF OUT (Pin 25) must be jumpered to REF IN (Pin 24). Under these conditions, a maximum output current of 1 milliamp will be provided by the internal reference, while maintaining rated performance.

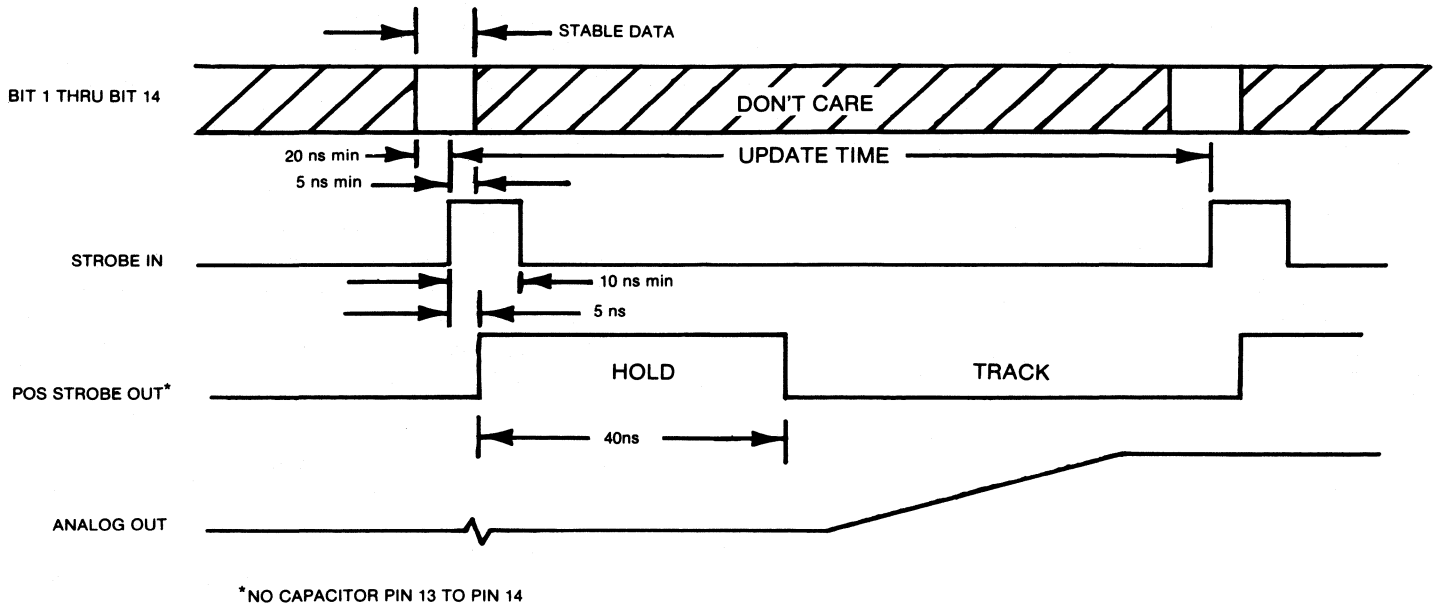


FIGURE 2. TIMING DIAGRAM

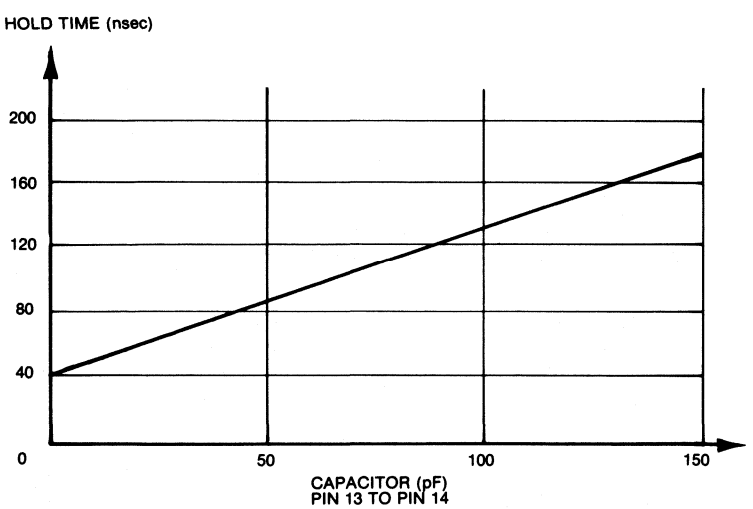


FIGURE 3. DELAY (HOLD) TIME ADJUST

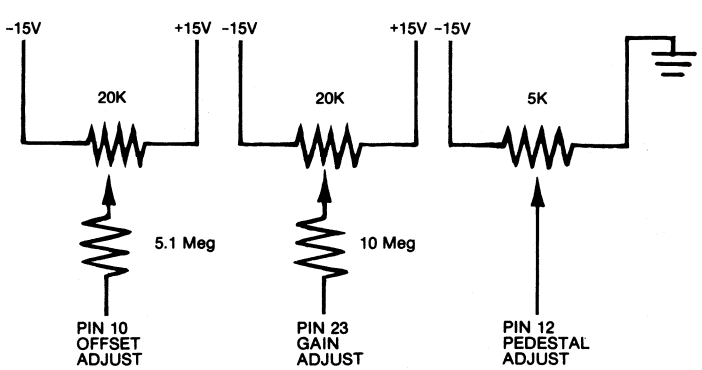


FIGURE 4. EXTERNAL TRIM CIRCUITS

	JUMPER CONNECTIONS				
Voltage Range	Pin 22 to	Pin 21 to	Pin 20 to	Pin 17 to	Pin 24 to
±10V	Pin 18	—	Pin 25	Pin 18	Pin 25
±5V	Pin 18	Pin 22	Pin 25	Pin 18	Pin 25
±2.5V	Pin 10	Pin 18	Pin 25	Pin 18	Pin 25
0 to -10V	Pin 18	Pin 22	—	Pin 18	Pin 25
0 to -5V	Pin 10	Pin 18	—	Pin 18	Pin 25

FIGURE 5. OUTPUT VOLTAGE PROGRAMMING

	OUTPUT VOLTAGE*	
INPUT DATA	BIPOLAR	UNIPOLAR
00 0000 0000 0000	+5.0000V	0
01 1111 1111 1111	+0.0006V	−4.9994V
10 0000 0000 0000	0	-5.0000V
11 1111 1111 1111	-4.9994V	-9.9994V

*10 Volt Full Scale Range

FIGURE 6. INPUT DATA CODING

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 8	17	Sense
2	Bit 7	18	Analog Out
3	Bit 6	19	-15 Volts
4	Bit 5	20	Bipolar
5	Bit 4	21	Feedback 1
6	Bit 3	22	Feedback 2
7	Bit 2	23	Gain Adjust
8	Bit 1 (MSB)	24	Reference In
9	+5 volts	25	Reference Out
10	Feedback 3	26	Ground
11	+15 Volts	27	Bit 14 (LSB)
12	Pedestal Adjust	28	Bit 13
13	Delay Adjust	29	Bit 12
14	Neg. Strobe Out	30	Bit 11
15	Strobe In	31	Bit 10
16	Pos. Strobe Out	32	Bit 9

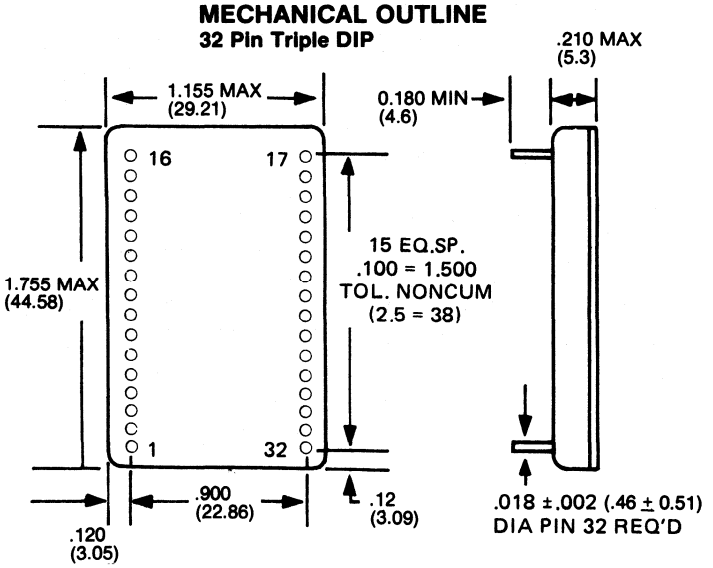
ORDERING INFORMATION

DAC-02310-103

- Linearity Grade:
  - 3=13 bit
  - 2=12 bit
- Reliability Grade:
  - 1=Conforms to MIL-STD-883
  - 0=Same except preburn-in test and burn-in are omitted.
- Operating Temperature Range
  - 1=-55° C to +125° C
  - 3=0° C to +70° C

MECHANICAL OUTLINE

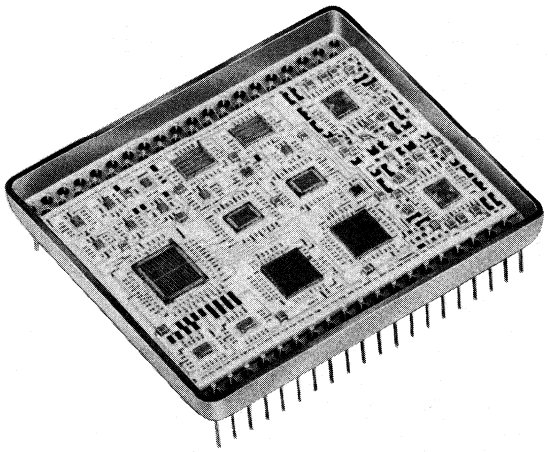
32 Pin Triple DIP



NOTES:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ± 0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-883, Method 2003.

DDC
ILC DATA DEVICE CORPORATION

MIL-STD-1553 DUAL REDUNDANT REMOTE TERMINAL HYBRID



DESCRIPTION

The BUS-65112 is a complete dual redundant MIL-STD-1553 Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. Based upon DDC custom ICs, it includes 2 transceivers, 2 encoder/decoders, 2 bit processors, RTU protocol, data buffers, and timing control logic. It supports all 13 mode codes for dual redundant operation, any combination of which can be illegalized.

Parallel data transfers are accomplished with a DMA type handshaking, compatible with most CPU types. Data transfers to/from memory are simplified by the latched command word and word count outputs. Error detection and recovery are enhanced by BUS-65112 special features. A 14 bit built-in-test word register stores RTU information, and sends it to the Bus Controller in response to the Mode Command Transmit Bit Word. The BUS-65112 performs continuous on-line wrap-around self-test, and provides 4 error flags to the host CPU. Inputs are provided for host CPU control of 6 bits of the RTU Status Word.

Its small hermetic package, −55°C to +125°C operating temperature range, and complete RTU operation make the BUS-65112 ideal for most MIL-STD-1553 applications.

FEATURES

- *SMALL SIZE: 1.9" x 2.1"*
- *COMPLETE RTU PROTOCOL*
- *SUPPORTS 13 MODE CODES: ANY COMBINATION CAN BE ILLEGALIZED*
- *TRANSFERS DATA WITH DMA TYPE HANDSHAKING*
- *LATCHED OUTPUTS FOR COMMAND WORD AND WORD COUNT*
- *14 BIT BUILT-IN-TEST WORD REGISTER*
- *4 ERROR FLAG OUTPUTS*
- *CONTINUOUS ONLINE SELF-TEST*

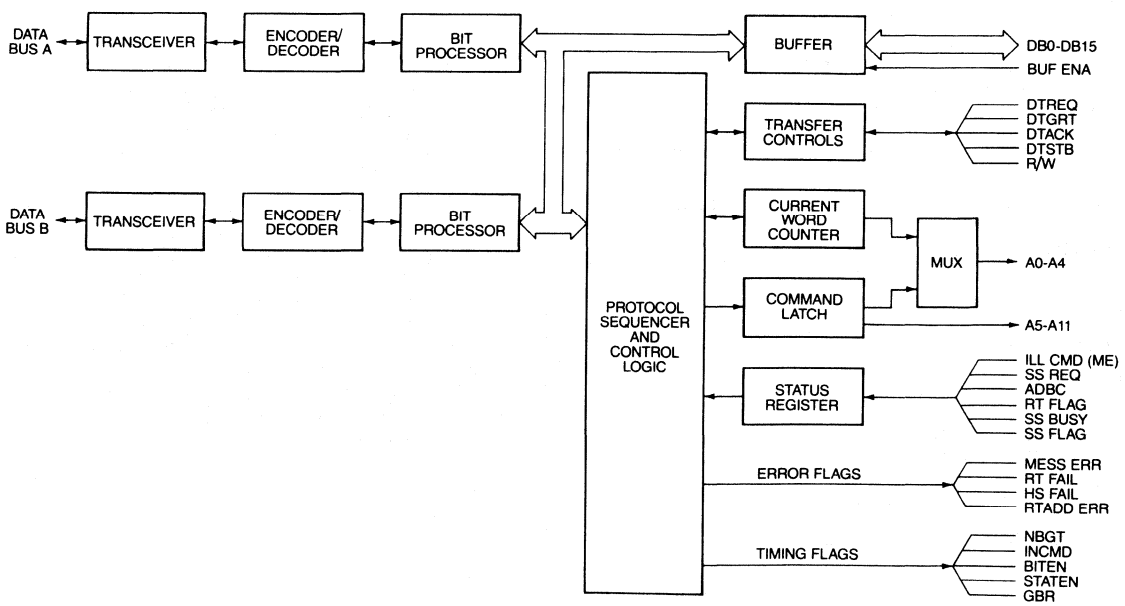


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS – Values at nominal power supply voltages and +25°C unless otherwise specified		
PARAMETER	**UNITS**	**VALUE**
RECEIVER		
Differential Input Impedance (DC to 1MHz)	kΩ	4 min
Differential Input Voltage	V_{p-p}	40 max
Input Threshold (Direct Coupled)	V_{p-p}	1 typ
CMRR (DC to 2MHz)	dB	40 min
CMV (DC to 2MHz)	V	±10 min
TRANSMITTER		
Differential Output Voltage		
Direct Coupled (Across 145Ω Load)	V_{p-p}	30 typ
Transformer Coupled (at Stub)	V_{p-p}	21 typ
Output Rise and Fall Times	ns	130 typ
Output Noise	mV_{p-p}	10 max
LOGIC		
V_{IH}	V	2.4 min
V_{IL}	V	0.7 max
I_{IH} (Note 1) (V_{IH}=2.7V)	mA	−0.2 max
I_{IH} (Note 2) (V_{IH}≥2.4V)	μA	±10 max
I_{IL} (Note 1) (V_{IL}=0.4V)	mA	−0.7 max
I_{IL} (Note 2) (V_{IL}≤0.7V)	μA	±10 max
V_{OH} (Note 3) (I_{OH}=0.3 mA)	V	2.4 min
V_{OH} (Note 4) (I_{OH}=3 mA)	V	2.4 min
V_{OL} (Note 3) (I_{OH}=−1.6 mA)	V	0.4 max
V_{OL} (Note 5) (I_{OH}=−4 mA)	V	0.4 max
V_{OL} (Note 6) (I_{OH}=−12 mA)	V	0.4 max
C_I (f=1 MHz)	pF	5 max
C_O (f=1 MHz)	pF	10 max
C_{IO} (Note 6) (f=1 MHz)	pF	15 max
POWER SUPPLIES		
+5VDC		
Tolerance	%	±10 max
Current Drain	mA	170 max
+15VDC		
Tolerance	%	±5 max
Current Drain	mA	130 max
−15VDC		
Tolerance	%	±5 max
Current Drain		
Idle	mA	130 max
25% Transmit	mA	175 max
100% Transmit	mA	305 max
TEMPERATURE RANGE		
Operating (Case)	°C	−55 to +125
Storage	°C	−55 to +125
PHYSICAL		
Size	in. (mm)	1.9x2.1x0.25 (48x53x6)
Weight	oz(g)	1 (28)

Notes:
1. I_{IH} and I_{IL} for input pins 12, 13, 14, 15, 53, 54, 55.
2. I_{IH} and I_{IL} for all input pins other than in Note 1.
3. V_{OH} and V_{OL} for output pins 1, 2, 3, 16, 25, 27, 28, 35, 40, 41, 42, 65, 73, 78.
4. V_{OH} for all output pins other than in Note 3.
5. V_{OL} for output pins 21, 22, 24, 26, 29, 60, 61, 62, 63, 64.
6. V_{OL} and C_{IO} for pins 43 thru 50 and 4 thru 11.

GENERAL

The BUS-65112 is a complete dual redundant Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. It is fully compliant with MIL-STD-1553B and supports all message formats. As shown in Figure 1, it includes 2 transceivers, 2 encoder/decoders, 2 bit processors, an RTU protocol sequencer, control logic and output latches and buffers. With the addition of 2 data bus transformers (DDC P/N BUS-25679), BUS-65112 is ready to connect to the MIL-STD-1553 data bus.

Data is transferred to and from the subsystem host CPU over a 16 bit parallel highway, which is isolated by a set of bidirectional buffers. All transfers are made with a DMA type handshaking of request, grant, acknowledge. Read/write and data strobes are provided to simplify interfacing to external RAM memory. Also simplifying the RAM interface, is the availability of latched command word and word counter. These address signals may be used to map the data directly to and from RAM.

BUS-65112 allows the subsystem host CPU to control 6 of the bits in the RTU status word. Of particular interest is the Illegal Command input which may be used to set the message error bit and illegalize any combination of the 13 mode commands that the BUS-65112 executes. Four error flags are provided to the subsystem host CPU by the BUS-65112, to aid in assessing its condition. In addition, a continuous online self-test is performed by the BUS-65112 on every transmission. Each transmitted message is wrapped around to the decoder and compared to the intended message. Any discrepancy is flagged as an error.

TIMING

The subsystem host CPU interface to the BUS-65112 is simple and compatible with most microprocessors. Figures 2 and 3 illustrate typical MIL-STD-1553 messages of transmit data and receive data respectively. In each case, $\overline{\text{NBGT}}$ identifies the start of the message, and INCMD identifies that a command is being processed. The handshake sequence $\overline{\text{DTREQ}}$, $\overline{\text{DTGRT}}$, and $\overline{\text{DTACK}}$ is used to transfer each word over the parallel data highway. $\overline{\text{DTSTR}}$ and R/$\overline{\text{W}}$ are used to control transfers to RAM memory. $\overline{\text{GBR}}$ identifies a "good block received", when a received message has passed all validation checks and has the correct word count.

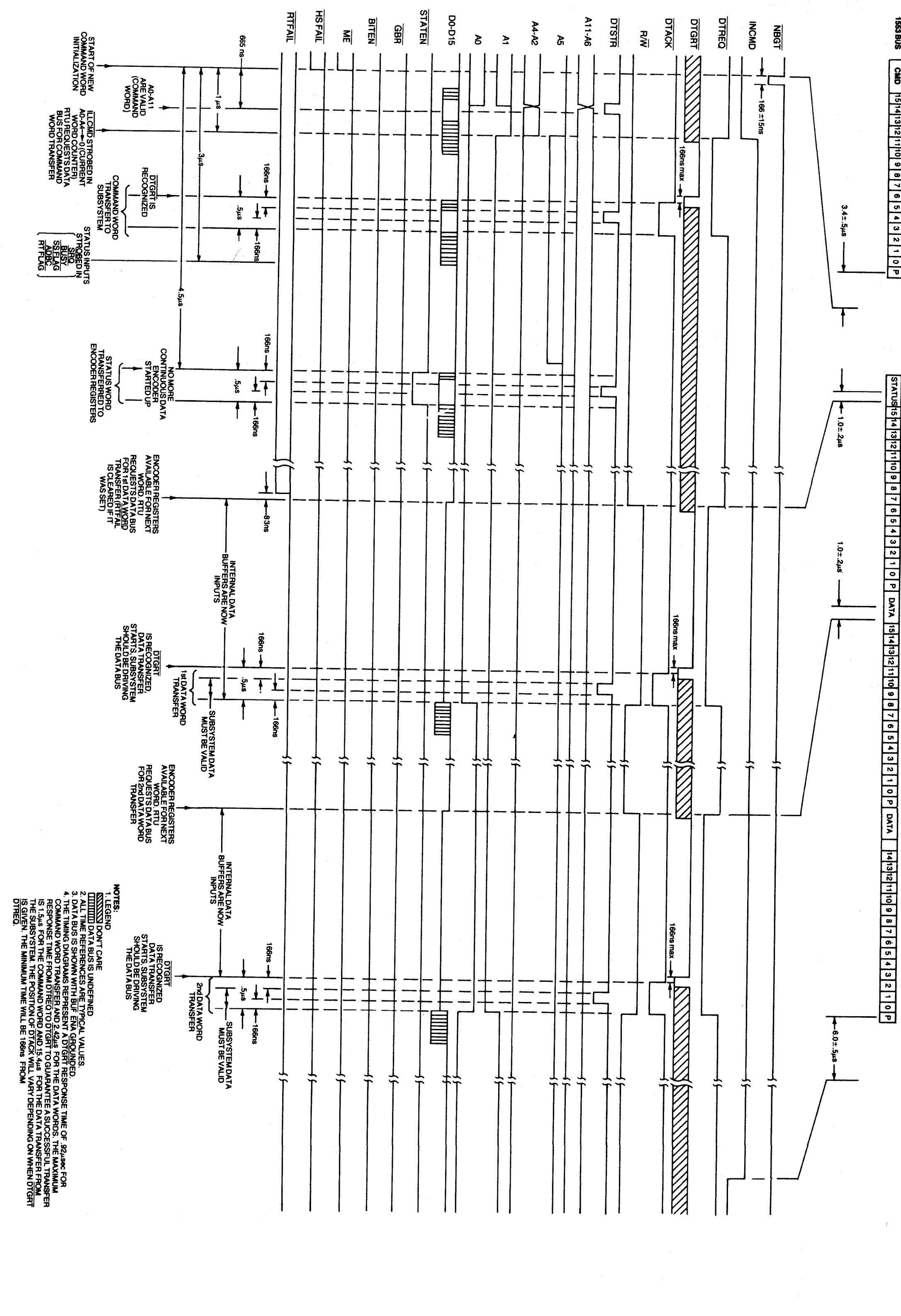


FIGURE 2. TRANSMIT TIMING DIAGRAM

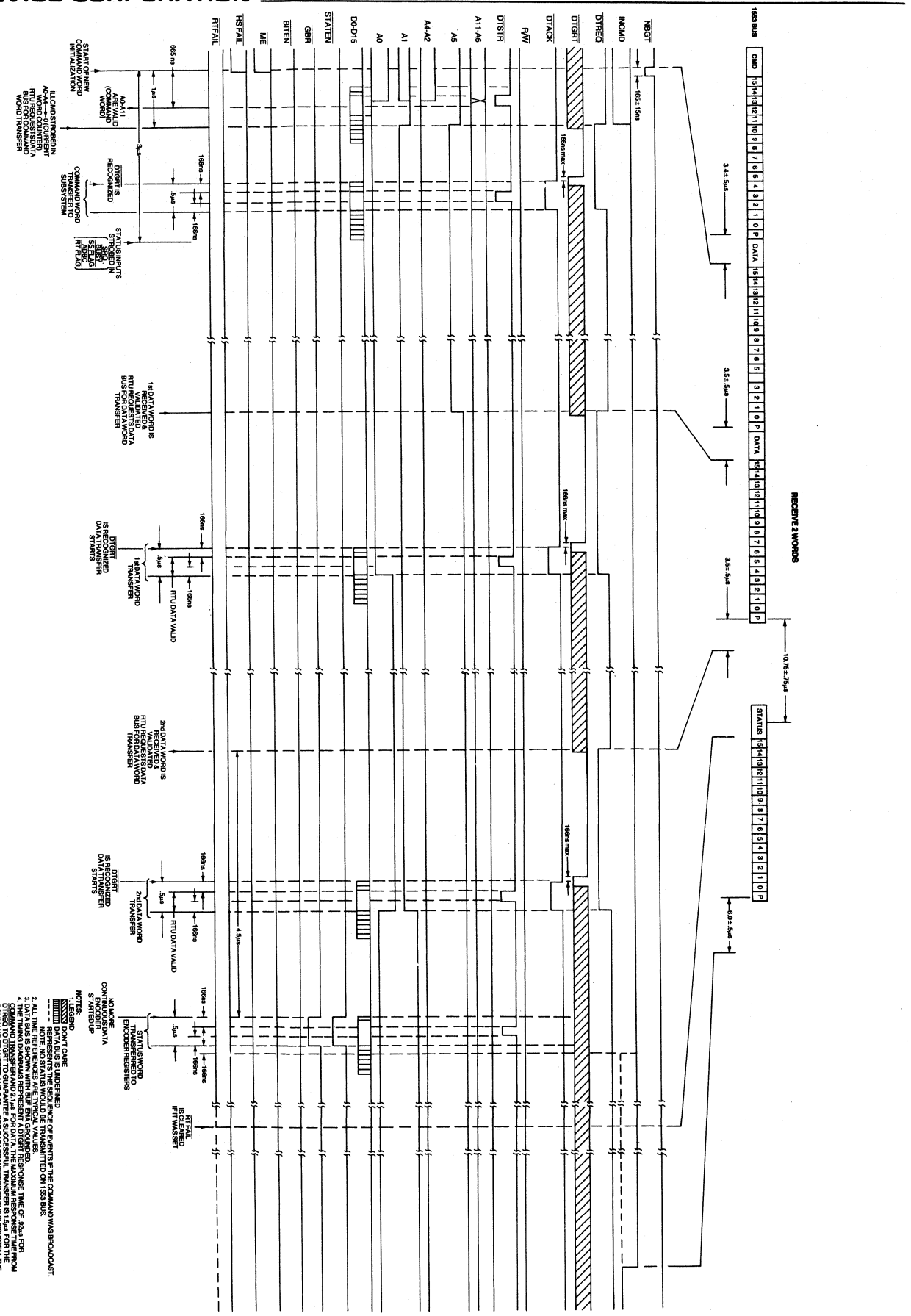


FIGURE 3. RECEIVING TIMING DIAGRAM

ERROR FLAGS

Four error flags are output to the subsystem to provide information on the condition of the BUS-65112. The Message Error ($\overline{ME}$) line goes LOW if any of the following error conditions exist: format error, word count error, invalid word, sync error, RT to RT address error or T/R bit error. The Remote Terminal Failure ($\overline{RT\ FAIL}$) line goes LOW whenever the results of the continuous wrap-around self-test shows a discrepancy, or the transmitter watchdog timeout has occurred. The Handshake Failure ($\overline{HS\ FAIL}$) line goes LOW whenever the subsystem has not responded to a $\overline{DTREQ}$ request soon enough with a $\overline{DTGRT}$ grant. The RT Address Error ($\overline{RTAD\ ERR}$) line goes LOW whenever the sum of the 5 address lines and parity line shows a parity error.

STATUS REGISTER

Six inputs to the BUS-65112 allow the subsystem host CPU to control bits in the RTU Status Word. The Illegal Command input may be used to set the Message Error bit in the Status Word. This line is particularly useful in illegalizing any combination of mode commands. An external PROM may be used to monitor the latched Command Word. This PROM would drive the Illegal Command input LOW when it identifies a mode command that is programmed to be illegal.

The Subsystem Request ($\overline{SRQ}$) line is used to set the service request bit in the Status Word. The Accept Dynamic Bus Control ($\overline{ADBC}$) line is used to set the Bus Control acceptance bit in the Status Word, if that mode command was sent. The Remote Terminal Flag ($\overline{RT\ FLAG}$) line is used to set the terminal flag bit in the Status Word. The Subsystem Busy ($\overline{BUSY}$) line is used to set the busy bit in the Status Word, and to inhibit requests for data from the subsystem. The Subsystem Flag ($\overline{SS\ FLAG}$) line is used to set subsystem flag (fault) bit in the Status Word.

BUILT-IN-TEST WORD

The BUS-65112 contains a 14 bit Built-In-Test (BIT) word register which stores information about the condition of the Remote Terminal. When a Mode Command is received to transmit BIT word, the contents of this register are transmitted over the 1553 data bus. Figure 4 shows the meaning of each bit in the BIT register. Information is included regarding transmitter timeouts, loop test failures, transmitter shutdown, subsystem handshake failure, and the results of individual message validations.

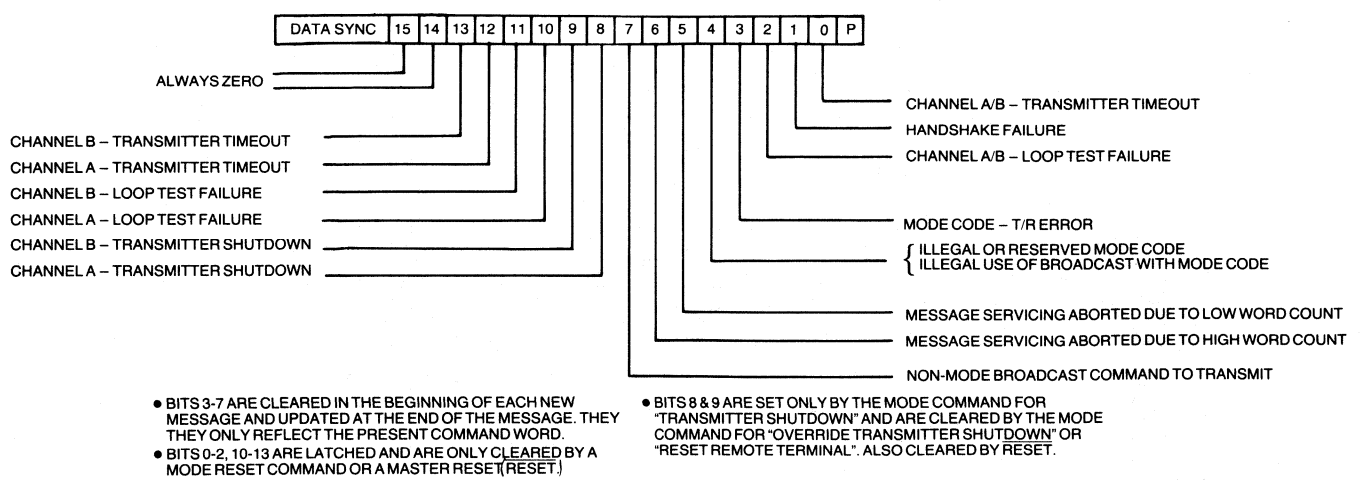


FIGURE 4. BUILT-IN TEST (BIT) WORD REGISTER

PIN FUNCTION TABLE		
PIN	**FUNCTION**	**DESCRIPTION**
1	A10	Latched output of the most significant bit (MSB) in the subaddress field of the command word.
2	A8	Latched output of the third most significant bit in the subaddress field of the command word.
3	A6	Latched output of the least significant bit (LSB) in the subaddress field of the command word.
4	DB1	Bi-directional parallel data bus Bit 1
5	DB3	Bi-directional parallel data bus Bit 3
6	DB5	Bi-directional parallel data bus Bit 5
7	DB7	Bi-directional parallel data bus Bit 7
8	DB9	Bi-directional parallel data bus Bit 9
9	DB11	Bi-directional parallel data bus Bit 11
10	DB13	Bi-directional parallel data bus Bit 13
11	DB15	Bi-directional parallel data bus Bit 15 (MSB)
12	BRO ENA	Broadcast enable – when HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW, it prevents response to RT address 31 unless it was the assigned terminal address.
13	ADDRE	Input of the MSB of the assigned terminal address.
14	ADDRC	Input of the 3rd MSB of the assigned terminal address.
15	ADDRA	Input of the LSB of the assigned terminal address.
16	$\overline{\text{RTADERR}}$	Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will respond to broadcast commands if BRO ENA is HIGH.
17	$\overline{\text{TXDATA B}}$	LOW output to the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
18	+15VB	+15 volt input power supply connection for the B channel transceiver.
19	GND B	Power supply return connection for the B channel transceiver.
20	RXDATA B	Input from the HIGH side of the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
21	A3	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 2nd MSB of the current word counter.
22	A1	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter.

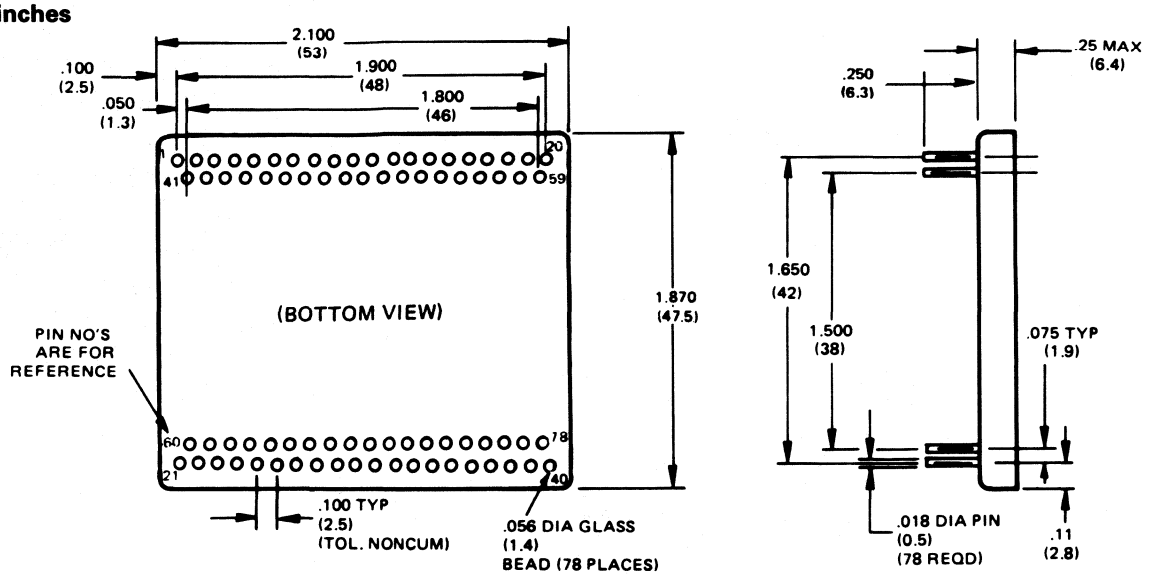
PIN FUNCTION TABLE		
PIN	**FUNCTION**	**DESCRIPTION**
23	$\overline{\text{DTGRT}}$	Data transfer grant – active LOW input signal from the subsystem that informs the RT, when $\overline{\text{DTREQ}}$ is asserted, to start the transfer. Once transfer is started, $\overline{\text{DTGRT}}$ can be removed.
24	INCMD	In Command – HIGH level output signal used to inform the subsystem that the RT is presently servicing a command.
25	$\overline{\text{HSFAIL}}$	Handshake Fail – output signal that goes LOW and stays LOW whenever the subsystem fails to supply $\overline{\text{DTGRT}}$ in time to do a successful transfer. Cleared by the next $\overline{\text{NBGT}}$.
26	$\overline{\text{DTSTR}}$	A LOW level output pulse (166ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommend using the rising edge to clock data in.
27	A5	Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transferred.
28	$\overline{\text{RTFAIL}}$	Remote Terminal Failure – latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Cleared by the start of the next message transmission (status word) and set if problem is again detected.
29	$\overline{\text{DTREQ}}$	Data Transfer Request – active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay LOW until transfer is completed or transfer timeout has occurred.
30	$\overline{\text{ADBC}}$	Accept Dynamic Bus Control – active LOW input signal from subsystem used to set the Dynamic Bus Control Acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control.
31	TEST 2	Factory test point – DO NOT USE.
32	A11	Latched output of the T/R bit in the command word.
33	$\overline{\text{ILLCMD}}$	Illegal Command – Active LOW input signal from the subsystem, strobed in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register.
34	$\overline{\text{SRQ}}$	Subsystem Service Request – Input from the subsystem used to control the Service Request Bit in the status register. If LOW when the status word is updated, the Service Request Bit will be set; if HIGH, it will be cleared.
35	$\overline{\text{BITEN}}$	Built-in-Test Word Enable – LOW level output pulse (.5μsec), present when the built-in-test word is enabled on the parallel data bus.
36	$\overline{\text{RXDATA A}}$	Input from the LOW side of the primary side of the coupling transformer that connects to the A Channel of the 1553 Bus.
37	+5VA	+5 volt input power supply connection for the A channel transceiver.

PIN FUNCTION TABLE		
PIN	**FUNCTION**	**DESCRIPTION**
38	−15VA	−15 volt input power supply connection for the A Channel transceiver.
39	TXDATA A	HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
40	$\overline{\text{NBGT}}$	New Bus Grant – LOW level output pulse (166 ns) used to indicate the start of a new protocol sequence in response to the command word just received.
41	A9	Latched output of the 2nd MSB in the subaddress field of the command word.
42	A7	Latched output of the 2nd LSB in the subaddress field of the command word.
43	DB0	Bidirectional parallel data bus Bit 0 (LSB)
44	DB2	Bidirectional parallel data bus Bit 2
45	DB4	Bidirectional parallel data bus Bit 4
46	DB6	Bidirectional parallel data bus Bit 6
47	DB8	Bidirectional parallel data bus Bit 8
48	DB10	Bidirectional parallel data bus Bit 10
49	DB12	Bidirectional parallel data bus Bit 12
50	DB14	Bidirectional parallel data bus Bit 14
51	+5V	+5 Volt input power supply connection for RTU digital logic section.
52	GND	Power supply return for RTU digital logic section.
53	ADDRD	Input of the 2nd MSB of the assigned terminal address.
54	ADDRB	Input of the 2nd LSB of the assigned terminal address.
55	ADDRP	Input of Address Parity Bit. The combination of assigned terminal address and ADDRP must be odd parity for the RT to work.
56	TXDATA B	HIGH, output to the primary side of the coupling transformer that connects to the B Channel of the 1553 Bus.
57	−15VB	−15 volt input power supply connection for the B channel transceiver.
58	+5VB	+5 volt input power supply connection for the B channel transceiver.
59	$\overline{\text{RXDATA B}}$	Input from the LOW side of the primary side of the primary side of the coupling transformer that connects to the B Channel of the 1553 Bus.
60	A2	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter.
61	A0	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the LSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the LSB of the current word counter.
62	$\overline{\text{DTACK}}$	Data Transfer Acknowledge – active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the $\overline{\text{DTGRT}}$ in response to $\overline{\text{DTREQ}}$ and is presently doing the transfer. Can be connected directly to pin 67 ($\overline{\text{BUF ENA}}$) for control of tri-state data buffers; and to tri-state address buffer control lines, if they are used.

PIN FUNCTION TABLE		
PIN	**FUNCTION**	**DESCRIPTION**
63	A4	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the MSB of the current word counter.
64	R/$\overline{\text{W}}$	Read/$\overline{\text{Write}}$ – output signal that controls the direction of the internal data bus buffers. Normally, the signal is LOW and the buffers drive the data bus. When data is needed from the subsystem, it goes HIGH to turn the buffers around and the RT now appears as an input The signal is HIGH only when $\overline{\text{DTREQ}}$ is active (LOW).
65	$\overline{\text{GBR}}$	Good Block Received – LOW level output pulse (.5μsec) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem.
66	12MHz IN	12MHz Clock Input – input for the master clock used to run RTU circuits.
67	$\overline{\text{BUF ENA}}$	Buffer Enable – input used to enable or tri-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to $\overline{\text{DTACK}}$ (Pin 62) if RT is sharing the same data bus as the subsystem.
68	$\overline{\text{RESET}}$	Input resets entire RT when LOW.
69	$\overline{\text{RTFLAG}}$	Remote Terminal Flag – input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set; if HIGH, it would be cleared. Normally connected to $\overline{\text{RTFAIL}}$ (Pin 28).
70	TEST 1	Factory test point – DO NOT USE.
71	$\overline{\text{BUSY}}$	Subsystem Busy – input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will still be transferred to subsystem.
72	$\overline{\text{SSFLAG}}$	Subsystem Flag – input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH, it will be cleared.
73	$\overline{\text{ME}}$	Message Error – output signal that goes LOW and stays LOW whenever there is a format or word error with the received message over the 1553 Data Bus. Cleared by the next $\overline{\text{NBGT}}$.
74	RXDATA A	Input from the HIGH side of the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
75	GNDA	Power supply return connection for the A Channel transceiver.
76	+15VA	+15 volt input power supply connection for the A channel transceiver.
77	$\overline{\text{TXDATA A}}$	LOW output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
78	$\overline{\text{STATEN}}$	Status Word Enable – LOW level active output signal present when the status word is enabled on the parallel data bus.

MECHANICAL OUTLINE

Dimensions in inches (millimeters)



ORDERING INFORMATION

BUS-65112-883

Power Supply Option:
2 = ±15 VDC
3 = ±12 VDC

Mating Data Bus
Transformer: BUS-25679

Mating Socket Textool
#278-5605-01

ILC DATA DEVICE CORPORATION

MIL-STD-1553 TO MIL-STD-1750 INTERFACE HYBRID

ADVANCE INFORMATION*

FEATURES:

- *COMPATIBLE WITH 1750 CPUs SUCH AS FAIRCHILD F9450 AND MDAC 281*
- *COMPATIBLE WITH 1553 BC/RTUs AND RTUs SUCH AS DDC'S BUS-65600 AND BUS-65112*
- *SMALL 1.9" x 2.1" HYBRID*
- *INTELLIGENT INTERFACE MINIMIZES 1750 CPU OVERHEAD*
- *INTERNAL MICROCODE CONTROLLER TRANSFERS COMPLETE 1553 MESSAGES TO A DUAL PORT RAM*
- *PROVIDES BUFFER CONTROLS FOR 1750 ADDRESS BUS AND DATA BUS*
- *INCLUDES REGISTERS FOR COMMAND WORD, INTERRUPT WORD AND MODE CONTROL WORD.*

DESCRIPTION:

The BUS-66300 hybrid provides a complete intelligent interface between a MIL-STD-1553 Bus Controller and/or Remote Terminal and a MIL-STD-1750 CPU. It is compatible with standard 1750 CPUs such as the Fairchild F9450 and the McDonnell Douglas MDAC 281. It is also compatible with DDC's single package 1553 BC/RTU (BUS-65600) and single package 1553 RTU (BUS-65112). Packaged in a small 1.9" x 2.1" hermetic hybrid, the BUS-66300 minimizes the 1750 CPU overhead required to service a 1553 I/O port.

Making use of its internal microcode controller, command register, and word counter, the BUS-66300 transfers complete 1553 messages to a dual port RAM with no 1750 CPU intervention. Internal memory contention control circuits provide the 1750 CPU with immediate access to the dual port RAM. The BUS-66300, plus the dual port RAM, makes the 1553 I/O port appear to the 1750 CPU as a block of memory.

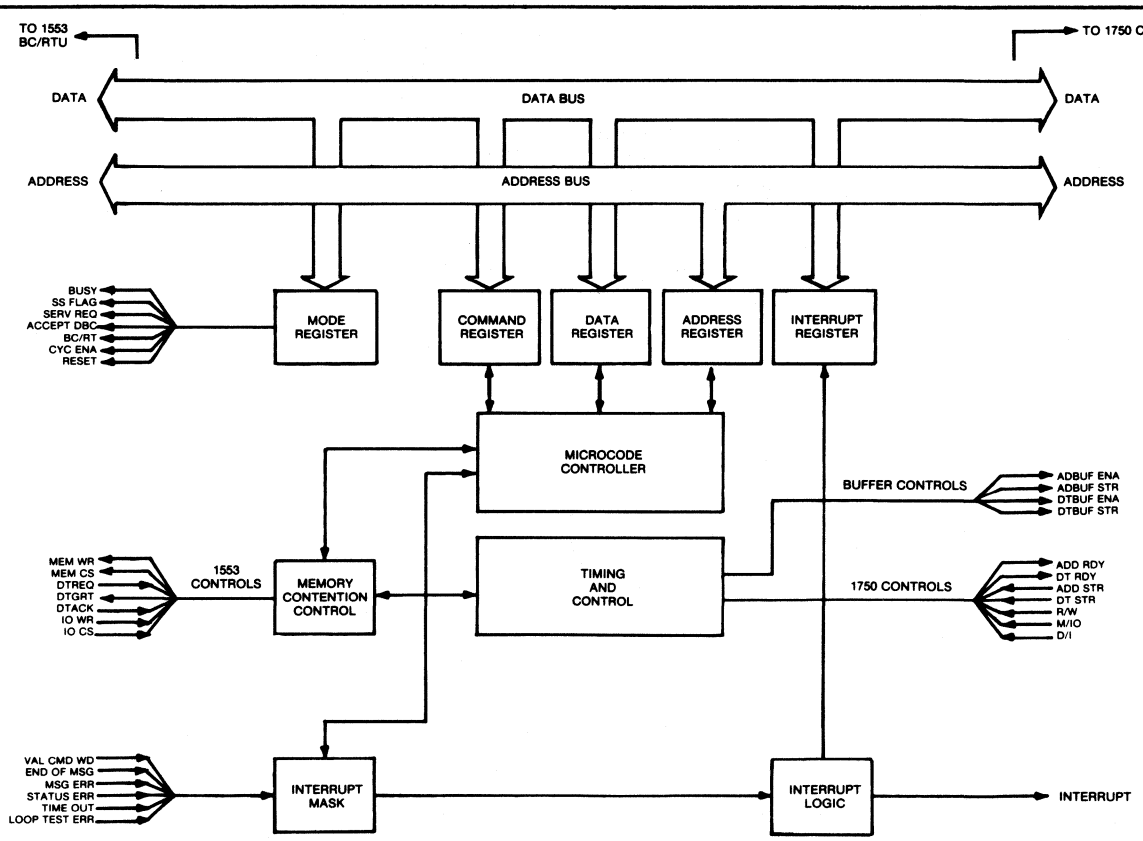


FIGURE 1. BUS-66300 BLOCK DIAGRAM

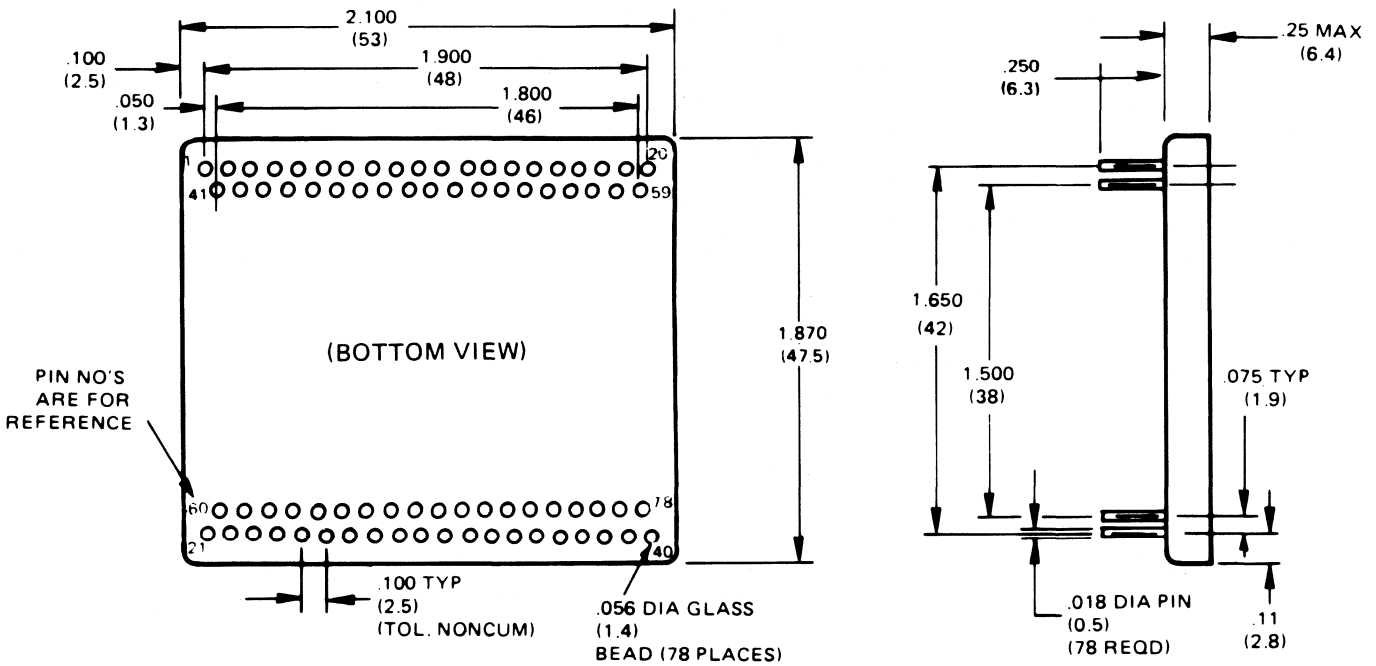
*In accordance with JEDEC Publication No. 103, this notice contains information on a new product. Specifications in the information herein are subject to change without notice.

The BUS-66300 provides buffer control output lines which allow the 1750 CPU address bus and data bus to be isolated with bidirectional tri-state buffers. A single interrupt line is provided to the 1750 CPU, although 6 interrupt inputs are accepted from the 1553 BC/RTU. The internal Interrupt Register allows the 1750 CPU to identify which interrupt has taken place. The BUS-66300 also contains a mode register for storing the 1553 Mode Control Word. This word contains subsystem selectable bits of the 1553 RTU Status Word, a BC/RTU mode selection bit, a BC message start bit, and a reset bit. The BUS-66300 also provides the 1553 BC/RTU with DMA type handshaking data transfer control lines.

The BUS-66300 is screened in accordance with the requirements of MIL-STD-883, and it operates over the full military -55° C to +125° C temperature range. Its small hermetic package, compatibility with standard 1750 CPUs and 1553 BC/RTUs, and intelligent features make the BUS-66300 ideal for any application requiring an interface between MIL-STD-1553 and MIL-STD-1750 equipment.

MECHANICAL OUTLINE

Dimensions in inches (millimeters)



ORDERING INFORMATION

BUS-66300-883

NOTES

PRODUCT INDEX

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*Products listed in Addendum became available after our production closing date.

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